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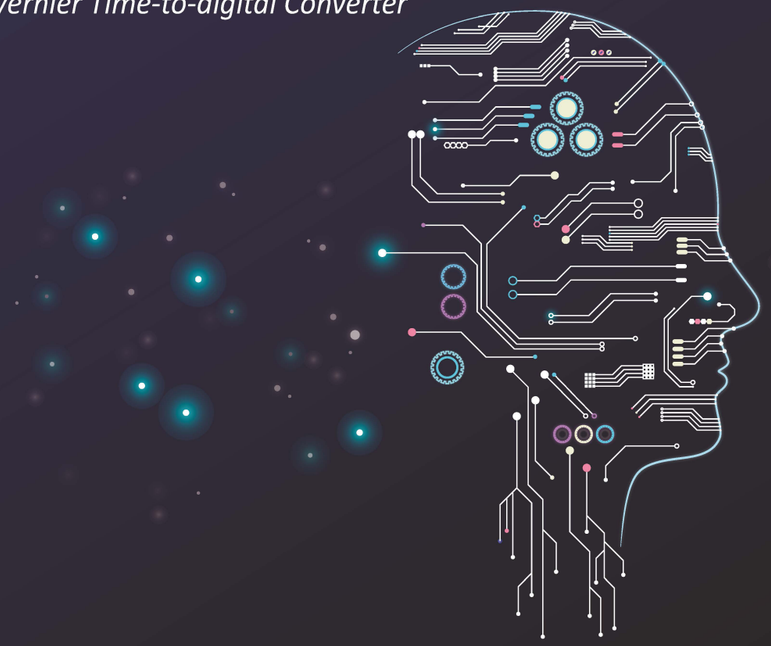
Nonlinearity Analysis
of 65nm 8bit Vernier Time-to-digital Converter



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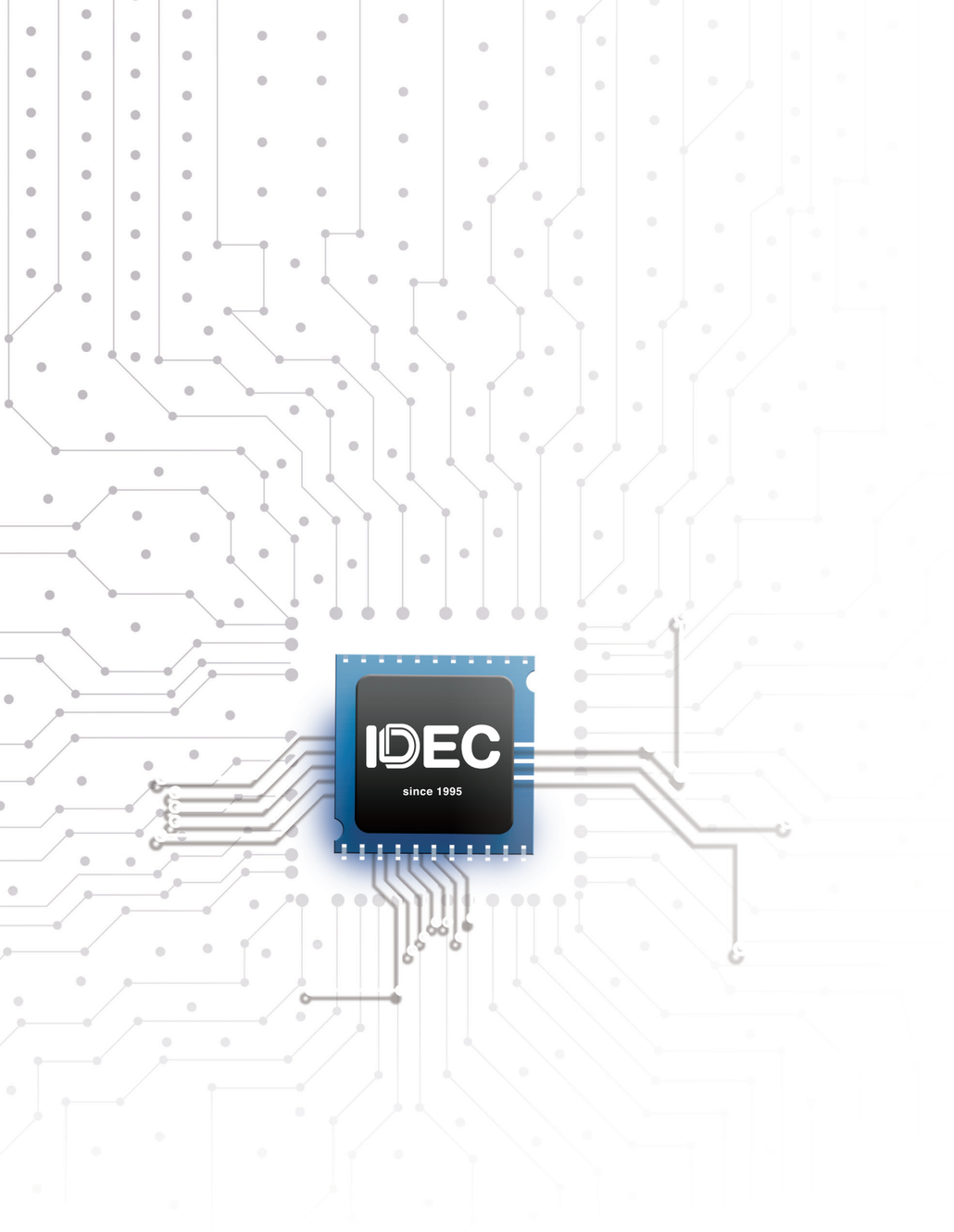

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CONTENTS

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Design and analysis of embedded flexible packages for wearable device wireless power transfer scheme

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***Abstract* -In this paper, we introduce a wireless power transfer (WPT) scheme using flexible coils and electronic circuits for wearable devices and future flexible devices. Recently, a flexible wearable market is rapidly growing and much effort is made to transform rigid devices into flexible devices. The reason is to provide the comfortable user environment. To realize the flexible devices, electronic circuits must be flexible. Therefore, we designed the voltage-controlled oscillator to analyze the oscillation characteristics with the bending radius. In this paper, we will discuss about a WPT scheme to deliver power to the VCO and designing process of the VCO by considering the effect of thin silicon substrate. To design the VCO, we used SK-Hynix 350 nm CMOS process.**

***Keywords*—Embedded packages, Flexible chip, Flexible printed circuit board, Wireless power transfer, Voltage-controlled oscillator**

I. INTRODUCTION

Wireless power transfer technology is very powerful methods to transfer power from one device to another device through an air space without any wired connection [1]. This technology is wieldy used in applications ranging from low power wearable devices to high power transportation [2], [3]. Especially, the WPT technology on a wearable device provides several useful functions. Firstly, the device can be protected from water or dust by removing power connectors on the surface. Secondly, any mechanical damage such as wear and tear can be removed by avoiding mechanical contacts between power connectors. Moreover, the wearable devices can be easily charged up by simply placing the devices on a wireless charging platform. However, the conventional wireless charging technology has several limitations. In the existing wearable devices, the wireless charging scheme is implemented in the flat or rigid surface of the device. This scheme increases the size of the devices and limits the freedom of design.

Fig. 1 shows the concept of the proposed WPT system using flexible coil and circuits. A polyimide substrate will be used to implement the system and face up, face down and

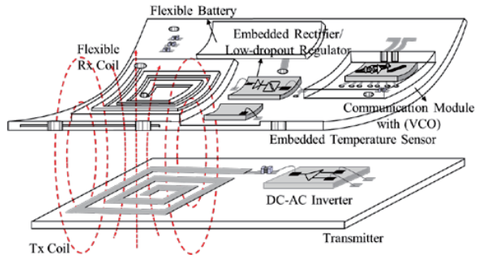

Fig. 1. Proposed wireless power transfer (WPT) scheme using the embedded flexible packages. Power will be delivered through the flexible coils using magnetic field resonance. The rectifier and regulator chips were embedded in the flexible PCB to rectify and regulate the received AC power. Finally, the regulated power will be delivered to the embedded VCO.

embedded packing on the flexible substrate is considered depending on the electronic components. The proposed system enables WTP system with entire flexible environment. The flexible coils were used to deliver the power and rectifier and low-dropout regulator (LDO) were used to rectify and regulate the received AC power for low power application. Finally, the regulate power will be used to supply the VCO. The LC VCO generates the 433 MHz AC voltage at the output. To verify the proposed scheme, power transfer efficiency and voltage transfer ratio between two isolated devices will be analyzed through measurement. More details about the designing process of the VCO with the variation of silicon substrate will be discussed in the later

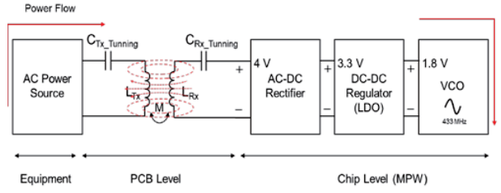

Fig. 2. Overall system block-diagram of the proposed wearable device wireless charging scheme.

section.

Fig. 2 shows the overall system block-diagram of the proposed wearable device wireless charging scheme. On the input side, the AC power will be supplied to excite the Tx coil to produce the magnetic field. The matching capacitor is

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added in series to minimize the reactive components from the LC resonant circuit. On the Rx side, the Rx coil receives the alternating magnetic field and the voltage will be induced on the Tx side by Faraday' law [4]. The received AC power will be rectified and regulate to charge up the battery in the device or directly supply the VCO for wireless communication.

II. SIMULATION AND MEASUREMENT RESULTS OF THE PROPOSED WIRELESS POWER TRANSFER SCHEME

To analyze the proposed wearable device wireless charging scheme using the wireless charging receiver, we designed the overall system as shown in Fig.3. The wearable device wireless charging system uses power sources as a commercial electricity and an AC power adapter was used to invert the AC voltage into the 12V DC voltage. The 12 V DC voltage is supplied to an input of the buck-converter that controls the total amount power to be delivered to the wearable device. The regulated DC voltage will be inverted into AC voltage for the WPT using magnetic field resonance. The received AC voltage on the Rx side will be rectified through the full-bridge rectifier. The rectified voltage will be regulated by the LDO to charge up the battery of the device.

We simulated the wearable device wireless charging system to compare with the actual measurement results obtained from the implemented system. Fig. 4 shows the time-domain voltage waveform comparison between the model parameter based simulation and measurement. Due to the parasitic components exist in the system, the measured

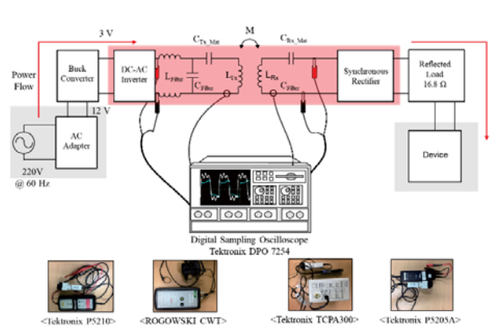

Fig. 3. Measurement setup of Tx and Rx coil voltage and current waveforms using voltage and current probes.

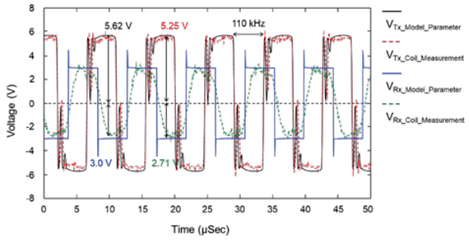

Fig. 4. Comparison between the time-domain voltage waveform simulation and measurement results.

waveforms were degraded. However, the voltage waveforms show the good correlation between the model parameter based simulation and the measurement. Fig.5 shows the comparison between the simulated current waveforms using with the measurement results. Those current waveforms were captured at the Tx and Rx WPT coils as illustrated in the Fig 3. As the results, the amplitudes and the frequency components of the current waveforms between the model parameter based simulation and the measurement results were correlated well with high precision.

III. FLEXIBLE LC VOLTAGE CONTROLLED OSCILLATOR CHIP DESIGN FOR WIRELESS COMMUNICATION FOR FLEXIBLE WEARABLE DEVICES

In the previous chapter, we discussed the simulation and experiments results for the WPT. In this chapter, we will discuss the flexible chip design of the flexible wearable devices. By using SK Hynix 350 nm CMOS process, we will design and fabricate the flexible WPT Rx module to analyze the effect on the current and voltage waveforms and finally the power transfer efficiency due to the bending of the fabricated ICs on the flexible substrate. Also, for the communication module in the devices, we designed the voltage-controlled oscillator (VCO). The VCO is very sensitive to the external environment such as temperature, humidity, and voltage variation. Due to this behavior, we will analyze the operating frequency of the VCO depending on the mechanical stress. Fig. 6 shows the circuit of the LG -G_M

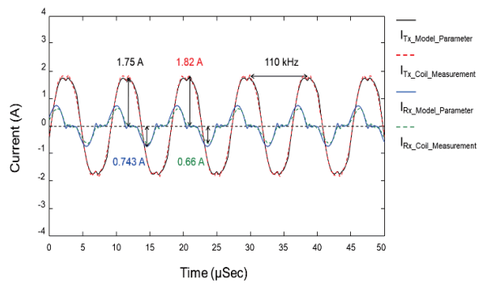

Fig. 5. Comparison between the time-domain current waveform simulation and measurement results.

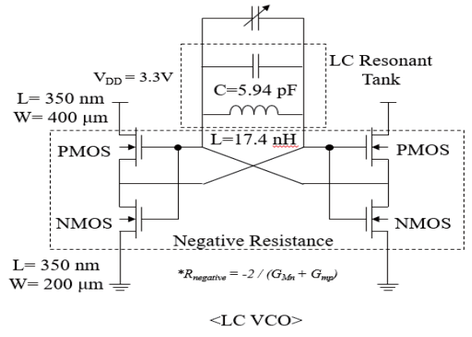

Fig. 6. Designed the LC -G_M voltage controlled oscillator (VCO) circuit

VCO. The LC resonant tank is used for the oscillation. To avoid the oscillation without damping, the negative resistance circuit is designed. Moreover, the MOS varactor is used to control the operating frequency. However, the SK Hynix 350 nm process does not provide the varactor, therefore, we change the capacitance value to control the operating frequency of the VCO.

For the VCO circuit, an inductor is the main component to oscillate the output waveform. Therefore, we designed the on-chip inductor by changing the designed variables using a 3D EM simulation tool. TABLE I shows the designed on-chip inductor parameters using the 3D EM simulation. Fig. 7 shows the 3D EM simulation result of the designed on-chip inductor. The inductor is designed to achieve the highest Q-factor at 433 MHz for VCO operation. To oscillate the output waveform of the VCO, we used a polysilicon-insulator-polysilicon (PIP) capacitor that can be used in 350 nm process. Once we have designed the on-chip inductor, we simulate the self-impedance Z_{self} of the inductor with the variation of the silicon substrate thickness as shown in Fig. 8. As the results, the self-inductance of the on-chip inductor varies with the thickness of the silicon substrate. As we increase the thickness of the silicon substrate, the self-resonance frequency of the inductor is reduced. This means the inductance of the capacitance of the inductor can be changed due to the thickness of the silicon substrate.

To realize the flexible devices, we need to make the thinner silicon substrate less than 50μm. However, the thickness of the silicon substrate without the back grinding is greater than 100μm. This means if we design the on-chip inductor with the 100μm silicon thickness, then the inaccuracy of the VCO resonance frequency will be produced due to the reduction of the thickness of the silicon substrate. During the design process, we need to consider the target thickness of the silicon substrate. In this paper, we set the silicon substrate thickness as 50μm since it is harder to achieve the thickness less than 50μm with the diced chips. By considering the above design guides, we apply the designed on-chip inductor using the 3D EM simulation to the actual layout of the on-chip inductor for the VCO.

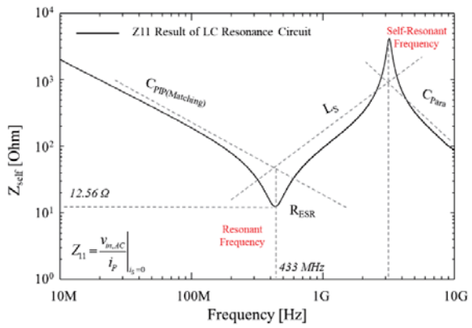

Fig. 7. Self-impedance (Z_{self}) 3D EM simulation results of on-chip inductor. We optimize the on-chip inductor to achieve the higher Q-factor at the resonance frequency.

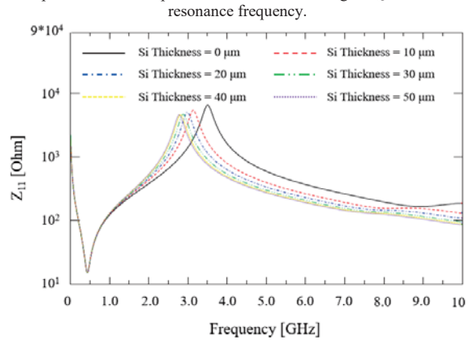

Fig. 8. Changes in the Self-impedance of the on-chip inductor with the variation of the Si substrate thickness.

Fig. 9 shows the voltage waveform output of the designed LC VCO using the Virtuoso circuit simulation tool. The output waveform shows the operating frequency at 433 MHz with the swing voltage of 2.8V. Fig 10 shows the Fast Fourier Transform (FFT) results of the output voltage waveform. As indicated in the graph, the fundamental component is located at 433MHz.

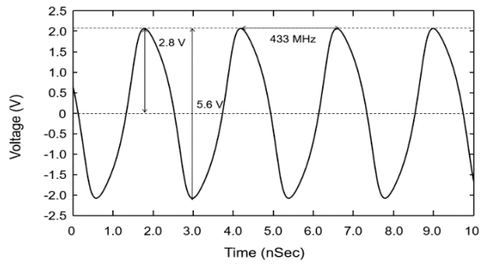

Fig. 9. The output voltage waveform of the designed LC VCO using a circuit simulation tool. The voltage waveform shows the oscillation frequency at 433 MHz

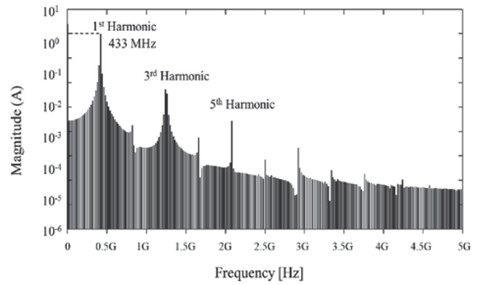

Fig. 10. Fast Fourier Transform (FFT) simulation result of the output voltage waveform.

TABLE I.

Designed On-chip Inductor Parameters

Design Parameter	Value
Line Width	30 μm
.Line Space	1 μm
Metal Thickness	0.7 μm
Coil Dimension	700 x 700 μm^2
Coil Turn	4 turn

IV. MEASUREMENT RESULT OF FABRICATED VOLTAGE CONTROLLED OSCILLATOR

Fig. 11 shows the fabricated on-chip inductor and voltage controlled oscillator (VCO) using SK Hynix 350 nm process. The on-chip inductor pattern for the VCO is designed individually to analyze the inductor characteristic itself since the inductor is one of the main components for the VCO. To measure the designed chip, we designed the probing pads with the 250 μm pitch.

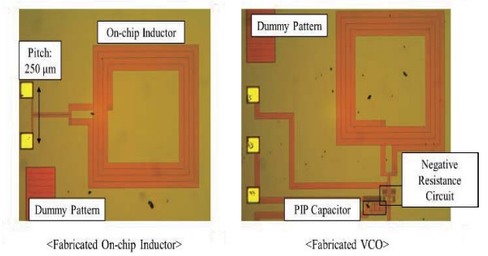

Fig. 11. Fabricated on-chip inductor and voltage controlled oscillator using SK Hynix 0.35 μm process.

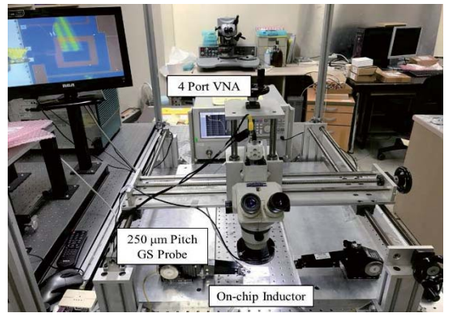

Fig. 12. The measurement setup of the fabricated on-chip inductor pattern using probe station and 4-port VNA

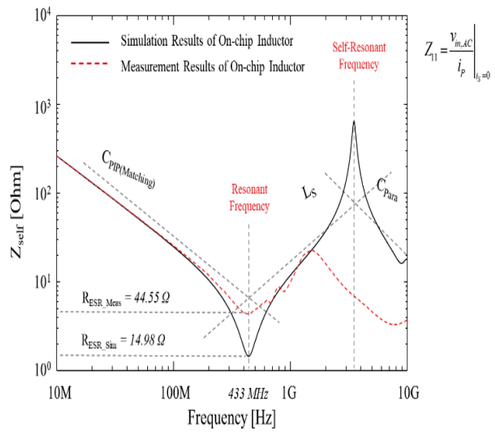

Fig. 13. The self-impedance Z_{self} measurement result of the fabricated on-chip inductor pattern.

Fig. 12 shows the measurement setup of the fabricated on-chip inductor pattern. To measure the inductor pattern, we used the 4-port vector network analyzer (VNA). By using the VNA, we can measure the self-impedance of the inductor. To measure the fabricated VCO, we provide the four probing pads. One pair is used for the input supply and another pair is used for the bias voltage.

When we measure the self-impedance Z_{self}, we set the target frequency range between 300 kHz and 10 GHz. In this range, we can analyze the resonance of the designed inductor with the matching capacitor for the oscillation and the self-resonance by the parasitic capacitance of the inductor. Fig. 13 indicates the Z_{self} of the on-chip inductor. The first declining section of the graph indicates the impedance of the matching capacitor. At 433 MHz, the resonance is produced due to design the inductor pattern with the matching capacitor. At this frequency, the only the real term exists since the reactive components of the inductor and the capacitance are canceling each other. Above the 433 MHz, the inclining section indicates the self-inductance of the inductor pattern. At higher frequency region above 3 GHz, the self-resonance is produced due to parasitic capacitance

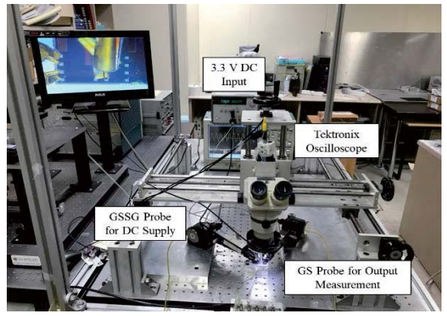

Fig. 14. The measurement setup of the fabricated voltage controlled oscillator (VCO) using the DC supply and oscilloscope.

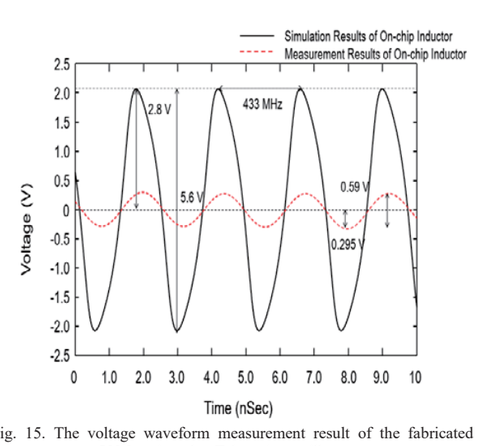

Fig. 15. The voltage waveform measurement result of the fabricated VCO using the Tektronix oscilloscope.

This parasitic capacitance comes from the overlapping region of the top and the bottom metal in the inductor. In the graph, the self-resonance from the measurement result is much lower than the 3D EM simulation results. This means the parasitic capacitance of the actual system is much higher than the simulation results.

Moreover, the measurement result of the equivalent series resistance (ESR) is much higher than the 3D EM simulation results. From the measurement, we achieved the 44.55 Ω at 433MHz. However, in the simulation result, the ESR is 14.98 Ω, which is one third of the measurement result. This higher ESR leads the lower Q-factor and degrades the system performance. To avoid the degradation of the Q-factor, we can take out the inductor pattern from the chip to the PCB.

Fig. 14 shows the measurement setup of the fabricated VCO. To measure the fabricated VCO, we supplied 3.3 DC input voltage to operate the VCO. The GSSG probe is used to supply the input voltage and bias voltage. On the output side, the Tektronix oscilloscope is used to measure the output voltage waveform. The GS probe is used to measure the output voltage waveform.

The red line in Fig. 15 shows the measurement result of the VCO. In comparison to the simulation results, the output oscillation is largely decreased. This is due to larger ESR on the on-chip inductor and PIP capacitor for matching. Even the output oscillation is very less, the designed VCO operate at 433 MHz with the peak to peak voltage of 0.59 V. In our research, we will analyze the VCO output depending on the mechanical stress as we bend the flexible PCB with embedded VCO chips.

V. RESULTS

In this paper, we firstly design the wireless power transfer (WPT) scheme using flexible coils for the flexible wearable devices. From the measurement result, we achieved coil to coil power transfer efficiency of 50.3% where the input power from the transmitter is 3.36 W while the output power from the receiver coil is 1.69 W. For the power transfer efficiency calculation, we used average power calculation using MATLAB tool to calculate the power efficiency from the measured voltage and current waveforms. We also simulated overall DC-DC power transfer efficiency of the proposed system. The input DC power of the buck-converter is 4.67 W and the output DC power delivered at the load is 1.4 W. The power transfer efficiency of the proposed system is 30%. Since the wearable device WPT system delivers very low amount power, the power transfer efficiency can be lower than the high power WPT system due to fixed power losses such as forward voltage drops of the diodes in the rectifier circuit. Compared to the Smartphone wireless charging system which has 50% of power transfer efficiency, 30% power transfer efficiency is not very low.

Once we finish the WPT system design using flexible coils, we designed the LC voltage controlled oscillator (VCO). The input power will be supplied from the WPT system and VCO chip will be flexible for the flexible wearable devices. To design the VCO, we focused on the on-chip inductor design. As the results, as we increase the thickness of the silicon substrate, the self-resonance frequency of the on-chip inductor is decreased. Therefore, we designed the on-chip inductor at 433 MHz with the thickness of 50 μm. Finally, the fabricated VCO is measured As the result, the amplitude of the oscillation is largely decreased in comparison to the simulation due to higher equivalent series resistance (ESR) of the on-chip inductor. However, the designed VCO operates at 433 MHz.

VI. DISCUSSION

To measure the effect of the curvature on the flexible chips, we need to put the fabricated chips on a flexible substrate. In our case, we will use Polyimide substrate, which has good electrical and thermal characteristics. Moreover, the Polyimide has good bending properties. The packaging of flexible circuits on the flexible substrate will be proceeded from Korea Institute of Machinery & Materials (KIMM). Firstly, the fabricated chip will be grinded to obtain the thin flexible chips. The thickness of the chips will be less than 50 μm to have a flexibility. Typically, 25 μm thick chips can have bending radius of 1 cm [5]. In our case, the mechanical stress on the chip due to the bending is not significant since we apply the flexible system on a wearable device, which has bending radius larger than the bending radius of a human wrist. To mount the chip on the PCB, the printing type interconnection technique will be used. This technique allows direct attachment of the flexible chips on the flexible PCB since it can realize the line pattern and pitch less than 50 μm. Therefore, the gap between the PCB level and wafer level can be removed.

VII. FURTHER WORK

The fabricated VCO will be processed by KIMM to make the thinner silicon substrate. Since the Si substrate is very thin, the fabricated chip can have flexible properties. Through the bulk etching process, the designed chip can have the flexible properties. Once we obtained the flexible VCO chip, we will test the output characteristics of the VCO depending on the silicon thickness. Once the VCO operates with the targeted thickness of the silicon substrate, we will mount on the flexible PCB. Finally, the VCO will be tested under the flexible environment.

VIII. CONCLUSION

In this paper, we proposed the wireless power transfer scheme using the flexible coils for wearable device and future flexible devices. Currently, the existing wireless power Rx module is implemented on the rigid FR4 PCB. To realize entire flexible device, the Rx chips must be flexible. Therefore, we design the VCO considering the thickness of the silicon substrate for a communication module in the wearable device. The on-chip inductor of the VCO is designed using 3D EM simulation to achieve the higher Q-factor with the target thickness of 50 μm. Finally, the oscillation amplitude is decreased in comparison to the simulation results, the VCO operates correctly at 433 MHz.

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Nonlinearity analysis of 65nm 8bit Vernier Time-to-digital Converter

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Abstract **- This paper analyzes the nonlinearity of Time-to-Digital Converter (TDC) used in wireless bearing angle measure system by using Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) specification. Nonlinearity can be represented by the distance error, which indicates the uncertainty of the angle and position in this system. We investigate the distance error based on INL and cause of nonlinearity from the viewpoint of layout. We compare pre and post layout simulations of parasitic resistance in metal power line, underlying important layout points. Jitter and mismatch simulation are proposed for setting delay buffer size and TDC time resolution. Wire bonding inductance simulation is also considered for checking robust circuit operation. Verified TDC is an 8bit with a 18ps resolution. The measured DNL and INL were 0.8 LSB and -15 LSB. The simulated TDC is fabricated through Samsung 65nm chip process.**

Keywords**—Angle sensor, Localization, TDoA, Time to Digital Converter**

I. INTRODUCTION

Location information is widely used in indoor office space, public place, hospital and industries. Among various methods for obtaining indoor location information, ultra-wideband (UWB) technology is particularly popular [1,2]. UWB is a wireless communication method using unlicensed ultra-wideband of 3-10GHz. It can be implemented with low power and it is strong against multipath interferences because impulse waveform exists only for a short time in times series.

Fig.1 is a diagram of typical wireless system for bearing angle measure between transmitter and receiver. The receiver can be largely divided into two parts. One is the analog front-end (AFE) stage that amplifies the received small signal in Fig.2, and the other is the time-to-digital converter (TDC) stage that detects the time difference between two received signals START and STOP in Fig.4 [3,4].

At the analog front-end stage, the small waveform signal transmitted from Tx is amplified and the edge of the waveform is extracted by the envelope detector. Finally, comparator makes the arrival point of received signal into one square wave pulse.

The time difference of the received pulse occurs between two receivers Rx_1 and Rx_2. TDC detects time difference and outputs it as eight bits. the distance difference can be achieved by multiplying the time difference (TD) by the speed of light (c) in Fig.3 and interval of Rx1 and Rx2 is already known. Therefore, the bearing angle(θ) can be obtained by inverse cosine as (1). Finally, the TX (target) position can be determined by using intersection of several bearing angle information [5].

TDC is a core circuit block in this bearing angle measurement system. Since nonlinearity causes distortion in the distance difference, high linearity TDC is required for accurate bearing angle measurement.

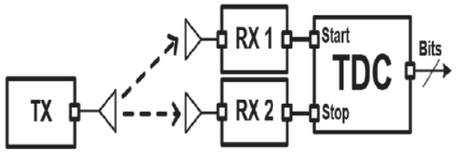

Fig.1. Bearing angle measurement system diagram

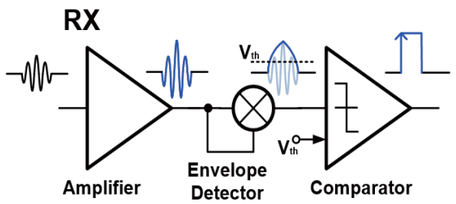

Fig.2. Analog front end receiver diagram

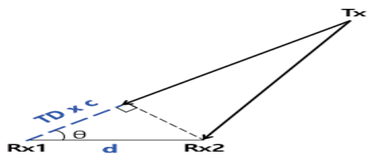

Fig.3. Principle of bearing angle measurement

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$$\theta = \cos^{-1}\left(\frac{TD \times c}{d}\right) \quad (1)$$

II. EXPERIMENTS

A. Concept of Vernier TDC

TDC converts time difference into digital bits and consists of a delay line and a thermometer to binary encoder as shown in Fig.4.

Vernier delay line measures the distance using the delay difference of the START and STOP delay buffer, thus achieving a finer resolution than a structure using one delay line known as flash TDC [6]. The delay difference between START and STOP line is implemented by changing the channel width, because the low to high (or high to low) transition time of inverter is proportional to the capacitance and is inversely proportional to VDD and channel width. The larger the channel width is, the more current flows and the faster delay can be realized.

The smaller the delay difference between START and STOP buffer, the finer time resolution can be achieved. However, the dynamic range is reduced. In other words, time resolution and dynamic range are inversely related.

Thermometer to binary encoder converts the 256 thermometer codes into digital bits. Thermometer codes can be obtained from the SR latch (arbiter, early-late detector), and the SR latch is connected to each delay buffer to determine which of the START and STOP signal has arrived first.

B. TDC simulation

Fig.5 is the simulation result of the timing diagram in Fig.4. The left side shows the simulation result where the START and STOP signals pass each delay buffer, and the right side shows the output of the corresponding SR latch.

At the first time, the START signal arrives before the STOP signal. In 7th delay buffer, the START signal is caught by the STOP signal. The SR latch output is 1 until the START and STOP signals are reversed. The SR latch outputs of the remaining delay buffers are all 0 after being caught. Just as the thermometer increases from the beginning to a certain temperature, the thermometer code increases from the beginning until the START and STOP signals are reversed.

The delay of the START buffer is 32ps, and the delay of the STOP buffer is 18ps. Therefore, the time resolution in simulation result is 14ps. In simulation testbench, START and STOP signals are put into the input with a 90ps time difference. Since the decimal of thermometer code is 6, TDC result estimate the START and STOP time difference to 84ps.

C. TDC measurement setting

Fig.6 shows TDC measurement setting. Data timing generator generates START and STOP signals with certain time difference and logic analyzer represents 8bit which is the TDC output value. We synchronized the data timing generator and logic analyzer and automated measure process using Labview.

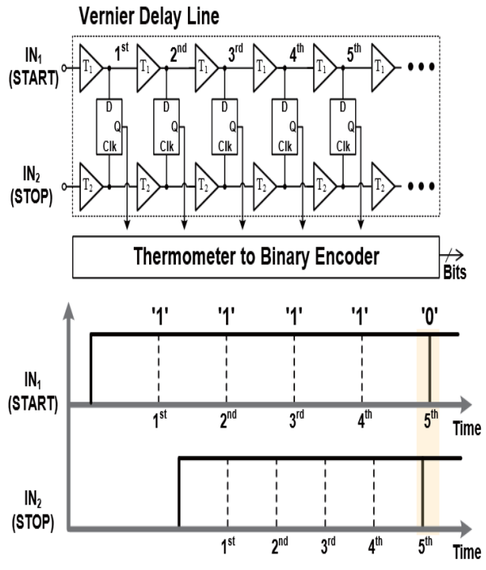


Fig.4 TDC block and timing diagram

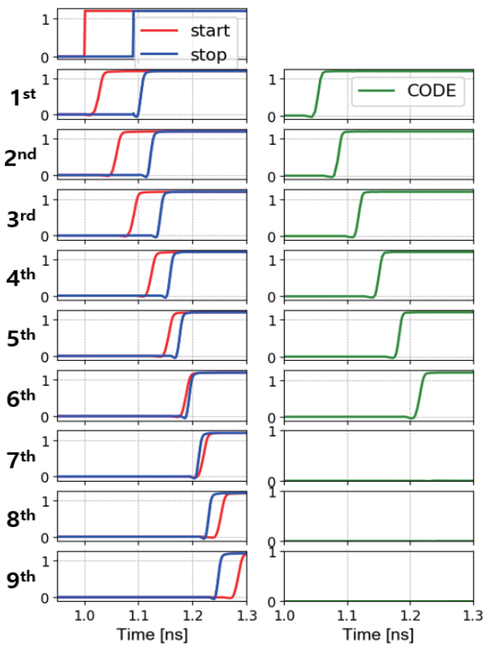


Fig.5. TDC timing simulation (a) START and STOP signal, (b) Thermometer code

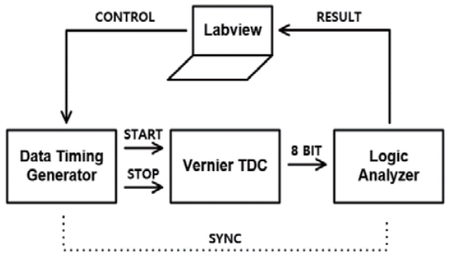
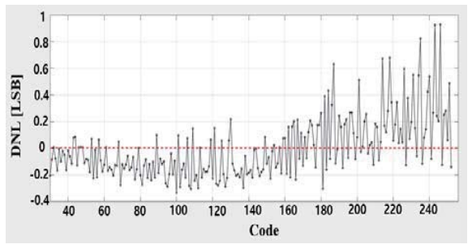
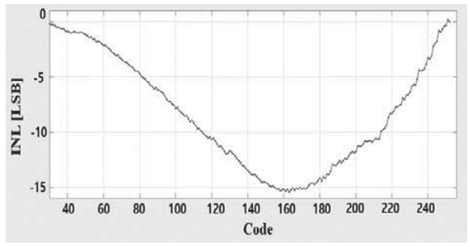


Fig.6. TDC measurement setting



(a) DNL



(b) INL

Fig.7. measured DNL & INL

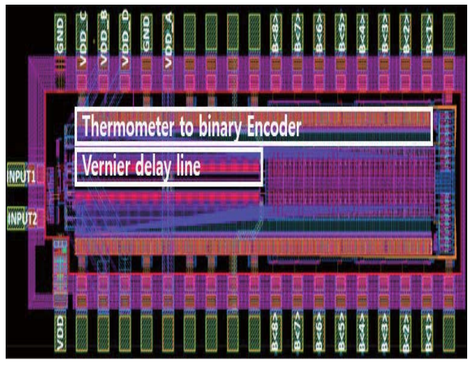


Fig.8. TDC Layout

III. RESULTS AND DISCUSSIONS

A. Linearity of TDC

The linearity of the TDC has been measured in terms of differential-non-linearity (DNL) and integral-non-linearity (INL). DNL is an error of each step from its average value (2), and INL is an error of the step position from its average value (3). In Fig.7 the measured DNL is -0.38 to 0.8 LSB and the INL is -15.3 to 0.2 LSB. The measured DNL sharply degrades after half the delay line.

$$DNL = \frac{measured\ \ delay - average\ \ delay}{average\ \ delay} \quad (2)$$

$$INL = \sum_{n=1}^{n=256} DNL_n \quad (3)$$

In TDC with 18ps resolution, 1 LSB error causes a 5.4 mm distance error, and -15 LSB error in INL finally results in 8 cm or more distance error.

B. TDC layout

Fig.8 shows the layout of the TDC, and it was confirmed that the parasitic resistance of the power line was the cause of the nonlinearity in Fig.7. We review several mistakes in the power line layout and verify this by pre and post layout simulation.

To reduce mismatch between transistors, which causes nonlinearity, the following points should be noted during layout [7]. Keep the channel width, number of fingers, and the channel length of the transistor as equal as possible and attach the delay line as closely as possible. If the delay line spacing is wide, parasitic capacitance and resistance are generated on the metal line interval between two delay buffers. Since the transistors are affected by temperature and other environmental changes such as noise, it is important to reduce such variations between each transistor by placing each delay buffer as tightly as possible. To densely attach the transistors, sharing the source (or drain) of two transistors or using the flatten function to remove unnecessary parts from

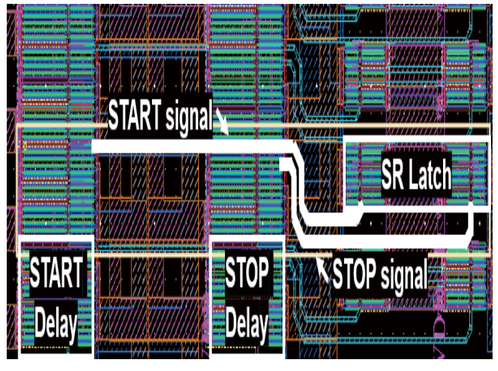


Fig.9 Asymmetry and non-uniform start and stop signal lines

the built-in transistor can be considered. It is also possible to arrange a dummy at the end of the delay line to suppress mismatch due to asymmetry at the end of the transistor.

The time delay is more influenced by the capacitance than by the resistance. Therefore, it is important to reduce the capacitance component of the transistor and signal line. The larger the number of transistor finger, the smaller the resistance of the transistor gate. However, as the number of transistor finger increases, the transistor area increases and causes a larger capacitance. Therefore, the number of fingers was two for the symmetry of the PMOS source, and the channel width per unit finger is changed depend on START or STOP line.

When the length of the metal line is constant and the width of the metal line in the layout increase, resistance in metal line decrease and the capacitance in metal line increase. Therefore, for the signal line connecting each delay buffer, the minimum metal width was used to reduce the effect of the capacitance rather than the resistance. Since the capacitance is inversely proportional to distance, using upper metal layer can reduce capacitance near signal line.

The most important point in TDC layout is the symmetry of the START and STOP delay lines. In Fig.9, START and STOP signal lines applied to the SR latch have different length and asymmetry. Timing offset can occur in different signal length and asymmetry. This problem can be solved by placing an SR latch between the START and STOP delay buffer or placing SR latch line parallel to the each START and STOP line side by side.

START, STOP, and SR latches were laid out in one delay unit. If certain circuit blocks are repeated in layout such as delay line, these repeated blocks can be bound to layout unit and it gives greater efficiency when the repeated blocks are modified.

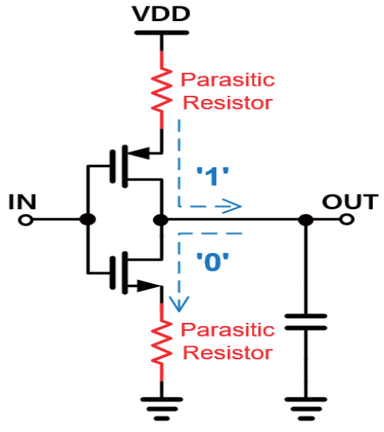


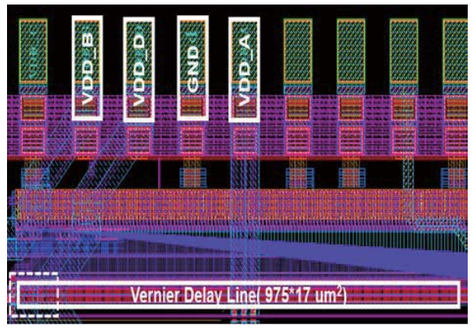
Fig.10. RC delay caused by parasitic resistance

C. Verification of Powerline Layout

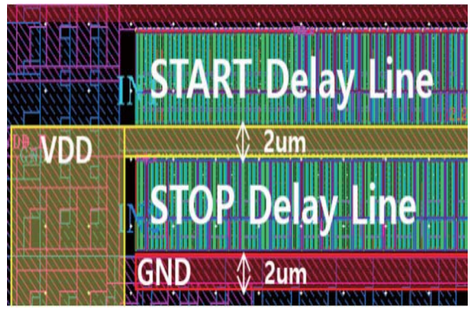
Mistakes in the power line layout cause parasitic resistance as shown in Fig.10. The parasitic resistance in the power and ground of the inverter delay cell causes RC delay with load cap during pull down or up state. RC delay makes serious distortion in uniform time delay. The parasitic resistance in the delay line is more problematic because the small parasitic resistances accumulate along the delay line and cause a greater adverse effect.

Fig.11 shows the failure examples of power line layout. In (a), VDD and GND supplied from the pad are not applied uniformly to the delay line but applied to only a specific portion. Since the only one metal layer is used, parasitic resistance can be induced. In (b), when the width of the metal line is narrower than the metal length, a large parasitic resistance occurs due to the sheet resistance.

The sheet resistance can be obtained by using the width (W) and the length (L) of the metal line. In Fig.11 (b), the length and width of the power line are 2000um and 2um respectively, and it has 1,000 sheet resistance. There are about 250 delay buffers in 8bit delay line, four sheet resistances occur between each delay buffer. Considering the one sheet resistance of the lowest metal layer, it can be assumed that about 400mΩ parasitic resistance occurs between each delay buffer.



(a)



(b)

Fig.11. Layout failure in power line (a) Problems of using one metal layer from pad and partially supplied power (b) problem of Narrow power line width

This can be simulated as shown in Fig.12 through the schematic model, and the result is shown in Fig.13. The cross function of Specter Calculator is used to extract the points that intersect with a specific threshold voltage value on the time axis and the time resolution, DNL and INL characteristics of the TDC can be obtained. In pre-layout simulation with parasitic resistance modeling, the DNL is -0.2 to 0.28 LSB and the INL is -17.5 to 1.9 LSB. In post-layout simulation, the DNL is -0.4 to 0.25 LSB and the INL is -27 to 1.4 LSB. The nonlinearity tends to be sharply decreased as the number of delay buffer increases. The accumulation of parasitic resistances causes this nonlinearity and shows a similar tendency when compared with the measured values in Fig.7.

Parasitic resistance can be minimized by using an upper metal layer which has small sheet resistance or by overlapping several metal layers and supplying power at both ends of the delay line which has the effect of making the sheet resistance look parallel.

The power line should be configured in a branch structure which provides a variety of ways for power, so that supplied power can be evenly distributed over long delay line.

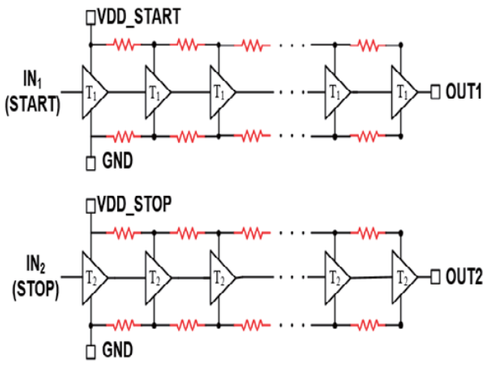
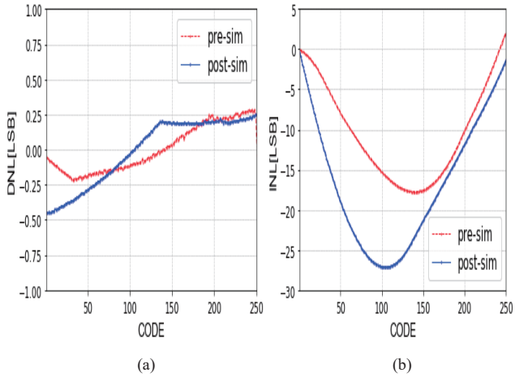


Fig.12. Schematic model with parasitic resistance



(a) (b)

Fig.13. (a) DNL and (b) INL of pre-layout simulation with resistor modeling and post-layout simulation

D. Wire-bonding inductance simulation

The following is a description of the simulation that should be additionally verified for TDC design. We will examine the wire bonding simulation if the chip is bonded on a PCB board and the jitter simulation to determine the resolution of the TDC.

For reliable TDC operation, bonding wire simulation on the substrate can be considered as shown Fig.14. The inductance of bonding, which occurs when a chip is mounted on a PCB board, is assumed to be approximately 1nH/mm [8]. Voltage ringing occurs by bonding as shown in Fig.15, which causes delay imbalance and damages TDC linearity. The voltage ringing is proportional to the inductance and current. Therefore, the rebound is much greater if a lot of current flows like an amplifier stage with a large gain or delay buffer with sudden transition.

The voltage ringing between VDD and GND can be reduced by giving the same rebound through the on-chip capacitor. In determining the capacitance of the on-chip capacitor, enough capacitance is considered to prevent noise, including ringing. However, an appropriate capacitance should be checked to prevent resonance with bonding inductance.

To reduce the inductance component, the GND pin uses down bonding using the metal ground plane under the chip. VDD and GND are placed side-by-side because the mutual inductance component is canceled because the direction of the current at the VDD and GND pads is opposite.

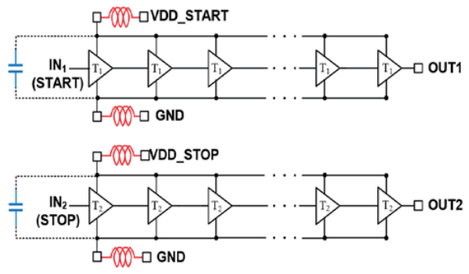


Fig.14. Schematic model with bonding wire inductance

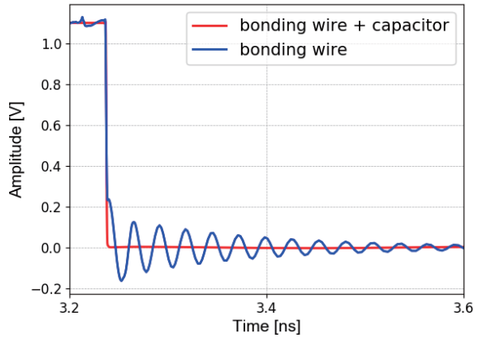


Fig.15. Ringing effect of bonding wire

E. Jitter and mismatch simulation

The causes of TDC nonlinearity are jitter and device mismatch. This variation can be seen from a global and local perspective. Global variations include process, supply voltage, and temperature, affecting overall TDC operation and producing offset or gain errors. Local variations include mismatch of threshold voltage, transconductance, and drain current, which leads to delay mismatch and directly affects DNL. These variations must be considered when determining the TDC time resolution, number of delays, and transistor size of the delay buffer [9,10].

The longer the length of the delay line, the larger the jitter. To guarantee integral error lower than 1 LSB error, the cumulative jitter of the entire delay line should be lower than the TDC time resolution. In other words, jitter limits the resolution of the TDC and the number of bits representing the TDC dynamic range.

Although there are many ways to measure jitter, the cycle-cycle jitter shows the difference between the period of the rising signal and previous period in Fig.16. Fig.17 shows the result of cycle-cycle jitter simulation in 200 cycles. The jitter of the 60th delay buffer is 1.7ps, and the 250th jitter is 3.5ps. If we observe more cycles, jitter distribution graph showing the Gaussian distribution. According to the simulation results, the TDC should aim at a time resolution of 3.5ps or more on 65nm 8bit TDC.

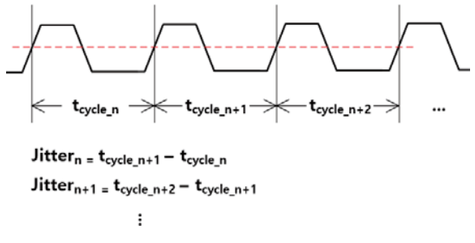


Fig.16. Concept of cycle-cycle jitter

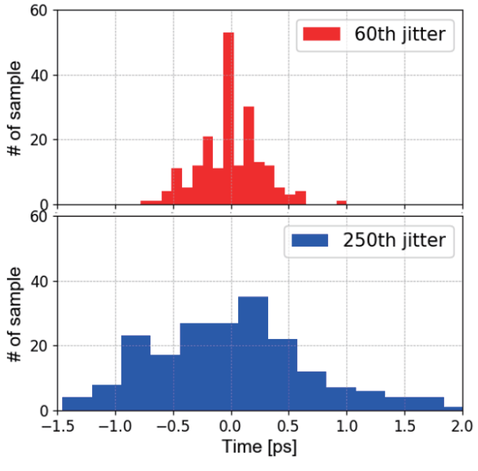


Fig.17 Cycle-cycle jitter distribution of 60th and 250th delay buffer

Fig.18 shows the result of a Monte-Carlo simulation with 200 samples showing the mismatch of the delay buffer. The average resolution of the delay buffer is about 16.2ps and has a standard deviation of 1.03ps. The 1.03ps mismatch variation is significantly lower than the TDC resolution of 18ps. The mismatch can be reduced if the L*W value is increased, however the power consumption increases accordingly. Considering this trade-off relationship, the size of the delay buffer can be determined according to the desired variation target [11].

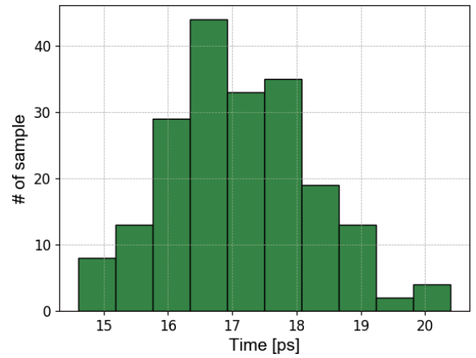


Fig.18. Delay buffer Monte-Carlo mismatch histogram

Most foundries provide a standard deviation of the threshold voltage or drain current mismatch according to the $\frac{1}{\sqrt{L \times W}}$ value with Monte-Carlo simulation. Circuit designer can refer to the results of these Monte Carlo simulations on the PDK to find the right transistor size for the desired standard deviation.

IV. CONCLUSION

The nonlinearity of the TDC measurement was analyzed from the viewpoint of layout, and the pre-layout simulation with the parasitic resistance modeling and the post-layout simulation were verified. We introduced jitter and monte carlo simulations that affect the nonlinearity of TDC, and we check the cycle-cycle jitter according to the number of delay and the delay buffer mismatch. The Cadence Virtuoso Specter and layout editor were used for simulation and layout, and the ADE XL for the monte carlo simulation.

This shows that there are many things to consider on the linear TDC operation, from setting TDC specification to the delay buffer and power line layout, including PCB board. By complementing the problems in this verification step, it is possible to improve the nonlinearity in the future TDC design and reduce the error of the bearing angle measurement. Low bearing angle error is expected to ensure accurate location information.

ACKNOWLEDGMENT

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Analysis of audio frequency ground integrity in TDMA smartphone system

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***Abstract* - In this paper, we designed a first-order discrete-time sigma-delta modulator to analyze the effects of ground noise coupling to audio circuits. The noise-coupling problem generally occurs in a time-division multiple access (TDMA) smartphone when its RF amplifier switch at 217 Hz to transmit signals for communication. We designed the modulator for operation at 3.3 V DC power and 6.144 MHz sampling frequency with 48 kHz baseband sampling frequency and 128 oversampling rate. With the designed modulator, we analyzed the output noise of the modulator when a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground node of the circuit. The modulator has shown a -50 dB 6 kHz noise power. Furthermore, we fabricated different designs of PCBs to mount the designed modulator and analyze the output noise of the modulator depending on PCB design. In the analysis, the amount of noise coupling reduced as the shared return current path between the modulator and a noise source on PCBs reduces.**

***Keywords*—Delta-sigma modulator, Ground noise, Time-division multiple access**

I. INTRODUCTION

In recent years, multifunction systems with small form factors have become a common requirement in the mobile device market. Because of this demand, various circuit blocks such as analog, digital, mixed mode, and RF blocks has been increasingly integrated into small systems, which is increasing the signal, power, and ground noise coupling between integrated circuits (ICs). Therefore, many researches are being conducted on signal and power integrity in integrated systems to solve signal and power integrity problems [1]-[9]. However, little research has been conducted on ground integrity (GI) [10], [11], and even those studies are mainly discussing GI in the high frequency domain [12]. This is because, even until recently, low frequency grounding is misunderstood as an equipotential point or plane that serves as a reference potential for circuits and systems.

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However, since the grounding structure of a handheld device has a finite size, it has finite impedance and can no longer be defined as equipotential points or planes. This will consist of a network of all interconnections that carry the current returning from the power-consuming circuits to the power supplier, and is termed the ground distribution network (GDN). Even at low frequencies, the small but finite impedance of GDN may cause ground noise coupling to low frequency targeting analog circuits and degrade the circuit performance. A common example is audio noise on smartphones using time-division multiple access (TDMA) communications [13]. Audio noise can have a direct impact on users and can have a significant impact on the reputations of smartphones.

The common audio noise in smartphones is bumblebee sound generated by the cellular phone's TDMA RF power

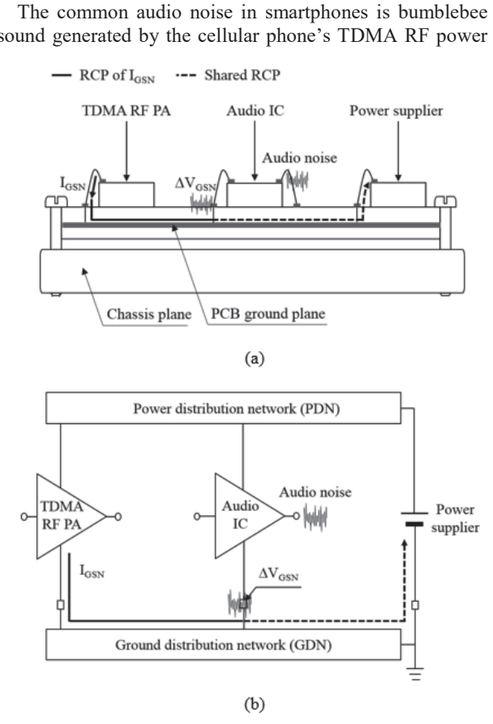

Fig. 1. Ground noise coupling mechanism between an audio IC and a TDMA PA in a smartphone. (a) Conceptual diagram (b) Block diagram.

amplifier (PA). Since 1990s, there have been many studies to solve this problem. However, the studies are focusing only on radio frequency interference or suppression of the noise through post processing the audio signal [14]-[18], and there is no research into ground noise coupling from RF PA to audio ICs.

Fig. 1 illustrates the mechanism by which ground noise is coupled and eventually leads the bumblebee noise to an audio IC in a TDMA smartphone. Ground noise coupling can occur while the operating current of the TDMA RF PA is flowing through the GDN of a smartphone that is composed of various components, such as the PCB plane and the chassis plane. TDMA RF PAs operate by switching at an audio frequency, which consumes a large switching current from the power supply during switching. For example, RF PAs in Global System for Mobile Communications (GSM), a typical example of a TDMA communication standard, consumes large switching currents of 1 to 3A (I_{GSN}) with a duty cycle of 12.5% at a frequency of 217 Hz [19]. This large current returns to the power supplier via the smartphone's GDN, and the path that this return current takes is called the return current path (RCP). When a large current flows through RCP, the non-zero impedance of the GDN causes the GDN voltage to fluctuate. At this time, when the audio IC is placed on the RCP of the RF PA and shares the RCP of the RF PA, the voltage of the ground node of the audio IC fluctuates to the TDMA frame rate. The ground voltage fluctuation (ΔV_{GSN}) degrades the performance of the audio IC and generates audible noise to the user.

Therefore, in this paper, we design a discrete-time sigma-delta modulator, the most suitable block in the data converters for audio application [20], to analyze the audio frequency ground noise coupling effect on audio circuits.

II. EXPERIMENTS

A. System level design of sigma-delta modulator

The first-order discrete-time modulator is designed and simulated with Virtuoso schematic editor from Cadence. Fig. 2 shows the overall block diagram of the designed circuit. The modulator comprises sampling circuits, an amplifier, a comparator and 1-bit DAC. The design and targeted performance of each block are discussed in later chapters. The maximum signal-to-noise (SNR) for n-order modulator can be expressed as (1), where N is the order and OSR is the over-sampling ratio of the modulator [21]. According to (1), the maximum SNR of the modulator becomes 66 dB.

$$SNR_{\max} = 10\log(\frac{3}{2}2^{2N}) + 10\log(\frac{3}{\pi^2}(OSR)^3) \quad (1)$$

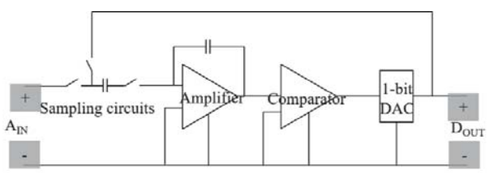

Fig. 2. Block diagram of the designed first-order discrete-time sigma delta modulator

B. Design of a switched capacitor integrator

The two switched capacitors sample the internal thermal noise as well as the input signal. Due to the oversampling operation of the modulator, the frequency bandwidth of the sampled noise power is spread and the noise power of the baseband is adjusted to a value divided by oversampling, and (2) expresses this value. With a 4dB additional noise margin and a target SNR of 70dB, the minimum required capacitor can be found \ as in (3). We set the capacitor value as 1 pF.

$$P_{noise} = \frac{2KT}{C \times OSR} \quad (2)$$

$$\sqrt{P_{noise}} \le -70dB \quad (3)$$

C. Design of a two-phase non-overlapping clock generator

A switched capacitor circuit requires two-phase non-overlapping clocks to reduce the signal-dependent charge injection. Fig. 3 shows the block diagram of the designed clock generator. The two cross-coupled NAND gates with inverters generate two clock signals with opposite phases, CLK1 and CLK2. A series of two inverters consist a single delay line, and it delays the two clock signals and generate CLK1D and CLK2D. The delay time is determined 32 ns, one-fifth of the input clock signal. Table I shows the transistor parameters of the designed clock generator.

D. Design of an operational amplifier

A folded cascode scheme is chosen to keep the output range as broad as possible. A differential input and single-ended output folded cascode operational amplifier is designed to have a DC gain higher than 60 dB, a gain-bandwidth greater than 24.6 MHz, which is 4 times the sampling frequency, and slew rate greater than seven times the reference frequency multiplied by a reference voltage of 1.65V, for reliability of the entire modulator. Fig. 4 shows

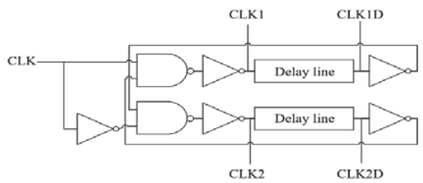

Fig. 3. Block diagram of the designed clock generator

TABLE I.
Transistor parameters of the designed two-phase non-overlapping clock generator

Transistor name	Transistor size W/L[um/um]
PMOS of inverters	0.595/0.35
NMOS of inverters	0.220/0.35
PMOS of delay lines	0.595/4.9
NMOS of delay lines	0.220/4.9
PMOS of NAND	1.015/0.35
NMOS of NAND	0.440/0.35

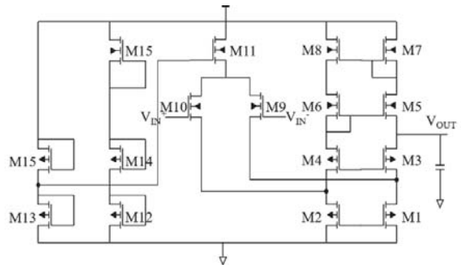

Fig. 4. Schematics of the designed folded cascode operational amplifier

TABLE II
Transistor parameters of the designed folded cascode operational amplifier

Transistor name	Transistor size W/L[um/um]
M1 ~ M10	150/0.7
M11, M15	3/0.7
M12 ~ M15	50/0.7

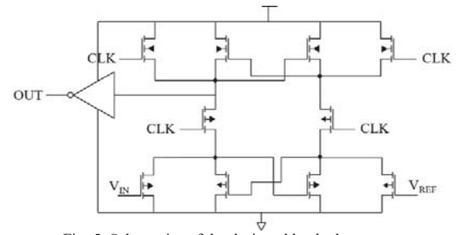

Fig. 5. Schematics of the designed latched comparator.

TABLE III
Transistor parameters of the designed latched comparator

Transistor name	Transistor size W/L[um/um]
PMOS of the comparator	0.595/0.35
NMOS of the comparator	0.220/0.35

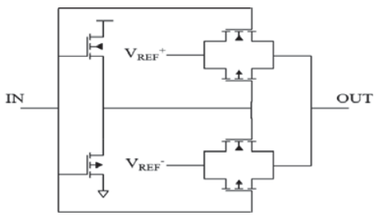

Fig. 6. Schematics of the designed 1-bit DAC.

TABLE IV
Transistor parameters of the designed 1-bit DAC

Transistor name	Transistor size W/L[um/um]
PMOS of the comparator	0.595/0.35
NMOS of the comparator	0.220/0.35

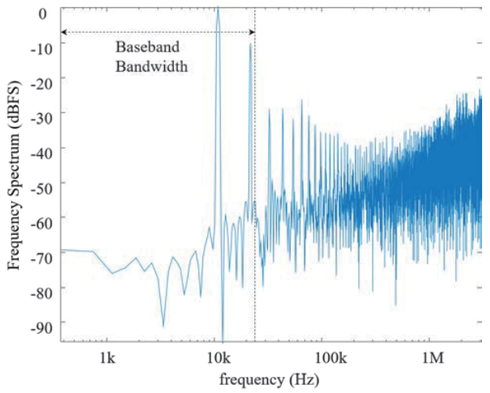

Fig. 7. Simulated frequency spectrum of the designed sigma delta modulator

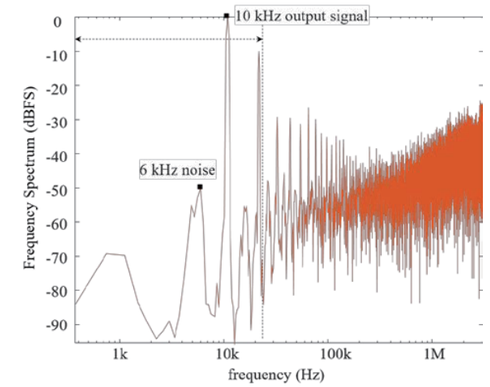

Fig. 8. Simulated frequency spectrum of the designed sigma delta modulator with ground noise

schematics of the designed folded cascode operational amplifier. Table II shows the transistor parameters of the circuit.

E. Design of a comparator

A latched comparator is designed for high-speed operation. An analog input is converted into VDD and GND after being compared to the reference voltage. Fig. 5 shows the schematics of the designed latched comparator. Table III shows the transistor parameters of the circuit.

F. Design of 1-bit digital-to-analog converter

A 1-bit digital-to-analog converter (DAC) converts digital to analog signal and feeds back to the integrator. It has two reference voltages, 1 V and 2.3 V. If the input data is 0, the output becomes 1 V, and if the input data is 1, the output becomes 2.3 V. Fig. 6 shows the schematics of the designed 1-bit DAC. Table IV shows the transistor parameters of the circuit.

III. RESULTS AND DISCUSSIONS

A. Analysis of audio frequency ground noise effect on the first-order discrete-time sigma-delta modulator

After completing the design, the first-order discrete-time sigma-delta modulator is simulated in the time-domain using a Virtuoso Analog Environment Simulator from Cadence. A sinusoidal input signal with a 0.7 V amplitude and a 10 kHz frequency is applied. The simulated time-domain waveform is processed into the frequency domain with FFT. Before the FFT, the waveform is Hanning-windowed to limit the spectrum leakage. The spectrum is scaled to the input signal frequency. The frequency spectrum is shown in Fig. 7. The spectrum shows the baseband noise successfully spread to over-sampled frequency range. The modulator has shown a 55.7 dB SNR. The harmonic components of the output signal is excluded in the calculation of SNR.

To check whether audio frequency ground noise coupling affects the performance of the designed circuit, a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground of the circuit. Fig. 8 shows its frequency spectrum. The modulator has shown a -50 dB 6 kHz noise power.

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B. PCB and Ground Designs for TDMA Smartphones

Fig. 9 shows two PCB designs for audio frequency GI analysis. The designed modulator and a noise source are placed on the PCBs. The ground noise is analyzed in simulation level by using power distribution network model of designed PCBs and circuit models. The noise source is an ideal current source which draws peak-to-peak 3 A of current at 217 Hz. The two PCBs differ the positions of the modulator and the noise source. On the first PCB named CASE A, the components are placed in the order of a noise source, a modulator and a power supply. On second PCB named CASE C, the components are placed in the order of a modulator, a power supply and a noise source. The modulator and noise source are placed radially from the power supply.

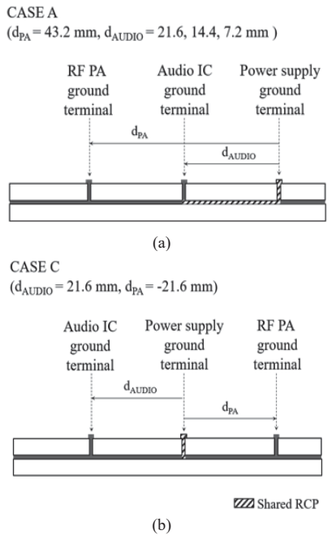

Fig. 9. Two PCB designs for audio frequency GI analysis.

Fig. 10 shows the frequency spectrum of the output of the designed modulators each in PCB CASE A and CASE C. In the ground design of CASE A, the location of the modulator determines the shared RCP as shown in Fig. 9 (a). The length of the shared RCP determines the ground noise coupled at the modulator. In the ground design of CASE C, the modulator and the noise source nearly do not share RCP, and therefore, the ground noise coupled at the modulator is much less than that in the PCB CASE A. Because the ground noise coupled at the modulator of CASE C is smaller than that of CASE A, the output noise of the modulator of CASE C is smaller than that of CASE A as shown in Fig. 10. The modulator of CASE C shows better SNR than CASE A.

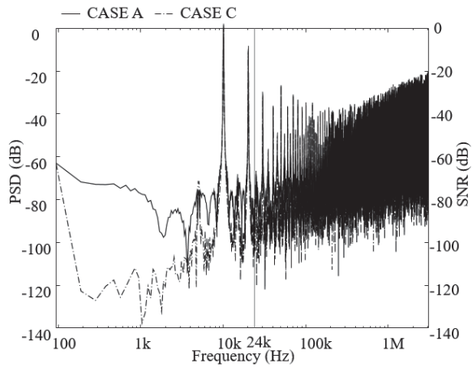

Fig. 10. Two PCB designs for audio frequency GI analysis.

IV. CONCLUSION

In this paper, we designed and simulated a first-order discrete-time sigma-delta modulator circuits with Virtuoso Schematic Editor and Analog Environment Simulator from Cadence to analyze audio frequency ground noise coupling effect on audio. The designed modulator operates at 3.3 V DC power and a 6.144 MHz sampling frequency with a 48 kHz baseband sampling frequency and a 128 over-sampling ratio. The spectrum shows the baseband noise successfully spread to over-sampled frequency range, and the modulator has shown a 55.7 dB SNR. When a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground of the circuit, the modulator has shown a -50 dB 6 kHz noise power. The designed modulator is further analyzed by being simulated with PCB power and ground network model, a supply, and a noise source. The amount of noise coupling reduces as the shared RCP between the modulator and a noise source reduces. The result clearly shows that the grounding structure of a system should be carefully designed to prevent degradation of the audio IC in systems that cause audio-frequency ground noise coupling.

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Low Noise, Low Power 5-Channel Sonar Signal Conditioning Receiver with 1.5 MS/s - 12.5 MS/s 16-bit Sigma-Delta ADC for Ocean Acoustic Measurements

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***Abstract* - This paper presents a design of 5-channel receiver for ocean acoustic measurement in a very noisy environment. When measuring the distance in the ocean with the sonar signal, the input signal level to the receiver is drastically changed depending on the distance between the transmitter and objects. Thus, the receiver with low sensitivity and wide dynamic range is proposed in this work. In order to minimize the Input-Referred (IR) noise for low sensitivity of the receiver, low noise pre-amplifier is proposed and implemented achieving the noise of 29.6 nV/√Hz at 50 kHz. In addition, Sigma-Delta Analog-to-Digital Converter (SD ADC) with variable sampling rates is proposed by using clock splitting technique in the Sigma-Delta Modulator (SDM) core. Also, the decimation factor of the digital filter placed after the SDM in the SD ADC can be controlled to reduce the power consumption. Thanks to these techniques in the SD ADC, we can implement the reconfigurable sampling rates from 1.5 MS/s to 12.5 MS/s with low power consumption. In order to overcome the limitation of the number of pins for multi-channel application, Parallel-to-Serial (P2S) interface is proposed and designed in the receiver. The 5-channel receiver in this paper is implemented in 0.18μm CMOS process and die area is 14.44 mm2. The total power consumption of this chip is 46.8 mW under the supply voltage of 2.4 V. The measured sensitivity and dynamic range are -100 dBV and 100 dB, respectively. The measured SNDR at the output of the SD ADC is 82.02 dB when the input signal frequency and sampling frequency are 7 kHz and 6.25 Msps, respectively. The maximum phase error between 5 channels is measured to be ± 0.8 °.**

***Keywords*— Multi-channel, Receiver, Sonar sensor**

I. INTRODUCTION

Sonar system has been actively studied from various perspectives such as sensor modeling, signal processing of the ultrasonic signal. Also, the signal processing circuits such as Analog-to-Digital Converter (ADC) have been actively researched. [1-7] The recent trends are more focusing on the sensor array than a single sonar sensor. Sensor array can have advantages in terms of reducing area and lowering costs accordingly. [8-9] In order to process signal from sensor array, multi-channel receiver is essential. Figure 1 shows the ocean acoustic measurement environment. The environment has many noise sources and the receiver is exposed to those noise sources. Many noise sources in the ocean environment degrade the performance of the receiver. In Figure 1, the distance between Object1 and Receiving Equipment is larger than d2, distance between Object2 and Receiving equipment. Especially, when receiving signal from the farther object, noise sources reduce the SNR performance much more. Thus, this measurement environment shown in Figure 1 requires the receiver with the low noise and Input-Referred (IR) noise should be lowered to improve the Signal-to-Noise Ratio (SNR) and sensitivity of the receiver. On the other hand, as the distance between the object and Receiving equipment is closer, the input signal level of the receiver will be increased, which can cause the nonlinear harmonic distortion in the receiver. For processing small and large input signal level depending on the distance, high dynamic range and Automatic Gain Control (AGC) is necessary.

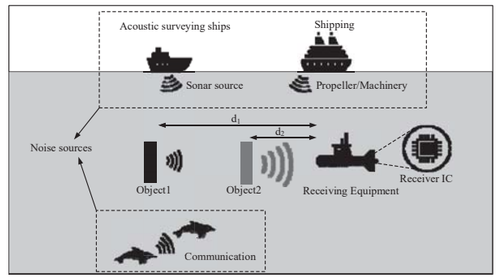

Figure 1. Environment of measuring distance on the ocean

In this paper, we propose receiver with the low noise pre-amplifier and wide dynamic range for sonar sensors. The pre-amplifier in the proposed receiver has the low IR noise of 29.6 nV / √Hz at 50 kHz. Also, it can apply the DC bias point of 1.2 V to the external sonar sensors since they do not have the DC bias voltage needed for proper MOSFET

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operation. A receiver takes the signal from each sensor of the sensor array and processes it in the single channel. For sensor array, the technique integrating separate multichannel circuits for signal processing is essential. The proposed receiver also includes the Sigma-Delta ADC (SD ADC) with reconfigurable decimation factor, and sampling frequency can be varied with oversampling ratio (OSR). In this paper, we propose and design 5-channel low noise receiver with SD ADC with reconfigurable sampling rate of 1.5 MS/s – 12.5 MS/s.

II. PROPOSED RECEIVER

The system specification of the proposed receiver is shown in Table 1. Input voltage amplitude range is from -100 dBV to -29 dBV. This large range requires the large dynamic gain range in the receiver. This system requires the IR noise less than -150 dBV / √Hz. When multiple input signals go to the proposed receiver in the same phase, the output of that is less than 1 degree. Parallel-to-Serial (P2S) is essential due to the number of channel. With P2S circuit, reducing the number of data output pins is available. Figure 2 shows the equivalent circuit of the unit sensor of the sensor array. Input signal is modeled as voltage source and sensor can be modeled with resistor and capacitor.

The block diagram of the proposed receiver is shown in Figure 3. Each channel of the proposed receiver consists of pre-amplifier, variable gain amplifier (VGA), band pass filter (BPF), SD ADC and P2S circuits into one chip. When differential signal comes from the sensor array, each signal goes into each channel of the 5-channel receiver IC.

TABLE I. System specification

Parameter	Specification
Input voltage amplitude(dBV)	-100 ~ -29
Supply voltage (V)	2.4
The number of Channel	5(in 3.8 mm * 3.8 mm size)
Dynamic range(dB)	20 ~ 100
Resolution(bit)	16
Sampling frequency (Hz)	> 2.5 M
IR Noise(dBV / √Hz)	< -150
Phase error between channels(degree)	< ± 1

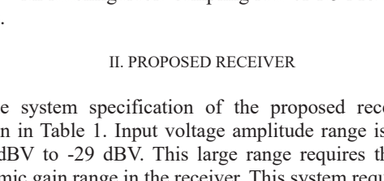


Figure 2. Equivalent circuit of sensor on the input

The receiver is designed to minimize the noise maximizing the SNR with the high resolution SD ADC. Each MOSFET in the pre-amplifier of input stage is designed to be large to reduce the flicker noise. Depending on input signal level, VGA can adjust its gain to make input signal level of the ADC to the Full Scale (FS). BPF has the function of DC offset cancellation and reducing noise at the high frequency. SD ADC is implemented to obtain high resolution for the low sensitivity sonar sensor application by applying variable oversampling and chopping scheme in the amplifier. In addition, Sigma-Delta Modulator (SDM) in the SD ADC uses clock splitting technique and adopts digital filter with adjustable decimation factor for reconfigurable sampling frequency. Parallel-to-Serial (P2S) interface is integrated for multichannel receiver due to the limitation of the pins. SPI Controller is designed to control gain of IC depending on the input signal level.

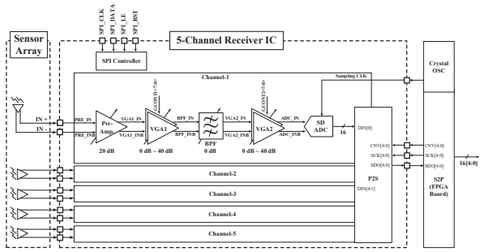


Figure 3. The block diagram of the proposed 5-Channel Receiver IC

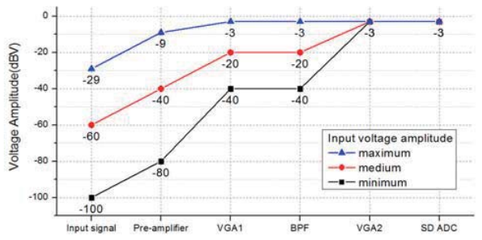


Figure 4. System budget of the proposed receiver with respect to input signal amplitude

III. PROPOSED RECEIVER

A. Pre-amplifier

Since the ocean measurement environment requires low noise receiver due to many noise sources around it, one of the most important issues is to increase the signal-to-noise ratio (SNR) in the high resolution receiver. In order to increase the SNR, lowering noise level of the input signal to ADC is necessary. In the receiver in this paper, the pre-amplifier is designed to lower the noise power for high SNR at the output of the ADC. In general, IR noise of the pre-amplifier dominantly determines noise performance of the whole receiver. Therefore, to design the receiver having low noise, it is important to minimize IR noise of the pre-amplifier. In addition, pre-amplifier plays the role to suppress noise from VGA1 and BPF by providing the gain of 20 dB. The schematic of pre-amplifier is shown in Figure 5. Since the input DC voltage level of the application is not determined by the external Sensor, we design the pre-amplifier for shifting the DC level to 1.2 V in order to meet the bias condition of VGA1. The size of input MOSFET is optimized so that input referred noise be minimized. With this pre-amplifier, IR noise of the proposed receiver is simulated to be 29.6 nV / √Hz at 50 kHz.

Figure 6 shows the OP-Amp used in the pre-amplifier. Two-Stage Op-Amp with PMOS inputs is designed. Miller compensation with R and C is applied to guarantee the Phase Margin (PM) of 60 °. With the OP-Amp, the noise contribution of all the devices in the Op-Amp is analyzed as shown in Figure 7. In Figure 7, IR noise is lowered by optimizing MOSFET size and bias current. Before optimization, flicker noises of the input MOSFETs are dominant factor. Thus, we reduce their noise to almost 1/10 than those before optimization. Figure 8 presents the IR noise simulation result of the pre-amplifier showing the noise of 28 nV / √Hz at 50 kHz.

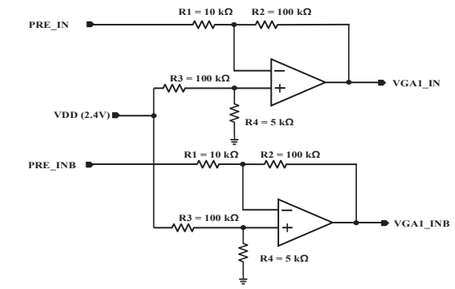


Figure 5. Schematic of pre-amplifier

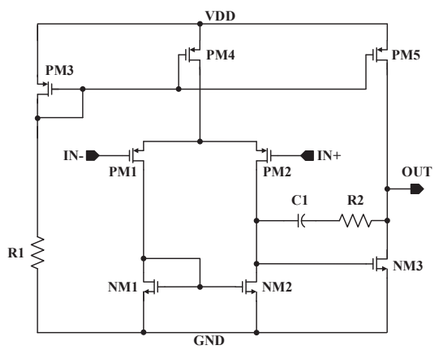


Figure 6. Schematic of OP-Amp in the pre-amplifier

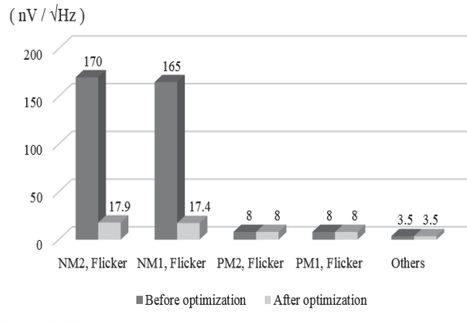


Figure 7. IR noise comparison before optimization and after optimization

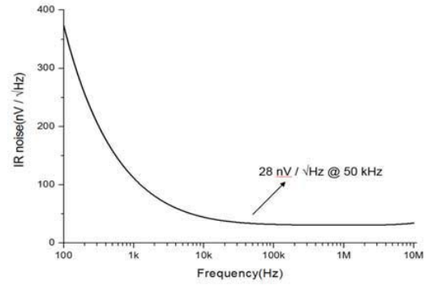


Figure 8. Noise simulation result of pre-amplifier

B. Variable Gain Amplifier

For high resolution of the SD ADC, precise gain control is needed. The proposed receiver has the function of controlling the gain with 1-dB step. As shown in Figure 2, input signal goes through the VGA1, BPF, and VGA2, sequentially. The maximum gains of VGA1 and VGA2 are 40 dB, respectively. Figure 9 shows the schematic of VGA1 and VGA2 uses exactly same structure as VGA1. Besides, they are designed to be adjustable using a resistive feedback structure by 1-dB step control depending on input signal level. As the signal amplitude is larger, lower gain is provided for meeting the input voltage range of SD ADC. AC simulation result of VGA1 is shown in Figure 10. Total gain is from 0 dB to 40 dB and it provides variable gain step of 1-dB.

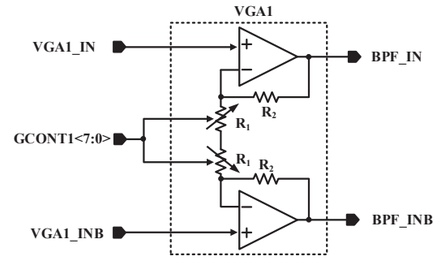


Figure 9. Schematic of VGA1

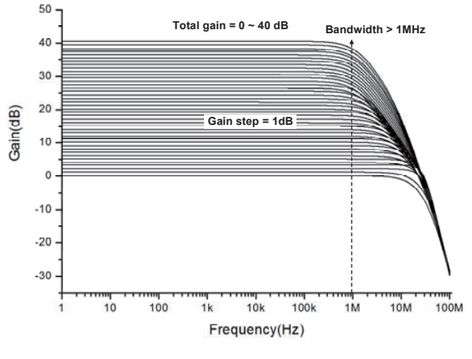


Figure 10. AC simulation result of VGA1

C. Band Pass Filter

For cancelling the dc offset and suppressing noise at high frequency, Active-RC Band-Pass Filter (BPF) is designed in the proposed receiver. The schematic of BPF is presented in Figure 11. BPF is designed as 4th order, Chebyshev type. In terms of noise performance, VGA1 is positioned right after pre-amplifier because the noise characteristic of BPF is worse than those of the VGA1 and VGA2. Thus, the noise from BPF can be attenuated by the gain of pre-amplifier and VGA1.

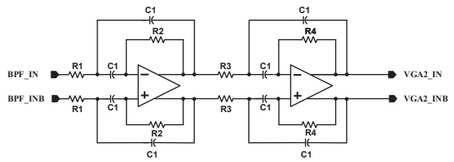


Figure 11. Schematic of Band-Pass Filter (BPF)

D. Sigma-Delta ADC

Figure 12 is the proposed simplified SD ADC designed in this work. SD ADC consists of SDM and digital filter. In this application, we designed high resolution for the ocean measurement environment. In order to reduce the noise, SDM is designed to push out the noise to higher frequency which can be filtered by the following digital filter. Decimation filter is designed to control the decimation factor to lower the current consumption.

Figure 13 shows the block diagram of SDM. The second order discrete type SDM with Cascaded Integrator Feed-Back (CIFB) structure is implemented. Two integrators and 1-bit Quantizer is used.

The schematic of the SDM is shown in Figure 14. The sampling operation is performed in the sampling capacitors as shown in the Figure 14. The differential signals (V_{IN} and V_{INB}) come from the analog circuits including pre-amplifier, VGA and BPF. Input differential range of SDM is 2 V_{pp} and common mode level is 1.2 V. In the first integrator, the coefficient value is determined by the ratio of the sampling capacitor ($C_I/4$) and integration capacitor (C_I).

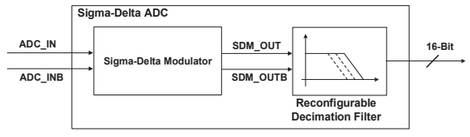


Figure 12. Simplified block diagram of the proposed SD ADC

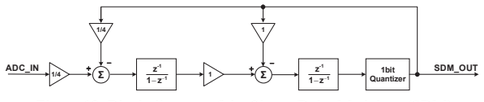


Figure 13. Block diagram of the Sigma-Delta Modulator(SDM)

Figure 15 shows the schematic of OP-Amp used in SDM shown in Figure 14. The amplifier has gain-boosted Folded-Cascode structure. In order to reduce the flicker noise at the

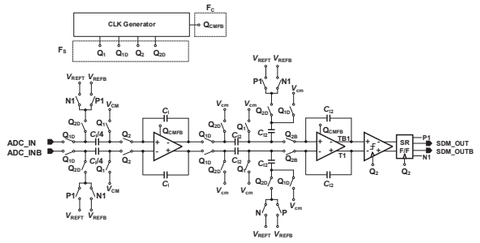


Figure 14. schematic of the designed Sigma-Delta Modulator(SDM)

low frequency, the chopping scheme is applied. The OP-Amp use the Chopper PMOS, Chopper NMOS, and Chopper_IN with their control switches. The chopper pushes out the noise in the signal band to higher frequency. The chopper circuits basically operate based on the clock. The clock is generated by CLK Generator shown in Figure 15. Besides, the common mode feedback (CMFB) circuit is designed to maintain the output common mode voltage level. Since in the high gain amplifier, the circuit that keeps the output bias voltage is essential. In order to use high sampling frequency, CMFB clock should be separated from sampling clock. If CMFB clock is same with sampling clock, the gain of OP-Amp used in the SDM is reduced. In that case, resolution of SD ADC is also degraded. In this paper, we split CMFB clock from the sampling clock.

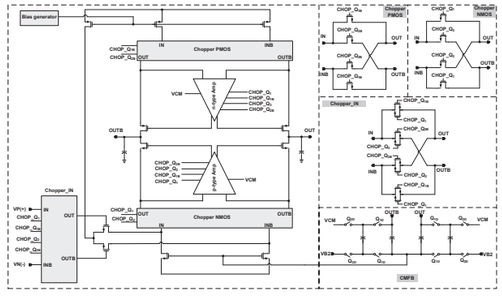


Figure 15. Schematic of OP-Amp in the proposed SDM

Figure 16 shows the schematic of the clock generator of the SDM. The circuit generates clock signals Q_1, Q_{1D}, Q_2, and Q_{2D}. Also, inverted signals, Q_{1B}, Q_{1DB}, Q_{2B}, and Q_{2DB} from Q_1, Q_{1D}, Q_2 and Q_{2D}, are also generated through clock generator circuit. Figure 17 shows the clock signal waveforms generated by the clock generator circuit. Since Q_{1B}, Q_{1DB}, Q_{2B}, and Q_{2DB} are inverted form of Q_1, Q_{1D}, Q_2, and Q_{2D} signals. Q_1 and Q_2 signals are non- overlapped clocks as well as Q_{1D} and Q_{2D} signals.

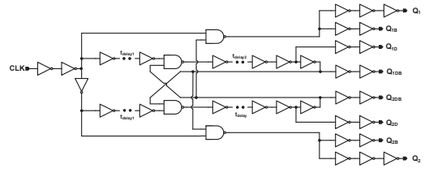


Figure 16. Structure of the non-overlap two-phase clock generator

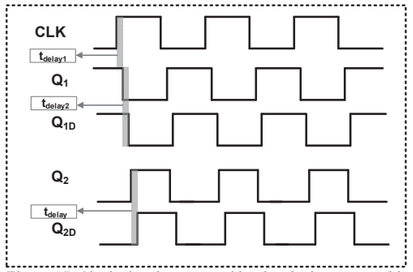


Figure 17. Clock signals generated by the clock generator block

Figure 18 shows the structure of the proposed comparator. Since the power consumption is smaller than that of the static type, a dynamic type of comparator is designed. The differential output of the second integrator is connected to the INP and INN inputs of the comparator. The outputs of the comparator (SDM_OUT and SDM_OUTB) are determined by latches. Q_1 and Q_2 clock signals control the comparator clocking and the P1 and N1 signals are determined to control some switches in the SDM as shown in Figure 14.

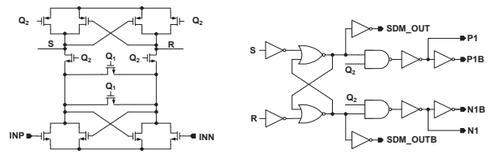


Figure 18. Structure of the comparator

The proposed SD ADC consists of mainly SDM and digital filter. A digital filter has a role as cutting the noise on the high frequency band. The main function of the SDM is pushing out the noise to higher frequency than input signal frequency. And the order of the SDM determine the slope of the output noise shaping. The higher order SDM makes the output noise shaping more sharp on the frequency domain. For applying digital filter to the high order SDM, the digital filter should have high power, large area with cascaded structure. In the conventional design, decimation factor of the digital filter is dependent value on the OSR of the SDM. In this paper, digital filter with controllable decimation factor and controller is presented.

The SDM in this paper has 2nd order configuration as it is shown in Figure 12. For small area, sinc3 type filter is adopted for the proposed receiver. The block diagram of the proposed decimation filter is shown in Figure 19. It includes the Integrators and Comb filters with cascaded structure. The controller is used to control decimation factor. Using the CONTROLLER block, the register width and proper clocking within the filter stages are selected. Integrator clock is same as sampling clock (Fs) of the SDM whereas Comb can be operated with sampling clock divided by decimation ratio (Fs/D). This process helps decimation filter to reduce the power dissipation at Comb stage of the CIC filter. This clock is controlled by the CONTROLLER block according to the requirements of the decimation ratio. Register size can be varied through the CONTROLLER when changing decimation ratio. This is because integration and differentiation (Comb) require different register sizes when the decimation ratio changes. Register sizes are proportional to the decimation ratio. They are related by the following equation (1)

$$\text{World Length} = L\,(\log_2 D \cdot M) + W_{in} \qquad (1)$$

In this Equation (1), L is the number of stages in CIC filter. D is decimation factor with variable features, M is the number of delays and W_{in} is the input word length. Inside the integrator and comb filter, register size is controlled for the specific decimation ratio. Output of the filter has the 14 Most Significant Bits (MSB) selected from single wide register (main register).

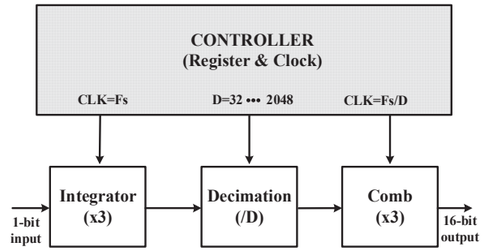


Figure 19. Proposed block diagram of the decimation filter

Figure 20 shows the CONTROLLER which is used in decimation filter. The CONTROLLER includes the Clock Controller and Register Controller. Clock Controller provides the clocks for needed in the Comb filter, Integrator, and CIC filter. Equation (1) presents how register size is calculated and maximum size for D=2048. This will be the main register used by all filters. The controller will select MSB 14-bits from this register based on the decimation factor and will discard the remaining bits.

Also, the controller operates by sampling clock sample with that used in SDM. The necessary clocks for the integrator, comb and other control blocks are generated based on this sampling clock. D_CNTRL (4 bits) is used to select among various options of the decimation factor (32, 64, ..., 2048). The register controller block selects 14 MSBs from the main register and assigns them to the output by dropping the LSB.

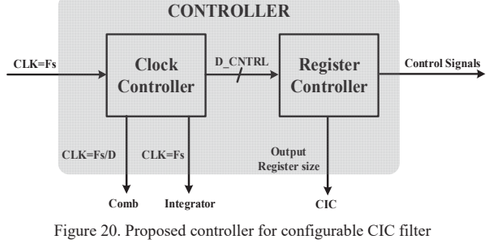


Figure 20. Proposed controller for configurable CIC filter

E. P2S-S2P Interface

The proposed receiver implemented the serial interface circuit inside the IC. For pin-constrained application, P2S interface is necessary to send the data. [10] Figure 21 shows the block diagram of the P2S-S2P used in the proposed receiver. SYNC is synchronization signal, DIN means parallel data input and SDO is serial data output. P2S interface is designed inside the IC and S2P is in the FPGA board. ADC output is the parallel data, then the data goes to P2S interface and its output is serial form data. This P2S-S2P interface has two synchronization modes which are high throughput mode (HTM) and highly synchronized mode (HSM).

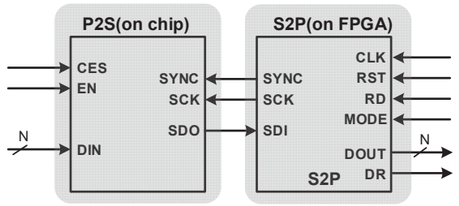
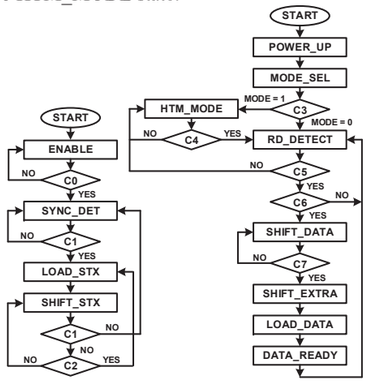


Figure 21. P2S and S2P block diagram

In HTM, SYNC is pulled down and MODE signal is high. After that, P2S receives data from DIN and at the active edge of clock SCK, transmits it to SDO. SDO is transmitted in serial from MSB to LSB. In this mode, no overhead bits or extra clock cycles exist. At the time that the communication between P2S and S2P interface starts, P2S and S2P are synchronized at the negative edge of SYNC once. Firstly, MODE is pulled down and the mode HSM that P2S and S2P synchronize is enabled after all serial data is sent and received. Only when RD is high, P2S takes sample and transmits it to P2S. This mode is determined due to features of the proposed receiver which does not need continuous data. For the high performance P2S interface operation, f_{sck} (the serial clock frequency) is necessary. It is given in Equation (2).

$$f_{SCK} \geq F_{ADC} \times N \qquad (2)$$

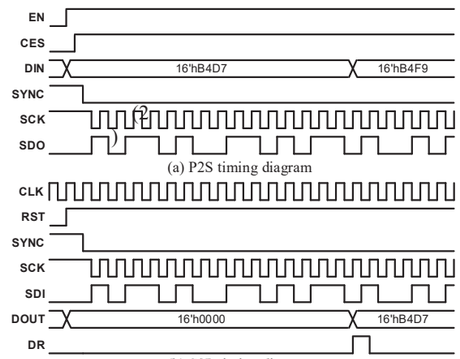
In the Equation (2), N is the resolution and F_{ADC} is the sampling frequency of ADC, respectively. The P2S and S2P interface is synchronous finite state machine (FSM) model based design. Figure 22 shows the FSM flow chart for P2S and S2P. Timing diagram of each data is presented in Figure 23. The P2S circuit in this paper is enabled only when EN from control logic is pulled high. For P2S, the positive or negative active edges can be selected by clock edge select signal (CES). On POWER_UP stage, P2S controller moves to ENABLE. Then, the controller goes to SYNC_DET state and hold on for SYNC negative edge. When SYNC is released from S2P, the P2S controller jumps to the next stage, LOAD_STX. In LOAD_STX state, the parallel data DIN is loaded from the internal register transmitting the MSB to SDO. Then, in SHIFT_STX state, if SYNC is held low, the internal register value is shifted one bit to the left and the MSB of the register is transferred to the SDO pin remaining for N-1 SCK clock cycles. In case of HTM enabled, the controller moves state to LOAD_STX for taking SD ADC sample. The controller goes back to LOAD_STX state for receiving next ADC sample. Or, it jumps back to SYNC_DET for resynchronization in case of HSM. The FSM for S2P controller is presented in Fig. 15(b). Data stays in POWER_UP state after reset for one clock cycle. Then it goes to MODE_SEL state and MODE signal from control logic select the mode HTM or HSM. When MODE is asserted, HSM is enabled and the controller get direction to HTM_MODE state.



(a) P2S FSM (b) S2P FSM

Figure 22. Serial interface FSM diagram

In this state, SYNC is pulled low for synchronization between S2P and P2S. Also, S2P enables the SCLK clock and starts to receive serial data at SDI from S2P. The bits are shifted in serial inside the internal register. There is a counter for checking the number of bits received from P2S.



(a) P2S timing diagram

(b) S2P timing diagram

Figure 23. Serial interface timing diagram

If N bits are received, N-bit DOUT load the register bits. Additionally, in order to announce the reception of the data to control logic, RD is changed to pulled high for one clock. In case that MODE is deasserted to select HSM during HTM, the controller goes to RF_DETECT state after processing the

data. When HSM is enabled, the controller moves to SHIFT_DATA state after waiting the assertion of RD on RD_DETECT state. SYNC is pulled down and it happens to shift serial data to an internal register on all rising edges of CLK. This is the process to receive N-1 bits. After that when SYNC is pulled up in SHIFT_EXTRA state, another shift is performed. In LOAD_DATA state, N-bits on internal register goes to DOUT. When state changes to RD_DETECT state, there is announcement for data ready. In RD_DETECT state, controller senses the RD signal after checking the mode switch condition. After synchronization, with continuous high RD, HSM-CR of the S2P stay same state to enable RD in HSMSR sub-mode or launch to receive the serial stream.

IV. EXPERIMENTAL RESULTS

Figure 24 is the chip photograph of the proposed receiver. Total area of the proposed receiver is 3.8 mm x 3.8 mm. It includes 5-channel with P2S interface. Figure 25 is the evaluation board for the proposed receiver. The evaluation board has the low noise low-dropout regulator (LDO) and Connector to Labview system. It uses SMA connector to receive the signal. Figure 26 shows the measurement environment of the proposed receiver. For measurement, the sine wave signal is applied by function generator. FPGA board has the function of S2P interface for testing P2S inside the IC.

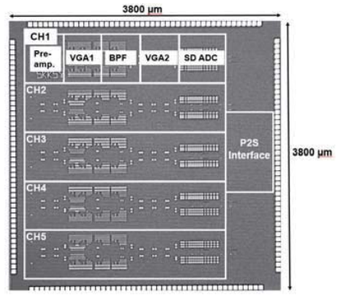


Figure 24. Chip photograph of the proposed receiver

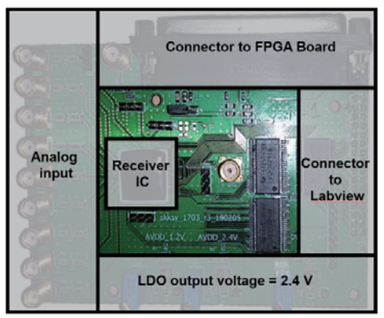


Figure 25. Evaluation board for the receiver IC

Figure 27 shows the AC simulation result including pre-amplifier, VGA1, VGA2, BPF. It has dynamic range from 20 dB to 100 dB. It shows the IR noise simulation result is around –150 dBV / √Hz. Table 2 shows the simulation result of SD ADC according to increasing sampling clock. Fs is sampling clock and Fc is the CMFB clock shown in Figure 14. If Fc is divided by Fs like this work, resolution is better especially when sampling clock frequency goes higher. [10]

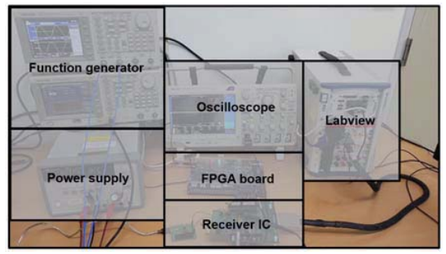


Figure 26. Measurement environment of the proposed receiver

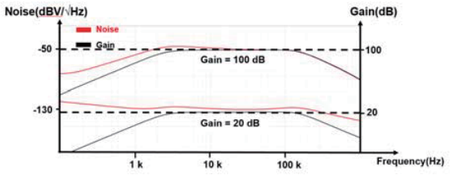


Figure 27. Noise simulation result with minimum gain and maximum gain

Table II. Simulation results of SD ADC

F_S(Hz)	OSR	Conventional structure		Proposed Structure	
		$F_C = F_S$		$F_C = F_S/16$	
		SNDR (dB)	ENOB (bits)	SNDR (dB)	ENOB (bits)
390.5 k	32	86.03	14.29	85.66	14.23
780 k	64	26.27	14.33	87.41	14.52
1.56 M	128	93.49	15.53	94.15	15.64
3.125 M	256	94.51	15.7	94.27	15.66
6.25 M	512	89.52	14.87	94.03	15.62
12.5 M	1024	74.35	12.35	92.59	15.38

The measurement result of BPF AC response is presented in Figure 28. It is flat at the frequency from 3 kHz to 130 kHz. Table 3 shows the noise measurement result of the proposed receiver. It shows the -150.36 dBV / √Hz according to adjusting gain. IR noise is output noise divided by gain. When signal goes to the receiver, the PSD result of the receiver is shown in Figure 29. It is normalized in the X axis to $F_{in}/(F_s/OSR)$. The PSD result is presented as decibels relative to full scale (DBFS) units. The SNR at the

fundamental frequency is 93.5 dB and 82.02 dB signal-to-noise and distortion ratio (SNDR). Figure 30 shows the phase difference measurement result between two channel when receiving 3 kHz signal.

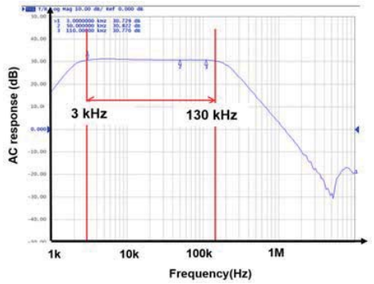


Figure 28. AC response of the band pass filter

TABLE III. Noise measurement result

Gain setting(dB)	Noise output (dBV / √Hz)
20	-126.35
29	-122.87
38	-115.6
47	-105.4
56	-92.38
65	-84.58
IR Noise (average) = -150.36	

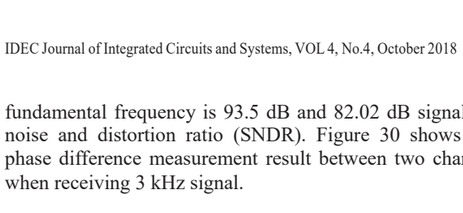


Figure 29. PSD measurement result of the proposed receiver with sinewave input

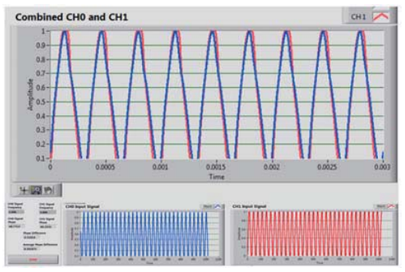


Figure 30. Phase difference measurement result between two channel

Table 4 shows the performance summary of the proposed receiver. The dynamic range is higher than those presented in [13]. The noise performance is better than that of [12]. Bandwidth of the input signal is higher than those of [11,12,13]. Since this work implemented reconfigurable structure of SD ADC, it can use variable sampling frequency that differs from [11,12,13]. Also, it can use higher sampling clock frequency than [11,12,13].

Table IV. Performance of the analog front-end

	This Work	[11]	[12]	[13]
Process (nm)	180	130	130	65
The number of channel	5	64	96	4
Dynamic range(dB)	20 - 100	N/A	N/A	40
IR Noise (nV/√Hz)	29.6 @ 50 kHz	N/A	2200 @ 10 kHz	N/A
Bandwidth (Hz)	2.8k - 130 k	1 k	< 10 k	25 k
Sampling frequency (Hz)	1.5 M – 12.5 M	N/A	31.25 k	10 M
Structure of ADC	Reconf igurable	Fixed	Fixed	Fixed
Supply voltage (V)	2.4	0.9 – 1.2	1.2	1.5
SNR (dB)	93.5	N/A	N/A	84.2
Phase difference (degree)	< ±0.8	N/A	N/A	N/A
Power consumption	46.8 m	1.8 u	6.5 m	68 u / 1-ch.
Area(mm²)	14.44	6	25	0.03

V. CONCLUSIONS

In this paper, we propose a low-noise 5-channel receiver for receiving dynamic amplitude signal especially for low frequency system for ocean acoustic measurement environment. Since environment has noise sources, we design the proposed receiver with low noise performance. Furthermore, the power consumption the receiver in the ocean environment should be lowered due to portability. This proposed receiver is applied several design techniques including chopping architecture in SD ADC. And, SDM in the SD ADC is designed with clock splitting technique. Also, digital filter in the SD ADC is designed with controller to lower the power consumption.

The designed receiver has an input-referred noise of 29.6 nV / √Hz at 50 kHz and a total gain of 100 dB. The gain of the receiver is controlled with 1-dB step precise gain so that it can be changed according to the power variation of the input signal. It implemented SD ADC with reconfigurable structure and obtain 93.5 dB SNR performance. The receiver of this paper is designed with CMOS 0.18 μm and the chip area is 3.8 mm x 3.8 mm. Power consumption is 46.8 mW at 2.4 V supply voltage. The proposed receiver can be used in the very noisy environment especially ocean acoustic measurement.

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