A Low Phase Noise Integer-N Frequency Synthesizer for 2.4GHz ZigBee Application

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Abstract **- A low phase noise and low power consumption integer-N frequency synthesizer for ZigBee application (IEEE 802.15.4) in the frequency range of 2.39-2.51GHz with channel spacing of 5MHz is designed through Samsung CMOS 65nm process. The phase noise and low power consumption are important factors for phase locked loop (PLL) design considering RF transceiver performance. The phase noise characteristics of proposed frequency synthesizer can be improved by dividing the large tuning range into a sub-band range with a small gain of VCO. Phase noise can be reduced by choosing the appropriate code value assigned to the desired channel using AFC (auto frequency calibration). Also, AFC's power consumption could be decreased in coarse tuning mode. It consumes 14 mW during the coarse tuning mode and 11 mW during the fine tuning mode at 1.2V supply, respectively. It occupies an area of 1.73 mm × 1.73 mm including PADs. The simulated phase noise characteristic of the frequency synthesizer is -125dBc/Hz at 1 MHz offset from the carrier.**

Keywords**— Auto frequency calibration, Frequency synthesizer, Low phase noise, Low power consumption**

I. INTRODUCTION

The explosive growth of the telecommunications industry has continuously promoted to increase demand for fully integrated RF transceiver with low cost and low power consumption. Among the various radio communication standards, the need for low data rates and low power software focused on sensor network applications led to the development of the ZigBee standard [1].

Frequency synthesizers are most widely used in a variety of systems such as wired and wireless communication system as well as CPU [2]. Phase noise is an important factor for RF transceiver performance, compared to other factors to considerer for frequency synthesizer design. Low power consumption is also a significant specification for RF transceiver.

This paper presents a 2.4 GHz frequency synthesizer with low phase noise and low power consumption for ZigBee applications. The paper is organized as follows. Section II presents the proposed synthesizer architecture. In Section III, the PLL building blocks are described. The simulated results are shown in Section IV and conclusions are drawn in Section V.

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II. PROPOSED SYNTHESIZER ARCHITECTURE

Fig.1 shows the block diagram of the proposed RF frequency synthesizer for ZigBee applications. It is composed of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), a programmable swallow divider, and an AFC based on digital counters. As shown in Fig. 2 (a), the VCO gain (K_{vco}) should exceed certain amount in order to obtain broadband frequencies in a VCO with single varactor. Therefore, since the output frequency f_o of a VCO with a large K_{vco} abruptly varies within a wide tuning range, the substantial gain of the VCO can significantly degrade the phase noise performance of the phase-locked loop (PLL) [3]. As shown in Fig.2 (b), the phase noise can be reduced by dividing the large tuning range into a sub-band range with a small K_{vco}. The proposed frequency synthesizer can perform low phase noise by choosing the code value assigned to the desired channel using AFC. It is called coarse tuning mode.

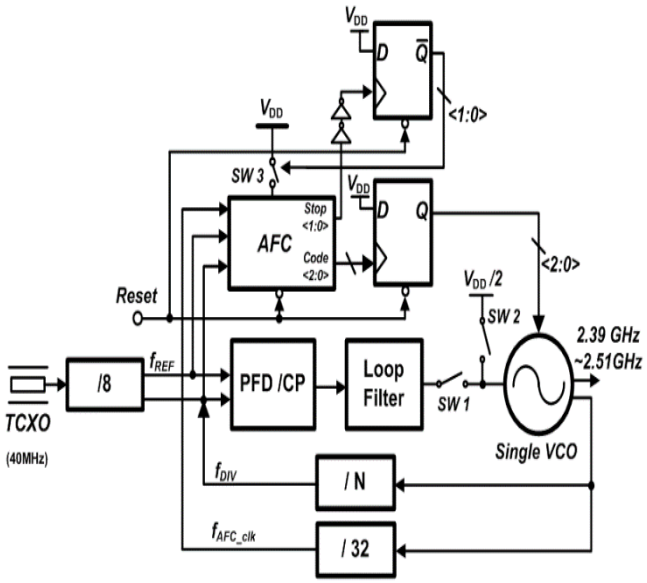
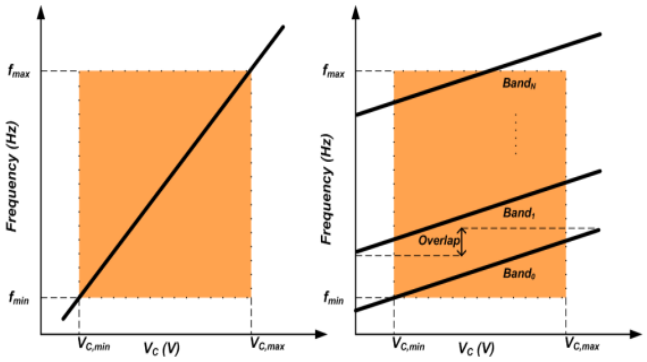


Fig. 1. Block diagram of the frequency synthesizer

Within the selected tuning range, the PLL synthesizes the selected output frequency by synchronizing the output frequency with the reference frequency generated from TCXO. It is called fine tuning mode. After coarse tuning mode, AFC is powered down to low power consumption. Then, the switch SW1 is closed and the SW2 is opened to form a PLL. Although the AFC is powered down, the value of the capacitance code is held by the D flip-flop triggered by the output of codes of the AFC.



(a) (b)

Fig. 2 (a) Single tuning curve, (b) tuning range divided into sub-bands for a wideband VCO operation.

III SYNTHESIZER BUILDING BLOCK

A. AFC

Fig.3 shows the proposed block diagram of the AFC which consists of two counters, a comparator, and a state machine. The flow of proposed AFC operation is as follows. First, two counters (counter1 and counter 2) count the rising clock edge of the reference frequency (f_{REF}) and the divider output frequency (f_{DIV}), respectively. The counter1 and counter2 counts 64 rising clock edges of f_{REF} and f_{DIV}, respectively. The outputs of two counters trigger D flip-flops to produce high logic signals for H_{REF} and H_{DIV}.

If the time difference between H_{REF} and H_{DIV} is larger than three times of the AFC's rising clock edge, the comparator generates an UP signal as shown in Fig.4 (a). The state machine that receives the UP signal from the comparator sequentially generates 3-bit code outputs from 000 to 111. In the opposite case, a DOWN signal is generated from the comparator and input to the state machine.

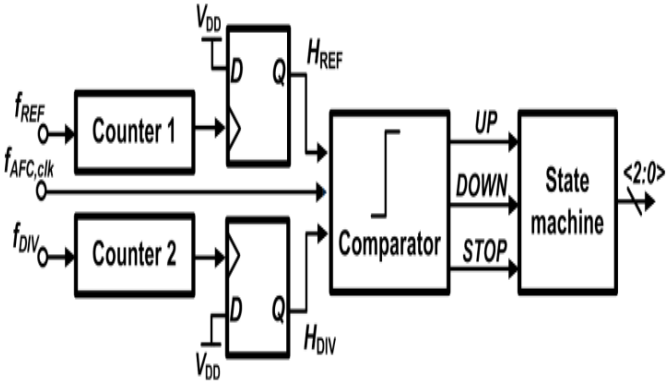
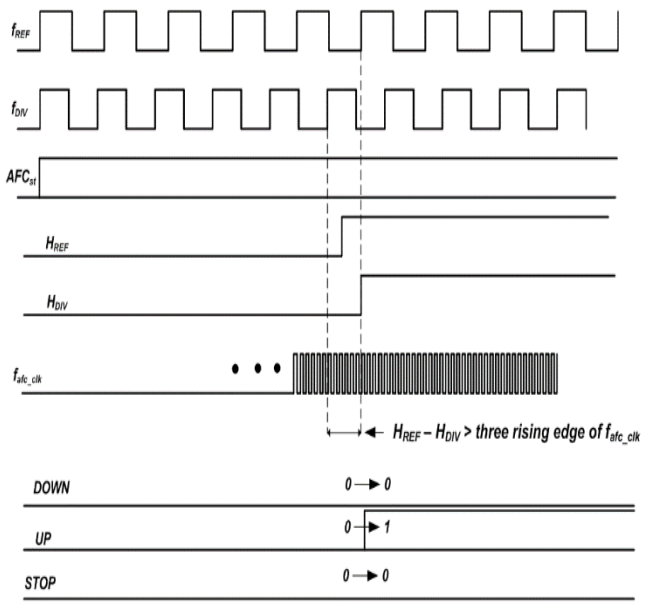


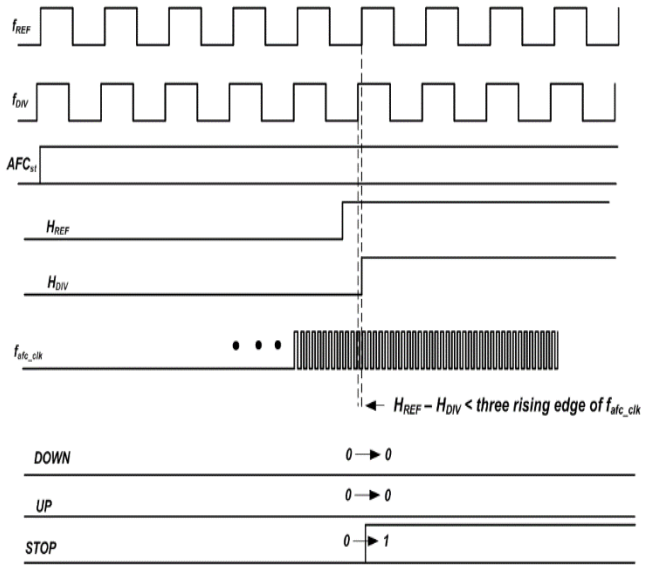
Fig. 3. Block diagram of AFC

In case that the time difference between H_{REF} and H_{DIV} is smaller than three times of the AFC's rising clock edge, the STOP signal is produced as shown in Fig.4 (b). Therefore, AFC is turned off until the RESET signal is input.

In coarse tuning mode, even though the output of the counter1 and counter2 is compared at all rising edges of f_{REF} and f_{DIV}, it can take considerable time to detect the frequency difference due to the initial phase error of f_{REF} and f_{DIV}. Therefore, the coarse tuning time depends on the initial phase relationship.



(a)



(b)

Fig. 4. Timing diagram of AFC operation: (a) when the time difference between H_{REF} and H_{DIV} is larger than three times of the AFC's rising clock edge, (b) when the time difference between H_{REF} and H_{DIV} is smaller than three times of the AFC's rising clock edge.

The flow chart for the digital calibration technique is shown in Fig.5. If the selected channel is out of tuning range, AFC is activated. Then, the switch SW1 is opened and the PLL loop is cut off. The switch SW2 is connected to V_{DD} /2. The time difference between the H_{REF} and H_{DIV} is compared to the clock of AFC to determine whether the output of the comparator is up or down. When the comparator generates STOP signal, the switch SW1 is closed and the switch SW2 is opened again, and the PLL loop is activated for fine tuning.

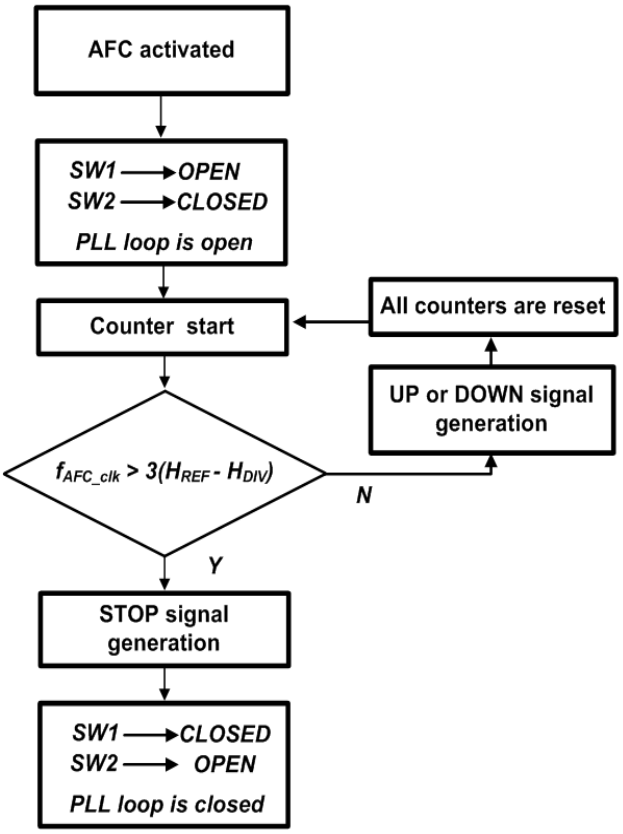
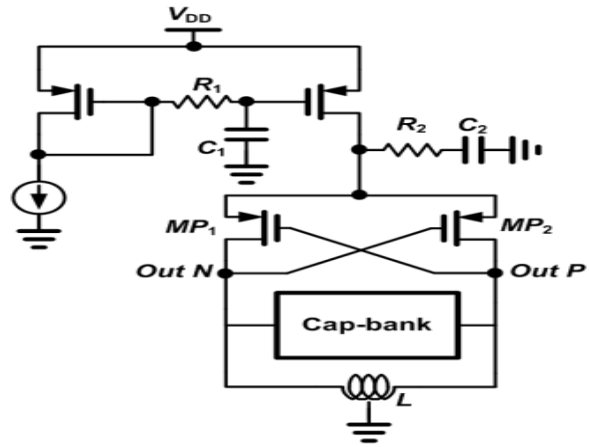


Fig. 5. Flow chart for the auto frequency calibration

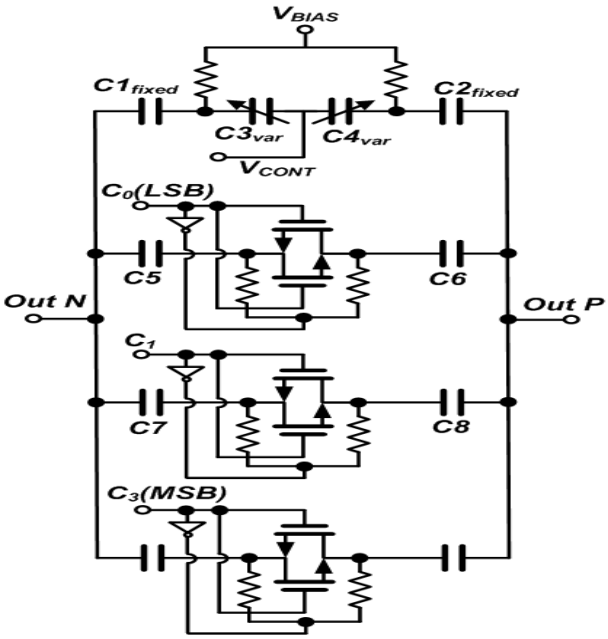
B. VCO

The simplified schematic of the VCO with frequency range from 2.39 to 2.51GHz is shown in Fig.6 (a). The designed VCO has 8 sub-tuning bands with low K_{VCO} of 33MHz. In order to reduce the phase noise caused from flicker noise, the VCO has cross-coupled pMOS transistor pairs. Since the pMOS transistor has small flicker noise compared to nMOS one, the VCO can have relatively low phase noise.

On the other hand, the noise from current source degrades the phase noise performance of a VCO [5]. It can be solved with low-pass filter composed of R_1 and C_1. Also, in order to reduce second-order harmonics of the oscillation frequency f_O, the low-pass filter composed of R_2 and C_2 is used as shown in Fig. 6 (a). Fig.6 (b) shows switchable capacitor-bank that is coarsely controlled by a 3-bit control signal. The VCO operates at the lowest frequency when the capacitor bank has maximum capacitance.



(a)



(b)

Fig. 6. (a) Schematic of VCO, (b) Capacitor-bank schematic

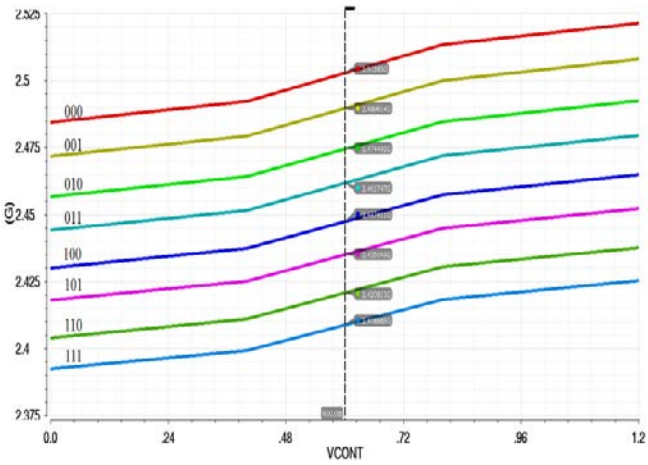


Fig. 7. Simulated tuning characteristics of the VCO

C. Gain-boosting Charge Pump

A conventional CMOS charge pump (CP) circuit has the current mismatch problem because the CMOS CP has up and down switch made of pMOS and nMOS, respectively. The mismatch between up and down current in a conventional CMOS CP causes several problems in phase-locked loop system, such as reference spurs [6]-[10]. The unbalanced charge pump has the static phase error which generates the fixed pattern jitter or degrades performance of PLL. In order to minimize current mismatch between up and down current, the gain boosting topology is adopted [11]. Fig.8 shows the simplified schematic of the designed charge pump. As shown in Fig.9, the current mismatch between up and down operation is under 5% without additional power consumption.

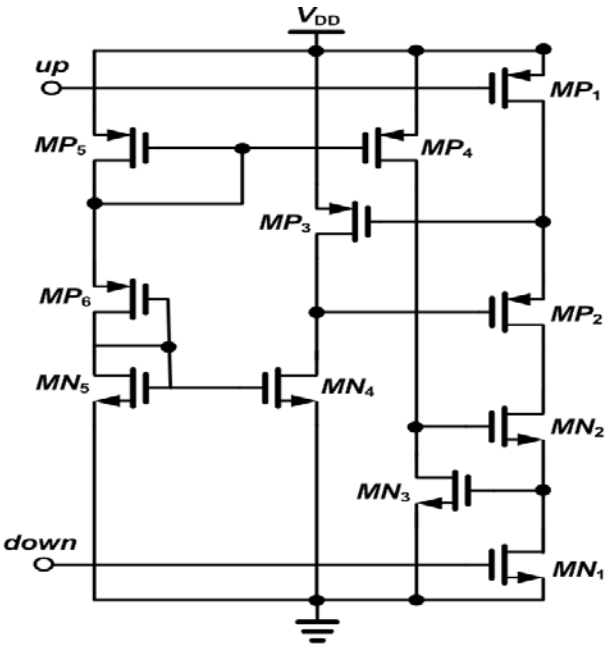


Fig. 8. Schematic of the charge pump

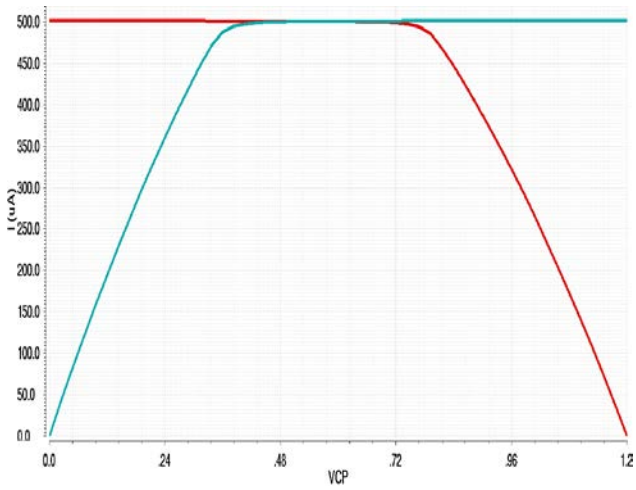


Fig. 9. Up and down output current of the charge pump using gain-boosting topology

IV. SIMULATION RESULTS

A. Transient response

The VCO control voltage is shown in Fig. 10. In the coarse tuning mode, the control voltage of VCO is connected to $V_{DD}/2$ and AFC begins to find the value of the capacitor-bank code for sub-band tuning range selection. After AFC operation is completed, the fine tuning mode is started.

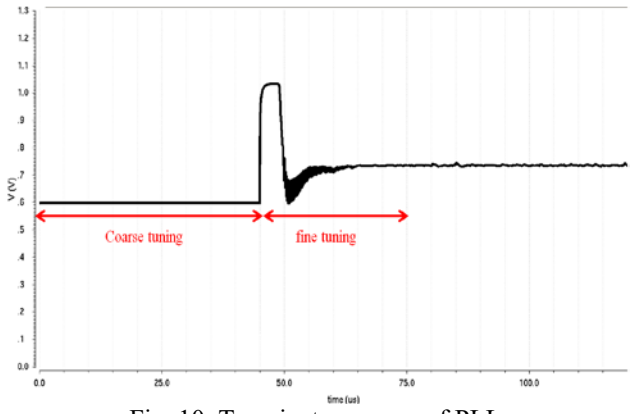


Fig. 10. Transient response of PLL

B. Phase noise simulation

The overall PLL phase noise performance is characterized by the noise contributions from all PLL circuits. Fig. 11 shows the linear phase–domain model of a PLL with additive noise source. θ_{ref} represents the noise source that appears at the reference input to the PFD. The noise source includes the noise from the crystal oscillator, crystal buffer, and reference divider. $\theta_{divider}$ shows the noise from the divider. θ_{VCO} and θ_{pfd} express the phase noise of the VCO and PFD, respectively. θ_{vcntr} represents the noise at the VCO control voltage by the loop filter. Fig. 12 shows the phase noise of the noise sources extracted from each block.

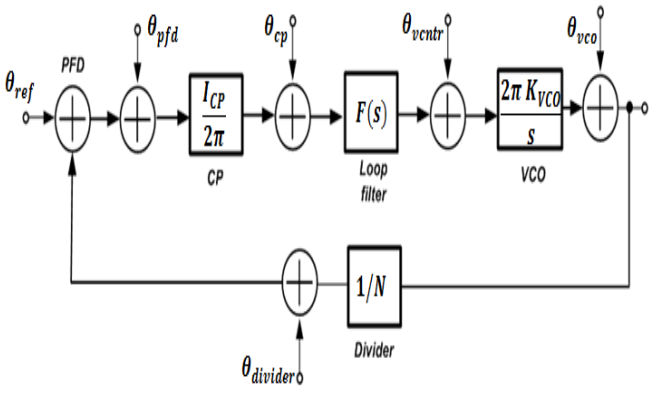
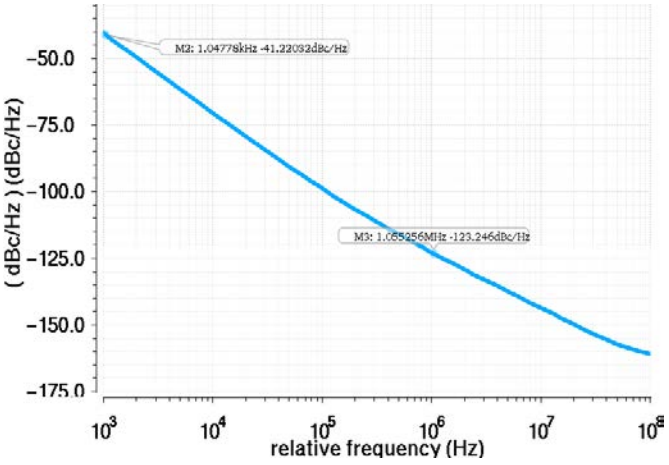


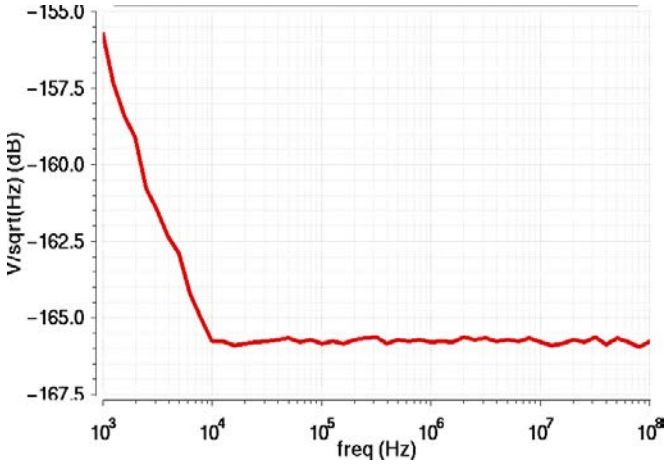
Fig. 11. Equivalent circuit model to simulate PLL phase noise

The phase noise of a VCO in a PLL is shaped by a PLL noise transfer function. A phase noise of a free running VCO is simply called VCO phase noise, while the phase noise of the VCO in a locked PLL is called PLL output phase noise.

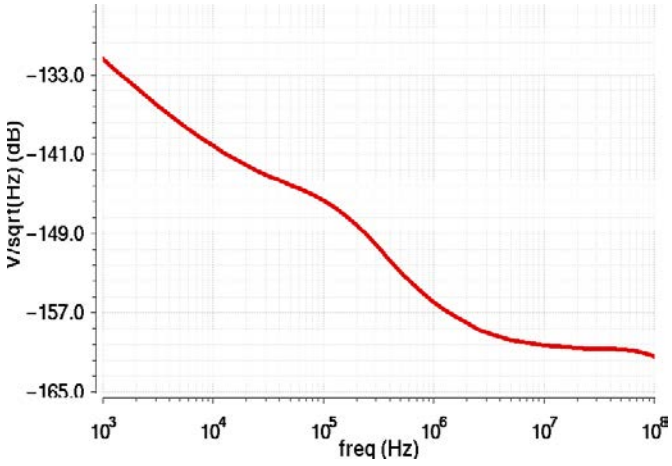
The total simulated phase noise results are presented in Fig.13. The simulated phase noise of fine tuning loop is -125 dBc/Hz at 1 MHz offset from the carrier. The phase noise of a crystal oscillator has an impact on the closed-in phase noise at 10 kHz of the PLL while VCO noise shapes phase noise of a PLL at 400 kHz offset. The phase noise of a PFD and CP increases in-band phase noise floor.



(a)



(b)



(c)

Fig. 12. (a) Phase noise of the VCO, (b) Phase noise of the TCXO, (c) Phase noise of the PFD and CP.

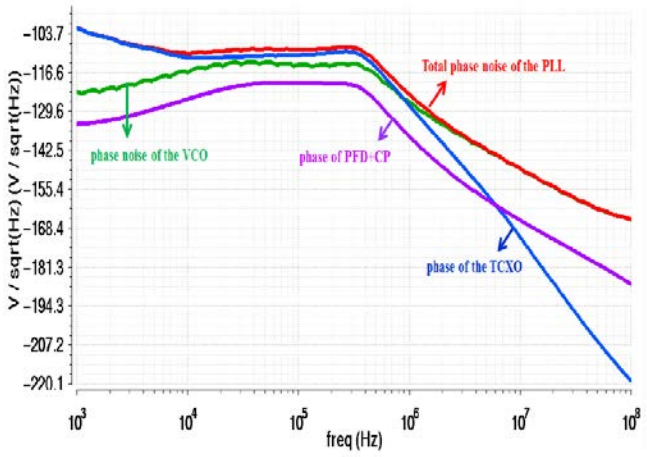


Fig. 13. Simulated total output phase noise of the frequency synthesizer.

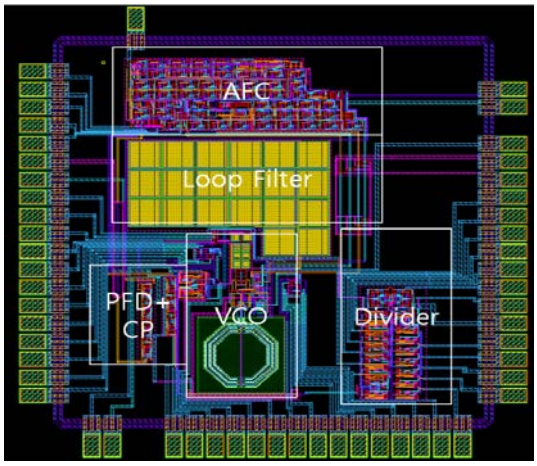


Fig. 14. Layout diagram of the frequency synthesizer

V. Conclusions

A low phase noise 2.4 GHz CMOS RF frequency synthesizer for ZigBee communication system is presented. By using a coarse tuning loop, the frequency synthesizer achieves improved phase noise performance. Since the designed synthesizer is capable of covering target frequency tuning range and a low K_{vco} of 33MHz, it is suitable for ZigBee applications.

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