A 1.2V 30 MS/s SAR ADC with Foreground Capacitor Calibration

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***Abstract* – In this paper, a successive approximation register (SAR) ADC with foreground capacitor calibration is presented. In order to overcome the drawback of SAR architecture with low-power consumption, several techniques are adopted such as high-speed latch, three-stage comparator, reference-less architecture, custom metal-oxide-metal (MOM) capacitor, and foreground capacitor calibration. The design methodology and measurement procedure is presented in detail. The prototype ADC is fabricated in a 65 nm CMOS process, and it achieves signal-to-noise and distortion ratio (SNDR) over 60 dB at sampling frequency of 30 MS/s under 1.2 V supply voltage. The power consumption is 1.1 mW, and the chip area of the core ADC is 0.045 mm^2.**

***Keywords*—Capacitor mismatch, foreground calibration, successive approximation register (SAR) ADC**

I. INTRODUCTION

Low-power techniques are an important factor to extend devices' battery life in the rapidly growing portable device market. Thus, a successive approximation register (SAR) ADC has been widely adopted in recent years due to its straightforward operation principle, with low power consumption compared to other architectures. However, it is difficult to improve sampling frequency, because of increased bit-decision cycles as the resolution of an ADC and limitation of DAC settling, which are determined by transistor turn-on resistance and capacitance. Therefore, a SAR ADC is commonly used in relatively low speed fields, such as bio-medical, sensor, EEG and EMG [1, 2].

As the semiconductor process progresses, the size of the MOS transistor has gradually reduced, which enables to raise the operating frequency of the SAR ADC to a higher frequency band. This is because of the resistance of the MOS transistor in the linear region being diminished, as technology scales down. The SAR ADCs enlarge the operating frequency band to several tens of MS/s, such as wireless section, and aims to reach several hundreds of MS/s using multi bit-per-cycle or any other techniques [3-5].

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Manuscript Received Jan. 07 2019, Revised Feb. 11, 2019, Accepted Feb. 13, 2019

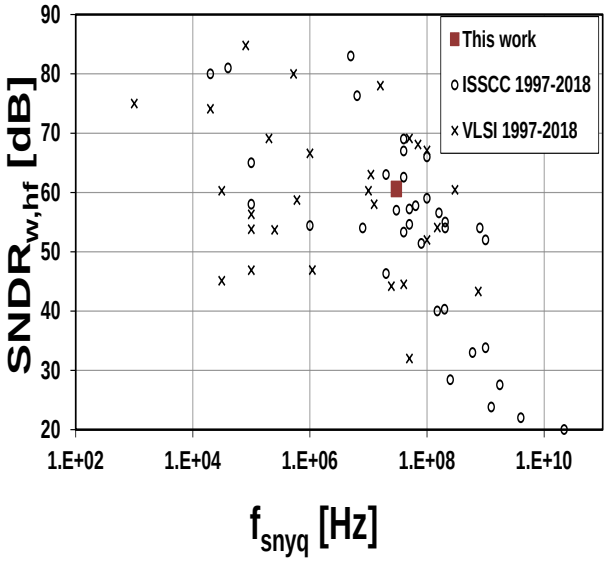


Fig. 1. A survey of SAR ADCs in terms of sampling frequency and SNDR

In contrast to the improvement in operating speed of SAR ADC, resolution performance such as SNDR has not been dramatically improved with the developing process. This is due to the fact that the reference level to convert the input signal depends on capacitor matching in SAR ADC. As the size of the metal is scaled down, the capacitor mismatch makes it difficult to guarantee high linearity.

Fig. 1 shows published SAR ADCs in terms of sampling speed and SNDR [6]. Based on the architectural disadvantages of SAR ADC, the SNDR performance and sampling frequency tend to be inversely proportional to each other. Nevertheless, methods to overcome these drawbacks have been intensively studied, as compared to other ADCs, owing to the low power architecture. Likewise, this paper describes a high-speed latch and three-stage comparator to increase the sampling frequency and introduces custom capacitor layout and capacitor mismatch calibration to improve SNDR performance. In addition, the overall design methodology is discussed.

This paper is organized as follows. The design of SAR ADC is described in section II. Section III shows the foreground capacitors mismatch calibration technique. The measurement and discussion are presented in section IV. Finally, the conclusion is drawn in section V.

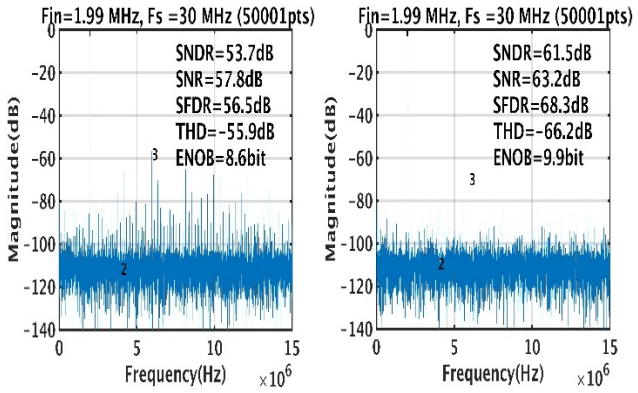
II. DESIGN METHODOLOGY OF SAR ADC

A. Modeling of SAR ADC

The modeling of the SAR ADC was performed using the MATLAB tool to determine the various design parameters such as total sampling capacitor, noise contribution for each ADC blocks, consideration of redundancy capacitors and so on.

```
------------------------------------------------------------------
---------------------- SAR CAPDAC ------------------------------
------------------------------------------------------------------
------------------------------------------------------------------
order     ideal_CW       CDAC_vip (fF)      CDAC_vin (fF)
------------------------------------------------------------------
 1(dum)      1             0.404934           0.390162
 2           1             0.468483           0.327797
 3           2             0.764891           0.818590
 4           4             1.605176           1.778557
 5           8             3.428516           3.112384
 6           8             3.265917           2.919589
 7          16             6.281568           6.273926
 8          32            12.538605          12.955526
 9          64            25.218985          26.078855
 10        128            51.016508          51.547936
 11        128            50.523988          52.636548
 12        256           102.254667         103.489483
 13        512           205.302992         204.240355
 14       1024           408.286525         406.992378
------------------------------------------------------------------
 Total                    871.3618           873.5621
 Cp                       440.0000           440.0000
------------------------------------------------------------------
 Cs                       1311.3618          1313.5621
------------------------------------------------------------------
------------------------------------------------------------------
---------------------- SAR Parameters --------------------------
------------------------------------------------------------------
Input signal swing (Diff pp) = 1.60 ( Vref = 1.2 )
------------------------------------------------------------------
1LSB step (Resolution)   = 194.7516 (uV)
------------------------------------------------------------------
Quantization Noise          = 56.22 (uV)
Comp Noise(Diff)            = 180.00 (uV)
KT/Cs Noise(Diff)           = 39.71 (uV)
Reference Noise(Diff)       = 75.32 (uV)
Amp Noise(Diff)             = 50.00 (uV)
------------------------------------------------------------------
```

(a)



(b) (c)

Fig. 2. Modeling of SAR ADC; (a) parameters (b) output spectrum before capacitor calibration (c) output spectrum after capacitor calibration for upper 4 MSB capacitors

Fig. 2 (a) shows the modeling results of the designed SAR ADC. It has 12-bit resolution and a total of 14 conversion cycles with two redundancy cycles. The total sampling capacitor is 1.3 pF to consider KT/C noise, and the unit size of custom capacitor is determined as 0.4 fF considering a practical layout. Our target performance of the SAR ADC shown is over 60 dB of signal-to-noise and distortion ratio (SNDR) after capacitor mismatch calibration. Before the capacitor mismatch calibration, the SNDR of the SAR ADC achieves about 54 dB due to the effect of capacitor mismatch as shown in Fig. 2 (b). After capacitor mismatch calibration for upper 4 MSB capacitors, the SNDR of SAR ADC is improved to 61 dB as shown in Fig. 2 (c). The amount of noise is set to have a smaller effect than capacitor mismatch. The detailed foreground capacitor mismatch calibration method is discussed in section III.

B. Bootstrap

In the designed SAR ADC, top-plate sampling is used to reduce the MSB sampling capacitor. Therefore, channel charge injection from a sampling MOS transistor is a major factor in performance degradation for ADC with high linearity. In order to alleviate channel charge injection, Fig. 3 shows the bootstrap circuit which keeps the gate-source voltage of the MOS transistor constant for any input level. When the clock is low, the sampling transistor is turned off and the capacitor is charged to VDD. When the clock is high, one side of the capacitor is connected to the input and the other side is connected to the gate of the sampling MOS transistor. As a result, the gate-source voltage is continuously kept at VDD by the capacitor. The body of the PMOS that controls the boosted voltage is connected to the boosted voltage side, not to VDD, because the boosted voltage is always greater than VDD. In our bootstrap circuits, a triple well MOS transistor is used to disconnect from supply noise caused mainly by the digital circuit.

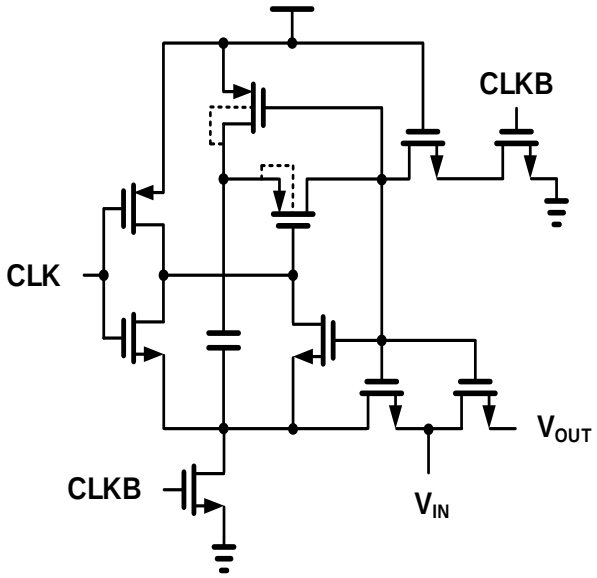


Fig. 3. The schematic of a bootstrap circuit to reduce channel charge injection of sampling switch

C. Comparator

Fig. 4 represents the dynamic comparator circuit of the designed SAR ADC [7]. In order to achieve a large gain at low supply voltage, we chose a three-stage architecture with 3-stacked transistors. The detailed operation method is as follows. When the clock is low, the first stage output of comparator is reset to VDD by M4 and M5. The final output stage is also reset to VDD by the reset switch M16, M17, M18 and M19. When the clock is high, the first output node rises to VDD with the time difference as the input levels. The second stage class-AB amplifiers amplify the each first outputs. Then, the cross-coupled inverters in the third stage quickly regenerate comparator outputs using positive feedback. In the designed comparator, the switch size should be determined appropriately, because the small size of the reset switch causes dynamic offset of the comparator, and the excessive size of reset switch causes the parasitic capacitor to slow down regeneration and consume more power. The regeneration core consists of M10-M13 should be small in size to achieve fast regeneration time. Moreover, input transistors M1 and M2 are large enough to reduce input referred noise and comparator static and dynamic offset from transistor mismatch. The detailed transistor sizes of comparator are summarized in Table I. From the modeling, the noise amount of comparator is set to about 180 μV_{rms}. Due to the limitation of increasing size of the input transistors, MOS capacitors are added on the first stage output to lower the noise level.

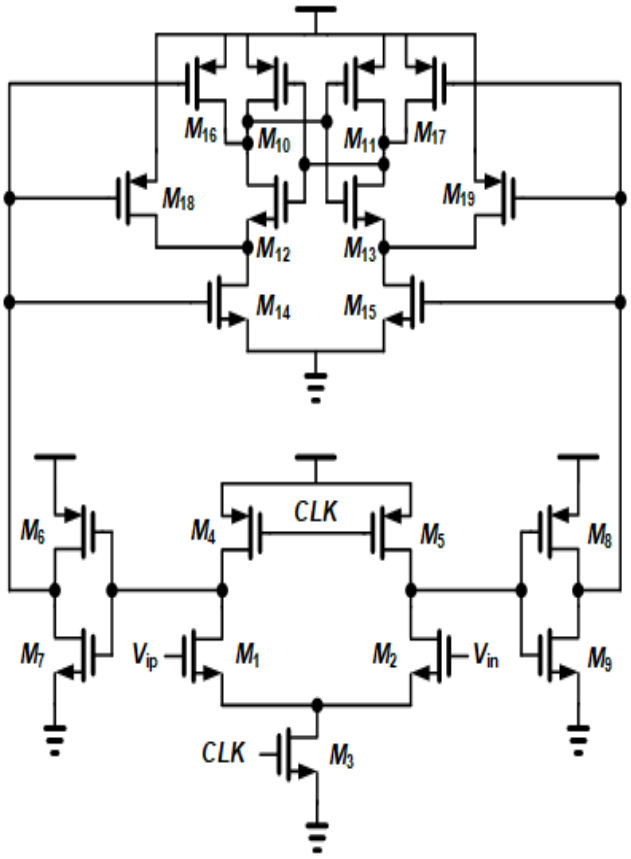


Fig. 4. Schematic of three-stage dynamic comparator

TABLE I
Transistor Parameters of Comparator

Transistor	Transistor Size W/L [um/um]
M1,M2	43.2/0.065
M3	6.48/0.065
M4, M5	8.64/0.065
M6, M8	7.28/0.065
M7, M9	4.32/0.065
M10, M11	1.44/0.065
M12, M13	0.72/0.065
M14, M15	1.44/0.065
M16, M17	0.72/0.065
M18, M19	1.44/0.065

D. Reference-less architecture

A reference buffer is used in many ADCs to provide a small output impedance for fast reference voltage settling. However, the reference buffer consumes static current to generate small output impedance and may even consume more power than the SAR ADC. In our design, we did not use the reference buffer for low power operation. As a penalty for this, the sampling frequency of SAR ADC is limited to reference voltage settling. Originally, the sampling frequency is possibly up to 40 MS/s except for reference voltage settling.

E. SAR Logic

Conventional digital logic of a SAR ADC consists of two flip-flop arrays. The first array provides a conversion sequence and consists of a shift register. Thus, the information of the current cycle is sequentially shifted every time when comparator is operated, and the size of shift register is determined by the total conversion cycles. The second flip-flop array is to catch and hold a comparator output. From the first flip-flop array conversion sequence, the comparator outputs are stored in each flip-flop in the second array and drive capacitor DAC to generate the next reference level. This logic configuration is very simple and can be implemented with low-power. However, the propagation delay of clock to output delay of flip-flop is the largest bottleneck in the SAR ADC to achieving high speed operation. Therefore, a custom SAR logic is adopted to catch data rapidly as shown Fig. 5 [8]. From the first flip-flop array, the enable signal (EN) is to be sequentially high. When EN is high, the data input D_{IN} is passed through transmission gates. Then, the logical data is propagated through three inverters. When the current conversion cycle ends, the enable signal is low. The input transmission gate separates stored conversion data from comparator output $D_{IN,}$ and the transmission gate in the output buffer activates the internal

latch. Lastly, the SAR logic is reset when SAR conversions are completed, the NMOS reset switch forces the input of output buffer to be low, and PMOS reset switch sets floating node to high level.

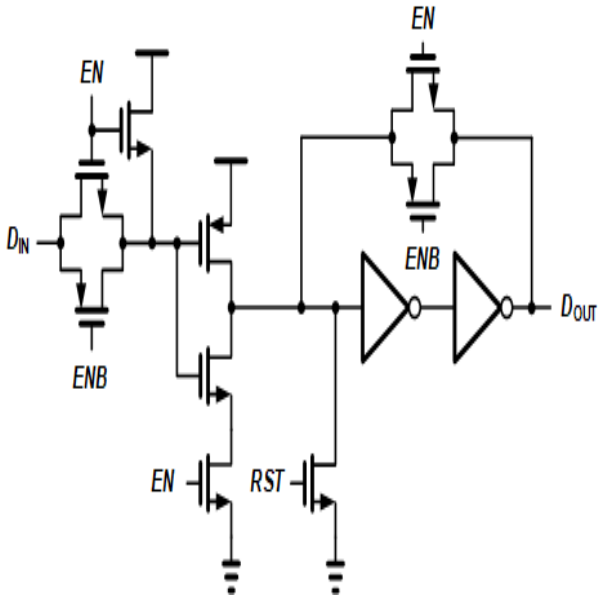


Fig. 5. Schematic of high speed data latch

Fig. 6 shows the custom MOM capacitor layout. Metal 5 and 6 layer are used to reduce parasitic capacitor from substrate. The unit capacitance of CDAC is 0.4 fF and unit capacitance for mismatch calibration is 0.125 fF, which is 4 times smaller than unit capacitance of CDAC for fine tuning.

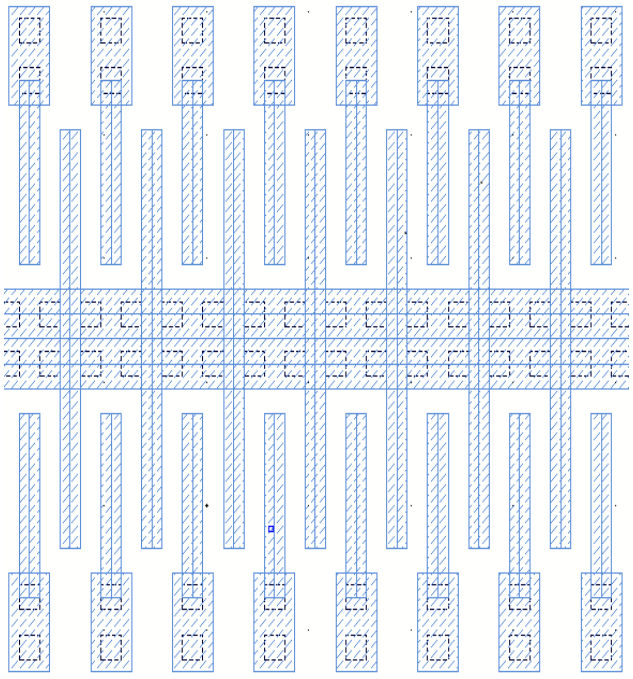


Fig. 6. Custom capacitor layout using stacked metal 5 and 6

III. FOREGROUND CAPACITOR MISMATCH CALIBRATION

As CMOS devices become smaller due to process evolution, the SAR ADC has the advantage of operation speed and low power implementation. However, the capacitor mismatch, which determines the linearity of SAR ADC, is becoming worse. For most SAR ADCs with high resolution, the minimum capacitor value is limited by capacitor matching rather than KT/C noise. Likewise, in this design, the small unit capacitor is used for fast operation speed, and the capacitor matching issue is resolved through calibration. Among two calibration methods, called foreground and background calibration, we adopt the former because the error from capacitor mismatch appears deterministically. We calibrate the top four capacitors with the largest matching error among the 14 capacitors including the two redundancy capacitors.

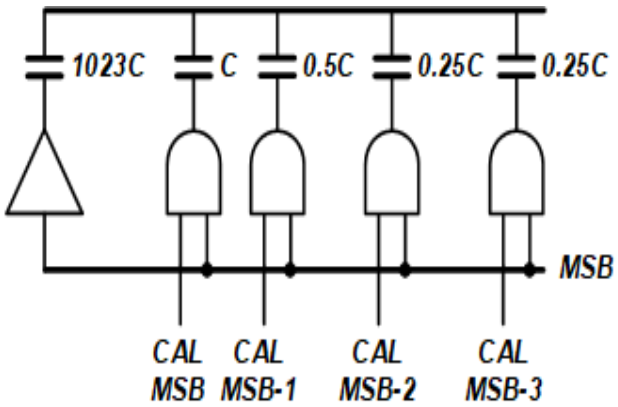
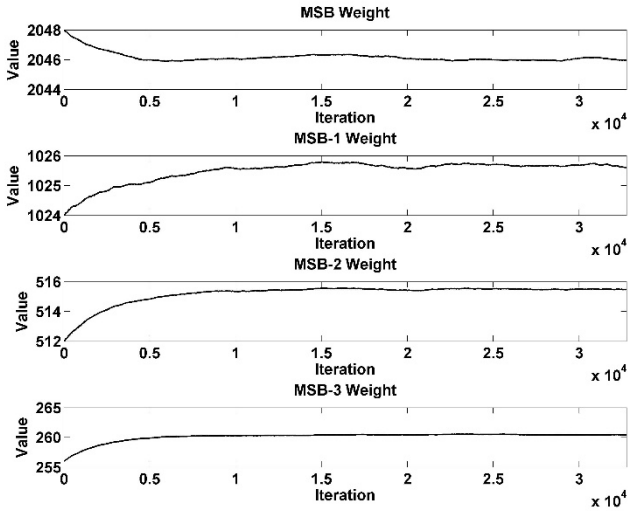


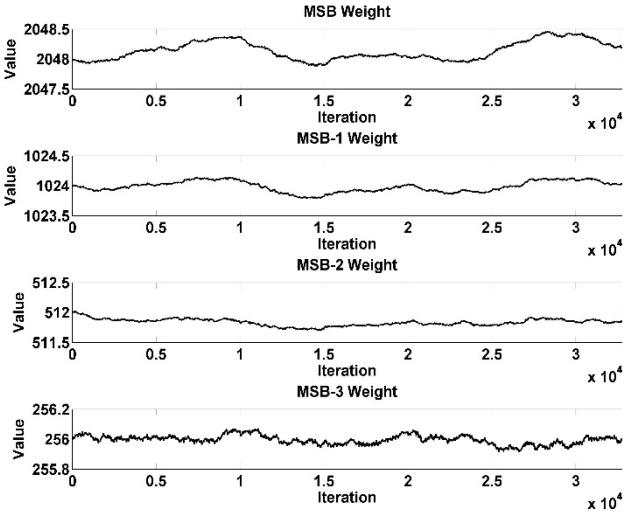
Fig. 7. Custom capacitor layout using stacked metal 5 and 6

Fig. 7 shows the MSB capacitor with mismatch calibration capacitors. Originally, the MSB capacitor is composed of a total of 1024C. The MSB capacitor is reduced to 1023C and total size of 2 unit capacitor with 1/4 of resolution is used to adjust the size of the MSB capacitor. The NAND gates drive each calibration capacitors, and calibration data codes CAL MSB from decoder determine the mismatch capacitor activation.

In the foreground calibration, the loot-mean-square (LMS) algorithm is used to obtain the error information. Fig. 8 (a) shows the calculation of the weights with the lowest error using the LMS for the weight of upper 4 MSB. Although we use approximately 215 measured output samples, it can be seen that the LMS algorithm can be utilized with approximately 10,000 output samples. Before calibration, four MSB weights with minimum error deviate from the binary weight due to capacitor mismatch. This error information is the source for adjusting the capacitor. For example, as the MSB-3 capacitor requires about 260 weight, the MSB-3 capacitor should be increased. Thereby, the capacitor mismatch calibration is performed in sequence from the lower capacitor to upper capacitor. After calibration, the capacitors are calibrated to achieve minimum error and hence, obtaining binary weight as shown in Fig. 8 (b).

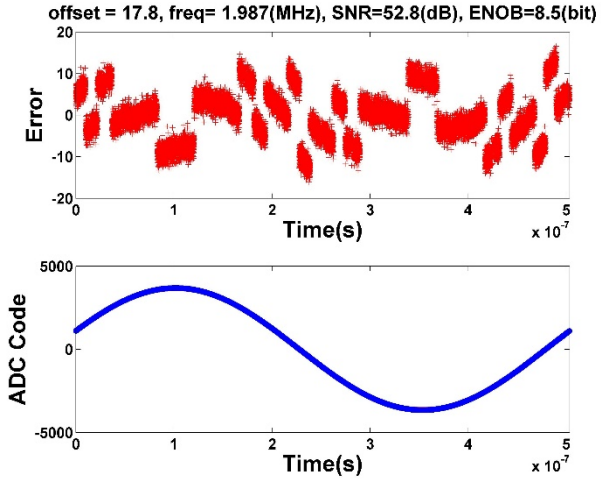


(a)

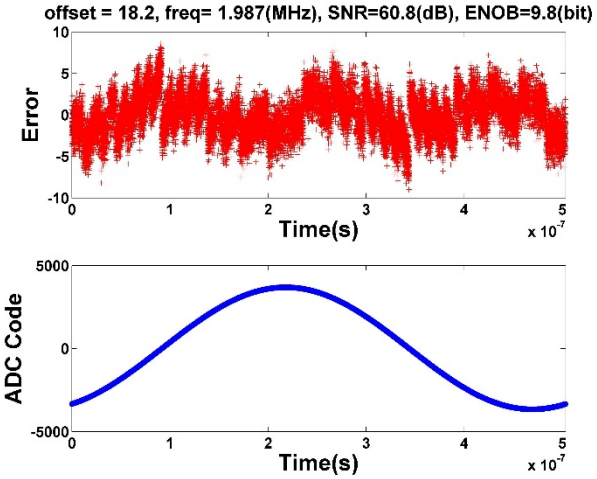


(b)

Fig. 8. The required weights for the 4 MSB through LMS algorithm; (a) before calibration (b) after calibration



(a)



(b)

Fig. 9. Sine wave curve fitting of measured outputs; (a) before capacitor mismatch calibration (b) after capacitor mismatch calibration

IV. RESULTS AND DISCUSSIONS

The prototype ADC is fabricated in 65 nm CMOS process with a sampling frequency of 30MS/s consuming 1.1 mW under 1.2 V supply. Fig. 11 shows the measurement board of prototype SAR ADC. Digital IO and LDO is implemented by using switches and external chips. In addition, the SPI controller, logic analyzer, and signal generator for testing ADC utilize instruments. Fig. 12 shows die photograph of the prototype ADC. The core ADC occupies 150-um height and 300-um width. Fig. 13 shows the measured output spectrum of prototype ADC. With 1.9 MHz input frequency, a measured spurious free dynamic range (SFDR) and SNDR are 66.1 dB and 60.8 dB, respectively. With near Nyquist frequency, the prototype ADC achieves SFDR of 75.2 dB and SNDR of 60.6 dB. The calculated figure of merit (FoM) is 41 fJ/conv.-step. Fig. 13 shows the DNL and INL to show the static performance. The measured minimum and maximum DNL are -1 LSB and 4.6 LSB, respectively, and measured minimum and maximum INL are -6.2 LSB and 5.6 LSB, respectively, owing to a capacitor calibration. The overall performance of the prototype ADC is summarized in Table II and compare to [5, 9, 10].

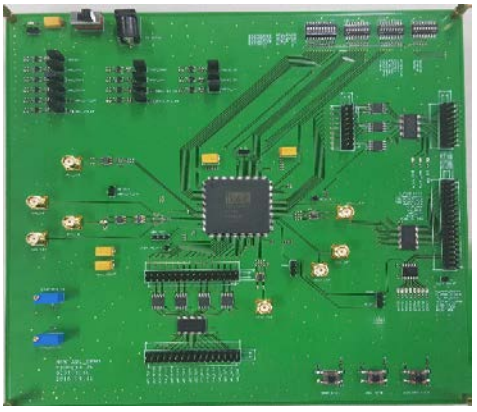


Fig. 11. Test Board to measure prototype SAR ADC

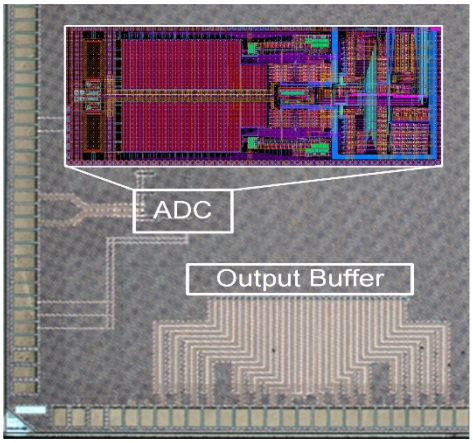
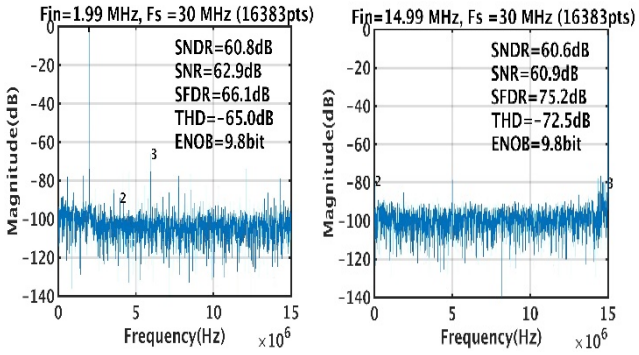
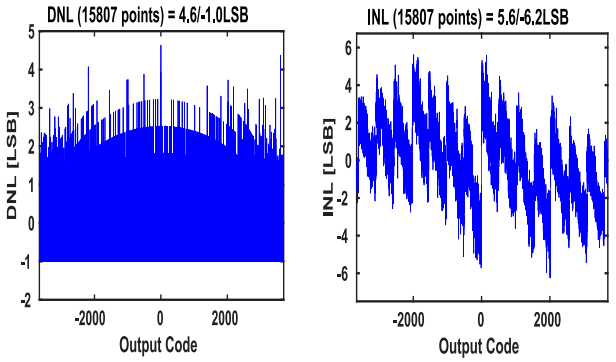


Fig. 12. Die photograph



(a) (b)

Fig. 13. Measured output spectrum at; (a) 1.9 MHz input (b) 14.9 MHz input



(a) (b)

Fig. 14. Static performance of the prototype ADC; (a) DNL (b) INL

TABLE II
Performance Summary and Comparison

	[5]	[9]	[10]	This work
Technology (nm)	130	130	90	65
Resolution (bit)	10	12	9	12
Sampling Rate (MS/s)	50	45	40	30
Supply Voltage (V)	1.2	1.2	1	1.2
Area (mm^2)	0.052	0.059	0.09	0.045
ENOB (bit)	9.2	10.8	8.2	9.8
Power (mW)	0.826	3.02	0.82	1.1
FoM (fJ/conv.-step)	29	36.3	54	41.1

V. CONCLUSION

A design methodology for high speed and linear SAR ADC with low power consumption is presented. The design considerations are introduced in the order of modeling of SAR ADC, bootstrap, three stage comparator, reference-less architecture, SAR logic and custom capacitor. In addition, the foreground capacitor calibration method is described to resolve the matching issue of reduced total sampling capacitor due to the high speed implementation. Thanks to the capacitor mismatch calibration, the prototype ADC achieves over SNDR of 60 dB under 30 MS/s sampling frequency with 1.1 mW power consumption, yielding 41.1 fJ/conversion-step.

ACKNOWLEDGMENT

This research was supported by the National Research Foundation of Korea Grant funded by the Korean Government (NRF-2016R1A2B4016544). The EDA tools were supported by IDEC, Korea

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