

Design of a hybrid SAR-cyclic ADC with gain-error calibration

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Abstract - Low-power consumption and medium resolution analog-to-digital converters (ADCs) operate at several tens of MS/s. These are crucial factors for portable wireless communication applications. In this paper, SAR-assisted cyclic ADC features the low-power merit of successive approximation (SAR) ADC and small chip area of cyclic ADC. It improves an intrinsic limitation of ADCs conversion speed. The power consumption of the operational amplifier for cyclic ADC is reduced dramatically by using a new simple gain-error calibration technique. The MSB 4-b is converted by cyclic ADC and it only needs 2 cycles by multiplying digital to analog converter (MDAC) operation. Residue voltage generated at the end of the 2nd cycle conversion of cyclic ADC is converted by 6-b SAR operation.

Keywords – SAR, Cyclic, gain-error calibration

I. INTRODUCTION

As shown in the Fig.1, the analog-to-digital converter (ADC) is an important block for wireless communication system to process analog signal. It passes through antenna for transmission and an analog filter of receiver converts to digital bits for a binary-based digital signal processor. The demand for various portable communication systems is increased by the day so medium resolution (8~10 bit) and moderate speed (tens to hundreds of MS/s) of ADCs are required. These must have two features. First, these operate always on at every time. Second, the minimum of the size and sophisticated integration are required for reduction of the costs. It is regard as a major consideration to analog circuit designers. Cost saving and microminiaturization require more advanced integration technologies and limited battery life is one of the serious specifications for portable devices. Therefore, low power scheme is the essential requirement in wireless ADCs to improve the efficiency of battery lifetime.

Among various Nyquist-rate ADC architectures, each ADC has different target range according to its resolution and sampling rate as shown in Fig.2. In general, the sigma-delta architecture is suitable to the industrial measurements

due to the medium speed and high accuracy. The flash ADC has an ultra-high speed characteristic but it has a structural limitation of the geometric number of comparators. Above two ADCs are not demonstrated in detail in this paper. As shown in the Fig. 2, the target of ADCs defines moderate speed and medium resolution, so successive approximation register (SAR) ADC and pipelined ADC can be strong candidates. However, both ADCs may not match perfectly for portable communication application because of several issues like low speed or power consumption. The technical analysis of new architectures of is presented in the following the chapters.

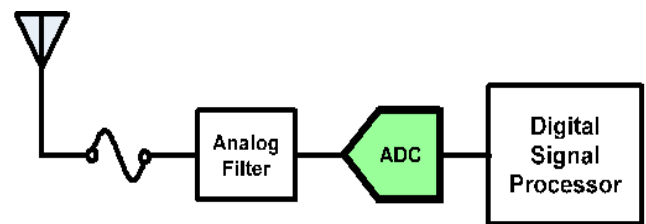


Figure 1. Wireless communication system block

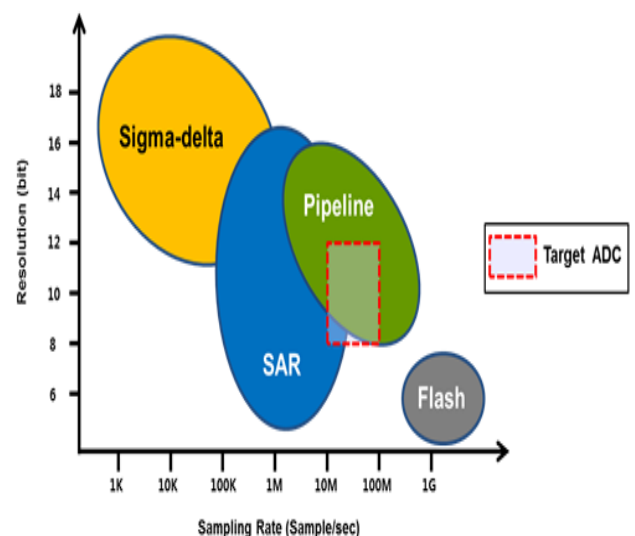


Figure 2. ADC architectures domain area

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II. SAR-CYCLIC ADC

A. The introduction of SAR-assisted cyclic A/D converter

Fig. 3. illustrates a SAR-assisted cyclic ADC block. This architecture consists of the cyclic ADC applied CLS gain error calibration and the binary weighted asynchronous SAR ADC. When the cyclic ADC converts Nth sampled input, the SAR ADC processes previous N-1th input signal in the same time. That means each ADCs convert the different sampled input, so the time interval is a one-conversion period causing the latency of total resolution as 2 periods.

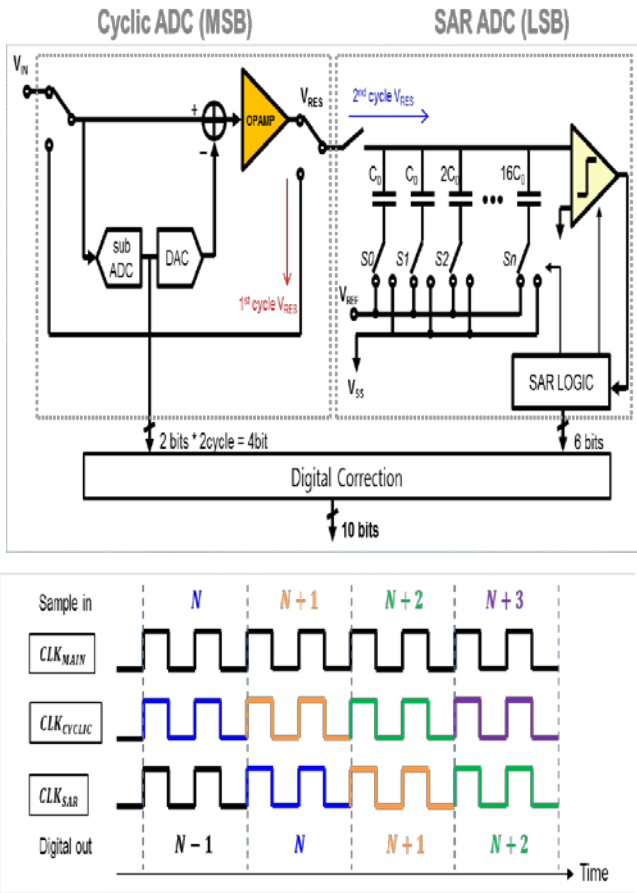


Figure 3. SAR-assisted cyclic ADC block

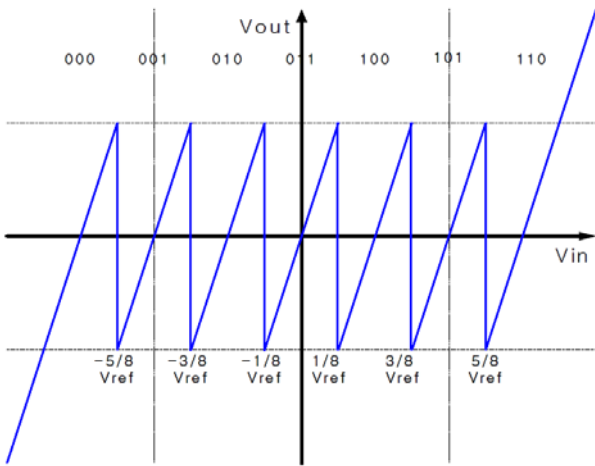


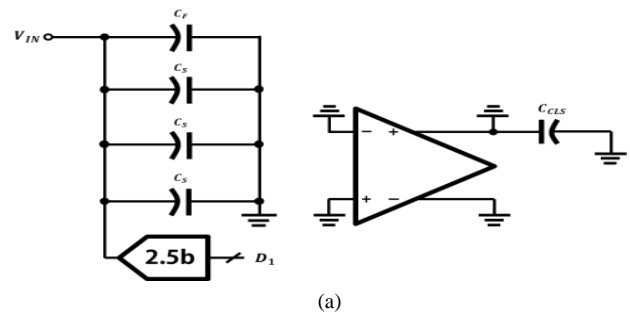
Figure 4. Transfer curve of 2.5bit MDAC

B. M-DAC operation for redundant calibration

The first stage of cyclic ADC with the CLS calibration is based on 2.5bit MDAC architecture. As shown in Fig.4., the output curve of 2.5bit MDAC is changed by using 6 comparators to generate 7 digital levels (000~110). In order to amplify a residue signal into the full reference swing, the closed-loop gain of the amplifier is 4 made by 3 feedback capacitors and 1 sampling capacitor. The transfer function is followed to (1) in the ideal case. Since more accurate resolution MDAC degrades the loop gain due to the reduction of the feedback factor (β), the amplifier is more gain required to maintain the same performance of CLS calibration.

$$V_{out} = \begin{cases} 4 \cdot V_{in} - 3 \cdot V_{ref} & \text{if } V_{in} > \frac{5}{8} \cdot V_{ref} \\ 4 \cdot V_{in} - 2 \cdot V_{ref} & \text{if } \frac{5}{8} \cdot V_{ref} > V_{in} > \frac{3}{8} \cdot V_{ref} \\ 4 \cdot V_{in} - 1 \cdot V_{ref} & \text{if } \frac{3}{8} \cdot V_{ref} > V_{in} > \frac{1}{8} \cdot V_{ref} \\ 4 \cdot V_{in} & \text{if } \frac{1}{8} \cdot V_{ref} > V_{in} > -\frac{1}{8} \cdot V_{ref} \\ 4 \cdot V_{in} + 1 \cdot V_{ref} & \text{if } -\frac{1}{8} \cdot V_{ref} > V_{in} > -\frac{3}{8} \cdot V_{ref} \\ 4 \cdot V_{in} + 2 \cdot V_{ref} & \text{if } -\frac{3}{8} \cdot V_{ref} > V_{in} > -\frac{5}{8} \cdot V_{ref} \\ 4 \cdot V_{in} + 3 \cdot V_{ref} & \text{if } -\frac{5}{8} \cdot V_{ref} > V_{in} \end{cases} \quad (1)$$

Total conversion steps are described in Fig.5. First, the 4 capacitors are sampled by the input signal. At the same time, the sub flash ADC converts 2.5bit binary code (D_1) and the amplifier and C_{CLS} are reset. Next, C_{CLS} samples the output voltage existing gain error like a typical MDAC. The bottom plates of the three sampling capacitors are connected to the each reference voltage ($+V_{REF}$, 0 , $-V_{REF}$) depended on D_1 . In comparison with a conventional cyclic ADC, there are no extra capacitors for the sample of the second conversion. In third phase, C_{CLS} is connected in serial while the sub ADC determines second 2.5bit digital output (D_2). The input value of the second cyclic conversion remained in the feedback capacitor (C_F). Prior to the 4th phase, the feedback capacitor is divided by 1/4 for next conversion capacitors. The rest implementation of phase 4 and 5 is almost a same process with phase 2 and 3 except to connect a capacitor DAC array (C_{SAR}).



(a)

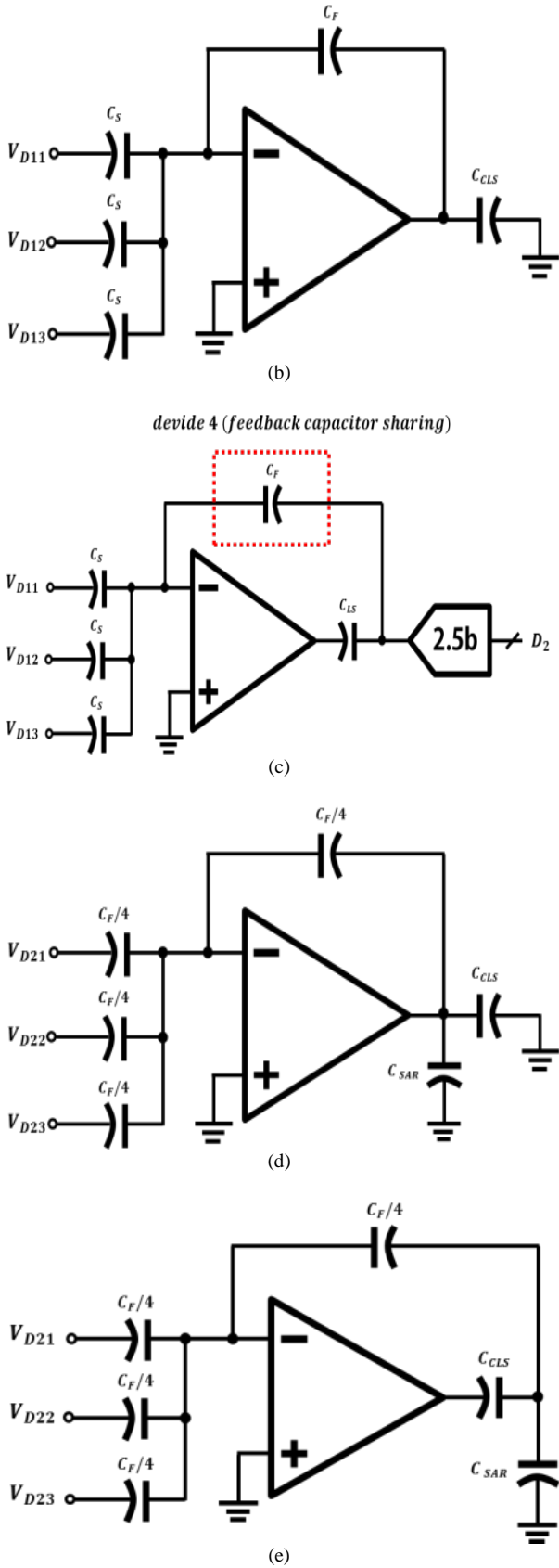


Figure 5. First stage cyclic ADC with gain-error calibration (a) phase1; sampling (b) phase2; 1st estimation (c) phase3;1st level shift (d) phase4; 2nd estimation (e) phase 5; 2nd level shift

This conversion is explained as a transfer equation. In phase 1, the total sampled charge is described in (2).

$$Q_s = (3C_S + C_F) \cdot V_{IN} \quad (2)$$

According to the charge conservation law, the estimation voltage of first cyclic conversion is shown in (3) during phase 2.

$$V_{EST1} = \frac{1}{1 + \frac{1}{T_1}} \cdot \left(\left(\frac{3C_S + C_F}{C_F} \right) \cdot V_{IN} + K_1 \cdot V_{REF} \right) \quad (3)$$

$$T_1 = \frac{A \cdot C_F}{3C_S + C_F + C_P}, \quad K_1 = \frac{C_S}{C_F} \cdot (D_{11} + D_{12} + D_{13})$$

In the phase 3, the first output (V_{OUT1}) is determined as illustrated in (4). The effective loop gain is the square of original loop gain (T_1).

$$V_{OUT1} = \left(\frac{2 + \lambda_1 + T_1}{1 + \lambda_1 + T_1} \right) \cdot V_{EST1} \approx \frac{1}{1 + \frac{1}{T_1^2}} \cdot \left(\left(\frac{3C_S + C_F}{C_F} \right) \cdot V_{IN} + K_1 \cdot V_{REF} \right) \quad (4)$$

$$\lambda_1 = \frac{1}{C_{CLS}} \cdot \left(C_F \cdot (3C_S + C_P) \right)$$

The input value of the second cyclic conversion reuses the charge of the feedback capacitor (C_P). The second estimation operation follows the equation (5) during phase 4.

$$Q_{RES1} = C_F \cdot \left(V_{OUT1} + \frac{V_{X1}}{A} \right), \quad C_F = 3C'_S + C'_F$$

$$V_{EST2} = \frac{1}{1 + \frac{1}{T_2}} \cdot \left(\frac{C_F}{C'_F} \cdot \left(\frac{Q_{RES1}}{C_F} \right) + K_2 \cdot V_{REF} \right) \quad (5)$$

$$T_2 = \frac{A \cdot C'_F}{3C'_S + C'_F + C_P}, \quad K_2 = \frac{C'_S}{C'_F} \cdot (D_{21} + D_{22} + D_{23})$$

Finally, the second residue output sampled by capacitive DAC (C_{SAR}) is created during phase 5. Regardless of an existence of C_{SAR} , gain error is calibrated by the square of T_2 (6).

$$V_{OUT2} = \left(\frac{2 + \lambda_2 + T_2}{1 + \lambda_2 + T_2} \right) \cdot V_{EST2} \approx \frac{1}{1 + \frac{1}{T_2^2}} \cdot \left(\frac{C_F}{C'_F} \cdot \left(\frac{Q_{RES1}}{C_F} \right) + K_2 \cdot V_{REF} \right) \quad (6)$$

$$\lambda_2 = \frac{1}{C_{CLS}} \cdot \left(C_{SAR} + \frac{C'_F \cdot (3C'_S + C'_P)}{3C'_S + C'_F + C_P} \right)$$

C. CLS gain-error calibration

According to the simulation result in Fig.6, the CLS gain error calibration alleviates the gain requirement of the amplifier as a square times of loop gain. Equation (7) describes the loop gain which is sensitive on internal parasitic capacitance in the switched capacitor feedback network. The parasitic capacitor (CP) is directly proportional to the input transistor size (W/L) and is sum of gate-drain, gate-source capacitor and so on in Fig.6. In the saturation region, Cgs is much larger than the others, because the channel charge tends to lean toward the source terminal as shown in Fig.7.

$$\text{Loop gain (T)} = A \cdot \beta = \frac{A \cdot C_F}{C_F + C_S + C_P} \quad (7)$$

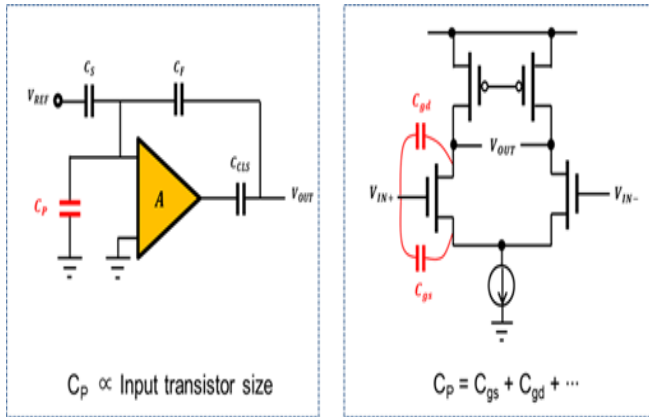


Figure 6. The internal parasitic capacitor of the amplifier

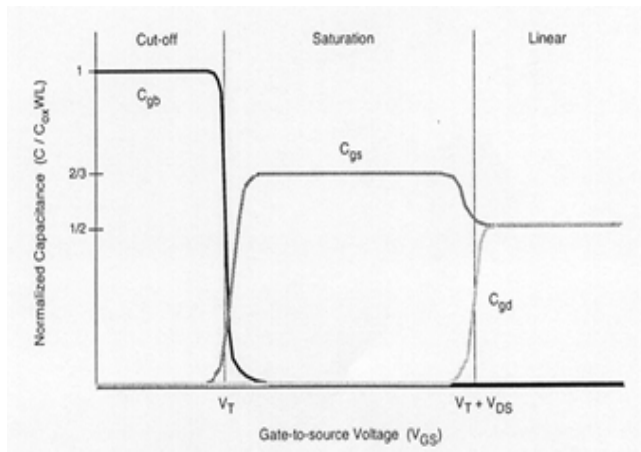


Figure 7. The internal capacitance of transistor depending on the operation mode

From the result of MATLAB simulation in Fig.8, the significant weakness of design exists in the parasitic capacitor coming from the amplifier input capacitor. The higher the value of \$C_p\$ is, the more number of tones that introduce non-linearity of ADCs is increasing. A huge size of input transistor is essential to increase bias current for wide bandwidth. However, if the \$C_p\$ is larger than roughly 50fF, the ADC accuracy is insufficiency to meet 9bit ENOB.

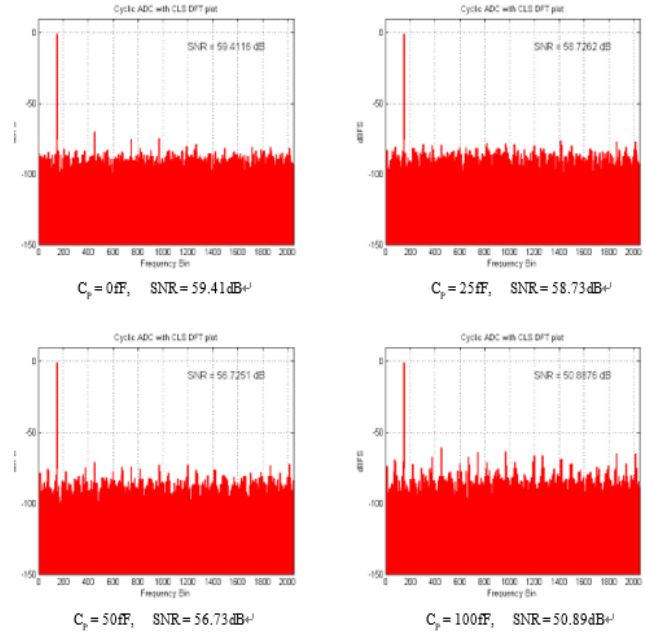


Figure 8. The effect on the variance of input parasitic capacitor

A pre-amplifier is used to enhance a little gain or prevent kickback noise, especially in prior part of a comparator with low power dissipation. In this work, a diode connected pre-amplifier works in order to overcome the limitation of CLS calibration about input transistor size while it complements the open loop voltage gain of the main amplifier. In Fig.9., a diode connected NMOS is in charge of an active load in the common source (CS) pre-amplifier. Equation (8) describes the pre-amplifier voltage gain demonstrated as the ratio of the trans-conductance between input transistor and active load in short. In the cadence simulation, the gain of first stage is about 2~3 times translated in 6~9 dB. Moreover, the input size of the main amplifier can be large due to the pre-amplifier without any loss of loop gain. As an additional feature, this amplifier does not require a miller compensation widely using two-stage amplifiers. Assuming that both of the two amplifiers are designed by similar specification, the first and second poles are very close in the frequency axis. On the other hand, the second pole of amplifier with diode connected pre-amplifier is far away from the first pole, because the resistance of the active load is far smaller than one of the output node. This amplifier maintains stable phase margin when the effective load capacitor to spread two poles. In CLS topology, CCLS capacitor performs a role of an adequate load.

$$A_V = -\frac{\sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_{D1}}}{\sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_2 I_{D2}}} \cdot \frac{1}{1 + \frac{g_{mb2}}{g_{m2}}} \approx -\frac{g_{m1}}{g_{m2}} \quad (8)$$

In this work, the performance of two stage amplifier with diode connected pre-amplifier is the unity frequency ($F_U=1.12\text{GHz}$), phase margin ($PM=50^\circ$) and power consumption ($P=1.02\text{mW}$). The gain variance of the full swing ($1.2V_{PP}$) is $33 \sim 35\text{dB}$ as shown in Fig 10. Also, switched capacitor common mode feedback (SC-CMFB) is used in this amplifier.

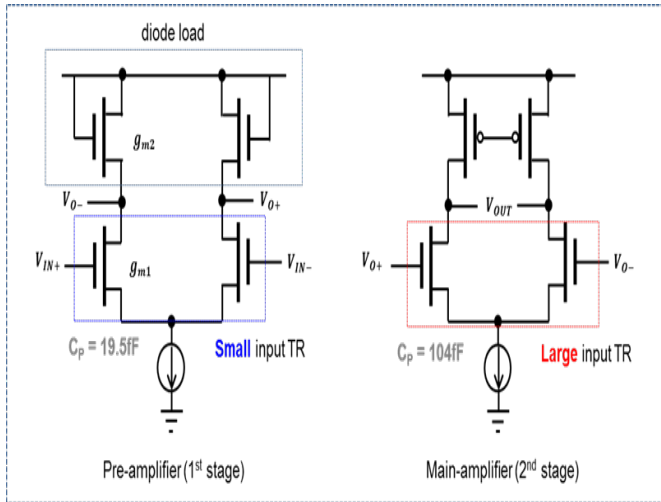


Figure 9. Two-stage amplifier with diode connected pre-amplifier

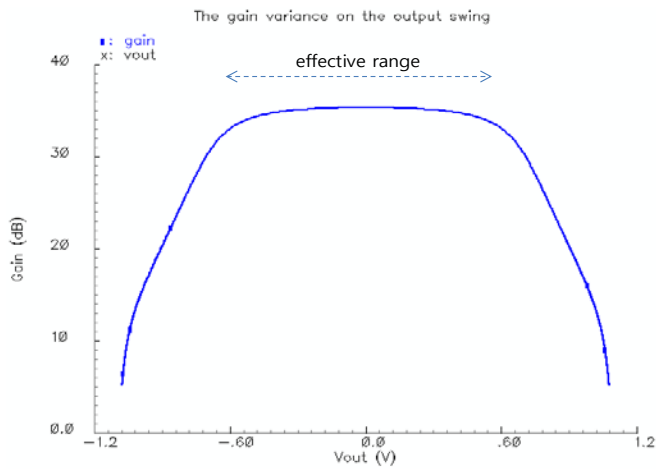


Figure 10. The gain variance on the output swing

D. Overall system diagram

The SAR-assisted cyclic architecture is composed of three time conversions to convert 10-bit resolution. In consideration of the each conversion, the requirement performance is different respectively. As shown in Fig.11. the first conversion has to own a process ability of 10bit accuracy unlike the second conversion is required for 8bit resolution. In spite of this reason, using the same scale of the circuit is an opposition to the power efficiency. Actually, the pipelined architectures that have several amplifiers scale down the individual stages by reducing the amplifier power and passive parts [10]. Unfortunately, the cyclic architecture

has only single amplifier. Nevertheless, the scale down of the cyclic converter is possible [11] with a capacitor sharing instead of a modification of the amplifier.

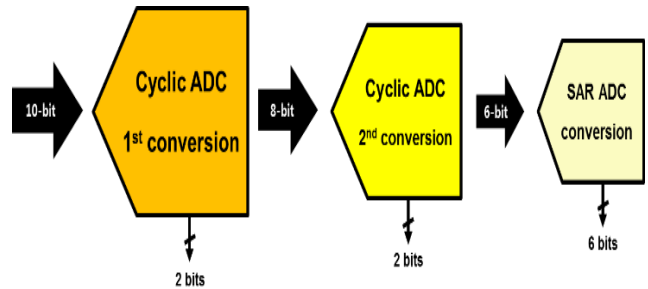


Figure 11. The design requirement of each conversion

Commonly, extra capacitors are necessary to sample a residue signal of cyclic ADC. Also, these capacitors are regarded as a load to the amplifier. In consequence of a normal MDAC process, a charge stored at both nodes of the feedback capacitor is perfectly equal to the one of the load capacitors in the ideal condition. The bottom plate of the feedback capacitor is connected to the output node and the voltage of the top plate is almost ground owing to the virtual ground property. That is why the feedback capacitor can successfully substitute the sampling capacitor for the following conversion.

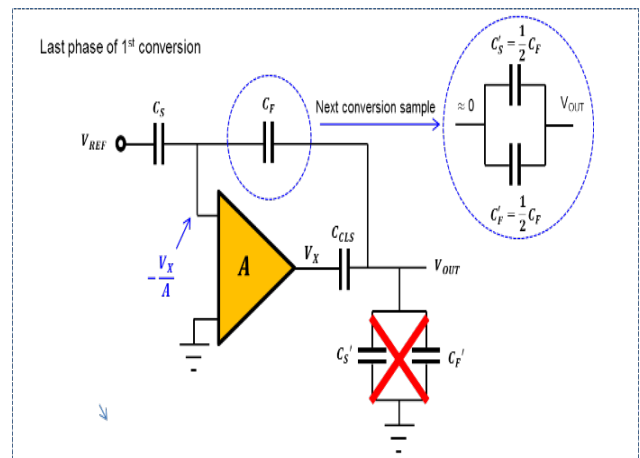


Figure 12. Feedback capacitor sharing topology

The basic concept of the feedback capacitor sharing is illustrated in Fig.12. The feedback capacitor is divided by next sampling capacitor and feedback capacitor equally. By using this technique, two advantages will be taken. First, the scaled down capacitors are effective to reduce the amount of total charge consumed for second cyclic conversion. Second, the amplifier is free to the load because of no additional capacitors. It also decreases the number of capacitors and some chip area. As a conclusion, the feedback capacitor sharing technique is reasonable for power efficiency.

Meanwhile, in the real condition, the amplifier input node is not completely virtual ground due to a leakage current by finite gain error. Thus, the accurate voltage of the top plate is $-V_X/A$ and the potential voltage of the feedback capacitor

is (9). Nevertheless, the gap between ideal and real condition is negligible due to the small swing of V_X . All the more, equation (8) subtracts a part of an additional error by $-V_X/A$, SNR is higher about 2dB in comparison of the normal MDAC operation in MATLAB simulation.

$$V_{OUT} + \frac{V_X}{A} \tag{9}$$

E. SAR operation using Cyclic-ADCs residue

The second residue voltage of the cyclic ADC is stored by the top plate capacitors of DAC using a bootstrap switch during phase 4 and 5 as shown in Fig.6. Total size of capacitor array is $32C_0$ in 6bit binary weighted DAC. Although a split capacitor DAC structure reduces the total capacitor size only roughly $16C_0$, it is very weak to parasitic capacitors especially of the LSB side without any parasitic compensation technique. However, the size of unit capacitor is allowed to be small as minimum capacitor in the CMOS process, because, this ADC is used for the last 6bit conversion. The size of MSB capacitor in the DAC, $16C_0$, is enough in spite of a capacitor mismatch issue. Generally, the capacitor mismatch of the latest CMOS technology is 0.1%. In terms of an amplifier, the capacitor array is regarded to a load capacitor reducing the bandwidth, so the minimum size is recommended as much as possible. Since the SAR conversion is implemented from the first phase to the third phase, total 12ns, the conversion time of 6bit SAR ADC is sufficient.

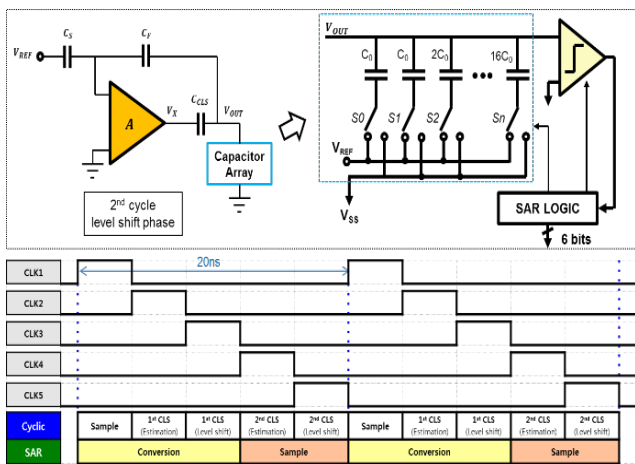


Figure 13. The block of second stage SAR ADC

There is one caution point. When the DAC array is connected to the output node, the anticipated sample signal is the one of 5th phase, second CLS level shift. Nevertheless, the DAC array has to be connected during the second estimation phase (ϕ_4) and second level shift phase (ϕ_5), because the precise gain error calibration is not possible if the CLS estimation occurs without the DAC array. In other words, the charge of CCLS transfers to the new load resulting in reduction of the equivalent gain when miss a connection of the DAC during phase 4.

III. RESULTS AND DISCUSSION

The Fig.14 is the photograph of the simulation layout. The blocks are arranged in cyclic ADC, SAR ADC, and sub flash ADC, preceded by the signal flow network and the amplifier is placed in the center. The chip size is 0.63×0.48 mm, about 0.3 mm^2 . The differential analog input signals enter from the top of the chip and digital outputs leave the chip from the left sides of the chip. The high speed (250MHz) input clock arrives in the clock generator which divides non-overlap 5 phases (50MHz).

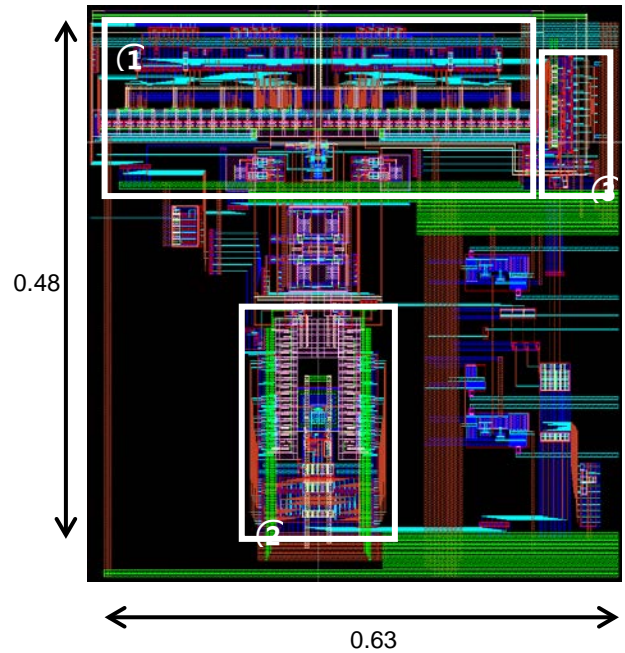


Figure 14. 0.18um CMOS layout ① cyclic ADC ② SAR ADC ③ Sub flash ADC

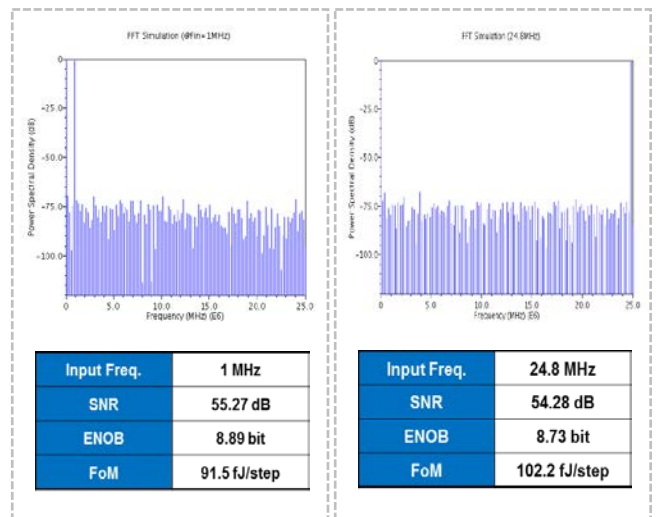


Figure 15. Simulated spectrum (at $V_{DD} = 1.2V$, $f_{in} = 1, 24.8 \text{ MHz}$, and $f_s = 50\text{MHz}$)

The ADC is simulated in 1-poly, 6-metal $0.11 \mu\text{m}$ CMOS technology with metal-insulator-metal (MIM) capacitor. Fig.5.2 shows the post-simulation spectrum of 1 MHz and 24.8 MHz inputs sampled at 50 MHz. The SFDR,

and SNR are 70 dB, 68 dB and 55 dB, 54 dB, respectively. The ENOB is approximately late 8 bits. The third tone is caused by non-linearity of ADC operation. The main source of the nonlinearity is supposed to be clock timing mismatch.

TABLE I. Simulation summary table

	Target	Design
Resolution	10bit	10bit
Conversion Speed	50 MS/s	50 MS/s
SNR	> 56 dB	55.27 dB
ENOB	> 9 bit	8.89 bit
Power Consumption	< 3 mW	2.17 mW
Chip Area	0.5 mm ²	0.3 mm ²
FoM	100 fJ/step	91.5 fJ/step

Table I. presents the simulated performance summary of this work. The accuracy of this ADC is insufficient on the target, more than 9 bit ENOB. The power efficiency and chip area are satisfied. The digital and analog power consumption is 1.08 mW and 1.07 mW, relatively and total power dissipation is 2.15 mW. The proposed SAR-assisted cyclic ADC has a FoM of 91.5 fJ/step with a 1.2 V supply.

IV. CONCLUSIONS

This paper proposes a new type of two-step A/D converter, which modifies cyclic ADC assisted by SAR ADC with CLS gain error calibration. The first cyclic ADC adopts 2 times 2.5 bit MDAC with only 34 dB of the amplifier gain for first 4 bits using CLS calibration. A diode connected pre-amplifier is suggested to the solution of input transistor size limitation of CLS technique. Besides, a feedback capacitor sharing technique helps efficient chip area and scale down of the second cyclic conversion. A second step ADC, asynchronous SAR ADC, generates last 6 bits with a simultaneous implementation to supports intrinsic low speed cyclic architecture and further saves the power dissipation.

The architecture achieves a medium resolution, moderate speed, low power and small area design requirements by complementing conventional cyclic and SAR architectures. The simulated design occupies 0.3 mm² of chip area and consumes only 2.15 mW static power, which changes to a FoM of 91.5 fJ/step.

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