In-Band Full-Duplex Transceiver Using Phase Locked Loop for Impedance Change Tracking

Yeong Seok Choi[1], Kun Hee Ha[2] and Choon Sik Cho[a]
School of Electronics and Information Engineering, Korea Aerospace University
E-mail : [1]ivory9675@naver.com, [2]yo0600@kau.kr

Abstract **- This paper describes the design of an integrated in-band full-duplex transceiver using phase locked loop. Generally, the transmission signal leakage to the receiver is detected in a transceiver with a single antenna. In order to minimize the signal leakage, a method of isolation between the leakage signals from the transmitter and the receiver is adopted. We suggest a method of impedance change tracking based on phase locked loop system, which can maintain high isolation between the transmitter and the receiver. Phase locked loop is therefore employed to sense the transmitter leakage and tune the impedance of the balance network. The TX port reflection coefficient of -29.65 dB at 1.95 GHz, the antenna port reflection coefficient of -28.09 dB, the RX port reflection coefficient of -26.41 dB, TX insertion loss of -11.58 dB, -45.2 dB the results of TX-RX isolation were obtained through measurements. The proposed circuit is fabricated in the area of 4mm x 4mm.**

Keywords **— Duplex Transceiver, Phase Locked Loop (PLL)**

I. INTRODUCTION

The development of wireless communication systems and the diversity of wireless communication technologies are increasing exponentially. However, Radio frequency resources are becoming increasingly depleted worldwide. A full duplexer has been commonly used in frequency division duplex (FDD) system to isolate the transmitter and the receiver while sharing the same antenna. However, because of the bandwidth limitation, integrating transmitter and receiver bands are considered as an important assignment. The integrated duplexer can reduce the bandwidth requirement and also maintain high isolation between the transmitter and the receiver. RF duplexer using a hybrid transformer and tunable CMOS integrated duplexer based on impedance tracking have been demonstrated [1, 2].

In this paper, an impedance tracking system based on phase locked loop (PLL) which can measure the transmitter leakage and tune the impedance of the balance network is suggested as shown Fig.1.

a. Corresponding author; cscho@kau.ac.kr

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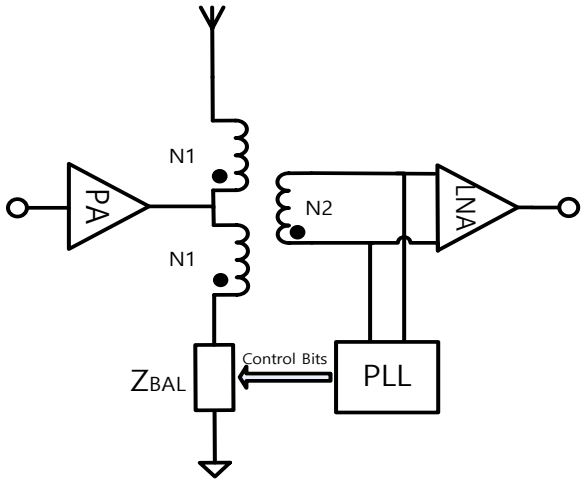

Fig. 1.The integrated full duplexer transmitter based on phase locked loop.

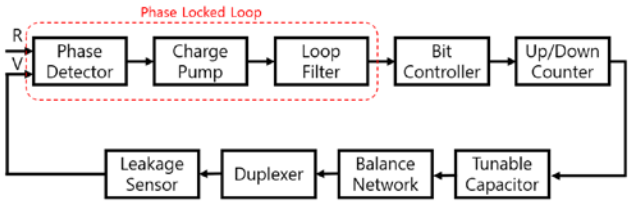

Fig. 2. Block diagram of the integrated full duplexer transmitter based on phase locked loop.

II. EXPERIMENTS

A block diagram of the integrated full duplexer based on phase locked loop is shown in Fig. 2. The self-interference signal received from the antenna is detected by a leakage sensor and a Phase/Frequency Detector(PFD). The PLL, which consists of PFD, Charge Pump, and Loop Filter transmits the sensed signal to the Balance Network, which generates the impedance equal to the impedance of the antenna and tracks the impedance of the antennas. Due to interactions between the user and the antenna, as the capacitance seen at the antenna varies, transmitter leakage increases. The transmitter leakage is shown in Fig. 3 and Fig. 4. Using the phase of transmitter leakage, the varactor determines whether to increase or decrease the capacitance in the balance network.

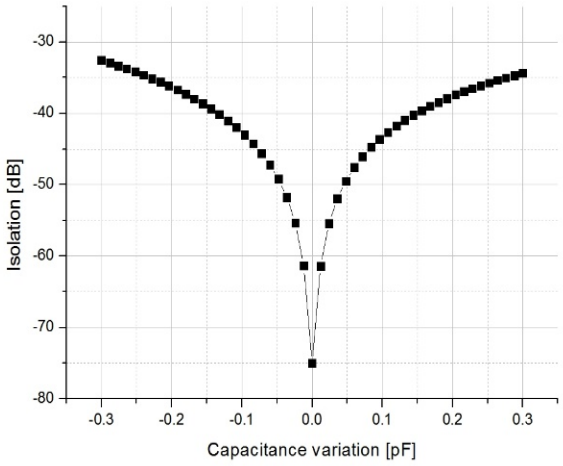

Fig. 3.Isolation between TX and RX by antenna capacitance variation.

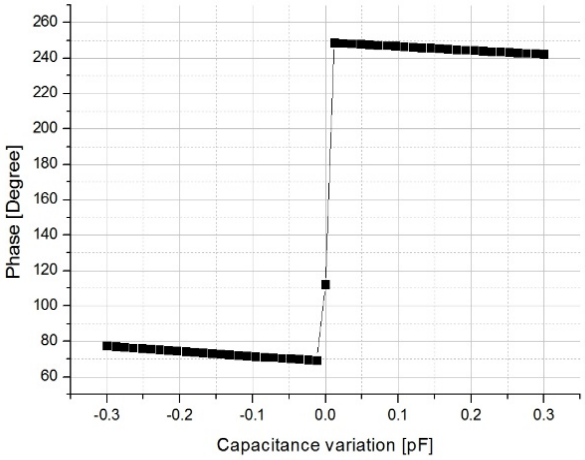

Fig. 4. Phase of the transmitter leakage by antenna capacitance variation.

A. Phase Detector

The phase detector consists of two D-flip flops (D-FF), one NAND gate, and several inverters refining the signals as shown in Fig. 5. D-FF detects the rising edge which can represent the phase of signal as described in Fig. 6. When both D-FFs are set, the value will be reset. The difference between the rising edges of transmitter leakage signal and the reference signal is transported to the charge pump.

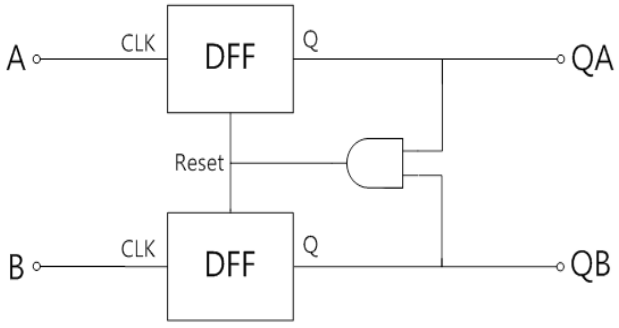

Fig. 5. Block diagram of the phase detector.

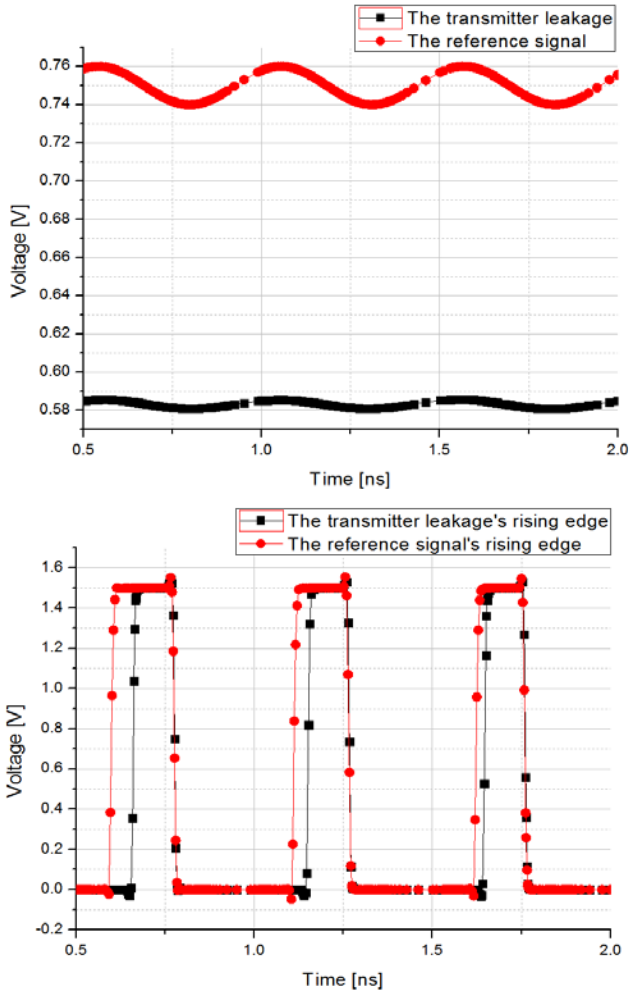

Fig. 6. Input and output voltages of the phase detector.

B. Charge Pump and Loop Filter

A charge pump detects the difference between the rising edges of transmitter leakage signal and the reference signal and adjusts the control voltage by charging or discharging the capacitor of loop filter as shown in Fig.7. A loop filter plays the role of a low pass filter (LPF) and a charge collector.

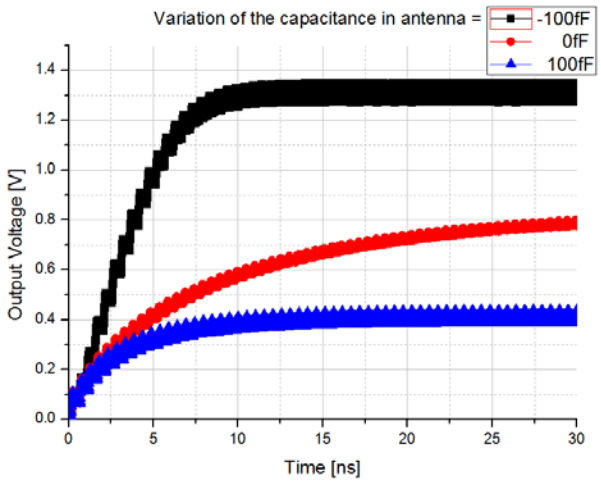

Fig. 7. Output voltage of charge pump and loop filter.

C. Bit Controller

Bit controller consists of six inverters, one NAND gate and one NOR gate as shown in Fig. 8. Two inverters in front divide the input voltage into three parts as shown in Fig. 9. And the NAND gate, the NOR gate and rest of the inverters determines whether to increase, decrease or maintain the control bits.

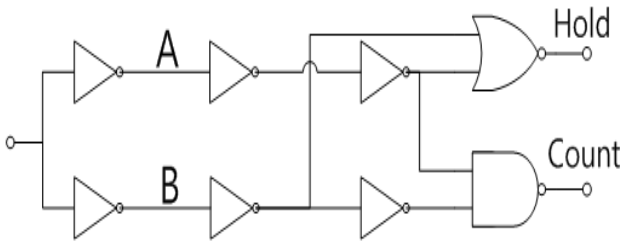

Fig. 8. Block diagram of Bit Controller.

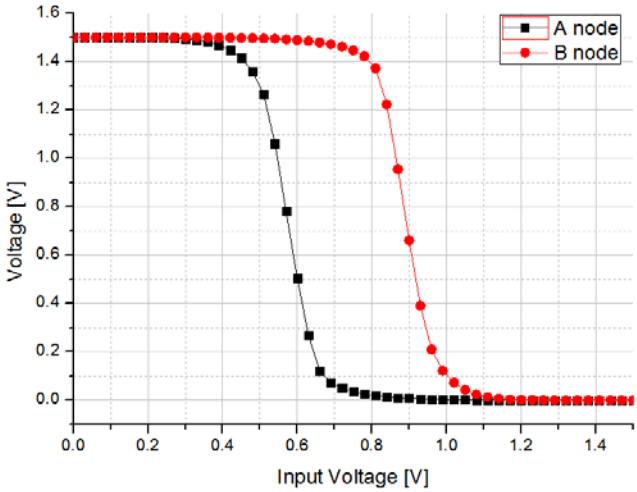

Fig. 9. Three parts of the input voltage at A and B node.

D. Up/down Counter

Up/down counter consists of three JK flip-flops, four NOR gates, four AND gates and two inverters as shown in Fig. 10. According to COUNT bit, control bits increase or decrease, and HOLD bit maintains the control bits.

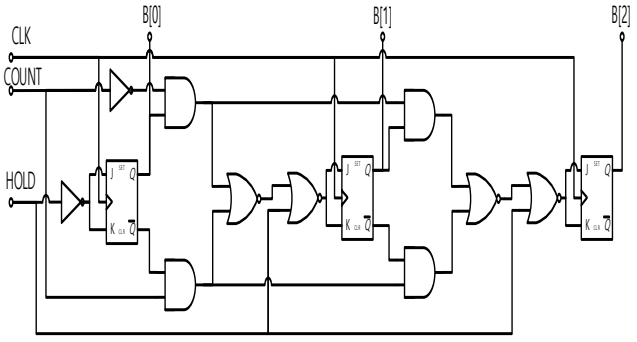

Fig. 10. Block diagram of Up/down counter

E. Tunable Capacitor

Tunable capacitor is placed in the balance network and the unit of tunable capacitor is 100fF as shown in Fig. 11.

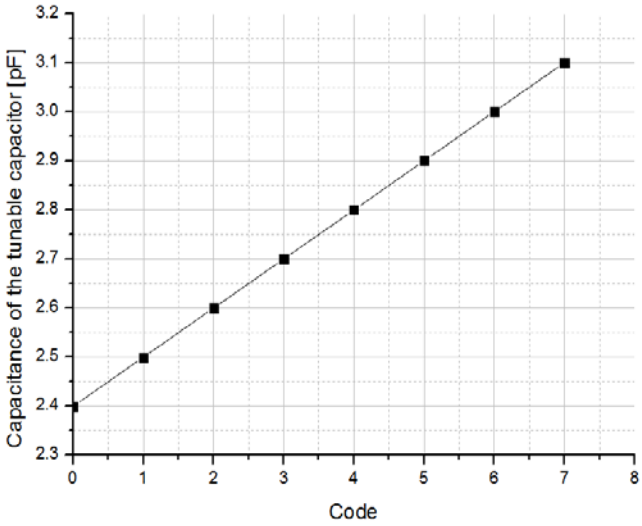

Fig. 11. Tunable capacitor with 100fF/step.

By the variation of the capacitance in antenna, the isolation get poor. But PLL system tracks the impedance variation of the antenna, therefore maintain high isolation between the transmitter and the receiver as shown in Fig. 12 and achieves average isolation of 65.5 dB and power consumption of 321.5 uW.

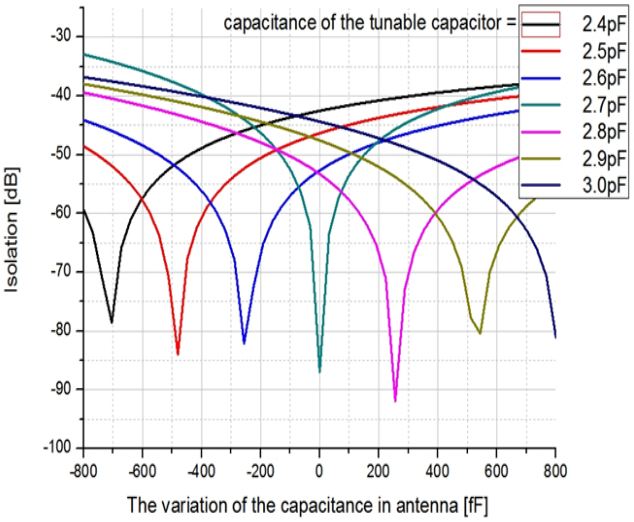

Fig. 12. Isolation by the variation of the capacitance in antenna.

The proposed in-band full duplexer has been fabricated in 65nm RFCMOS process as shown in Fig. 13. The designed chip is wire-bonded and connected on PCB to the test equipment for providing the input signal and measuring the leaked signal. The PIFA model consisting of passive elements and leakage cancellation transformer are located outside the chip and soldered on PCB as shown in Fig. 14. The designed full duplexer has been tested by varying the capacitance value of PIFA model which is chosen to be 2.7 pF initially.

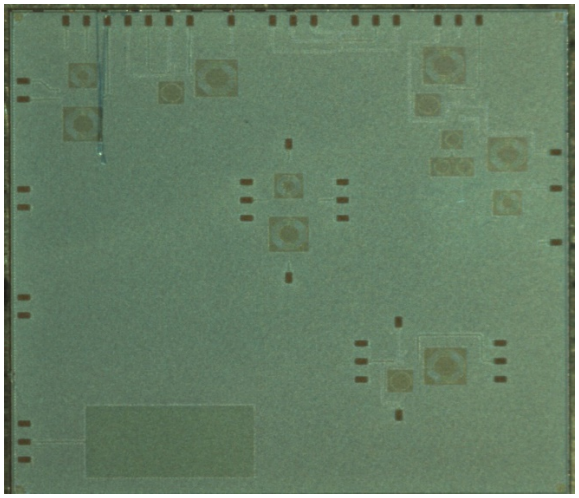

Fig. 13. The microphotograph of fabricated full duplexer.

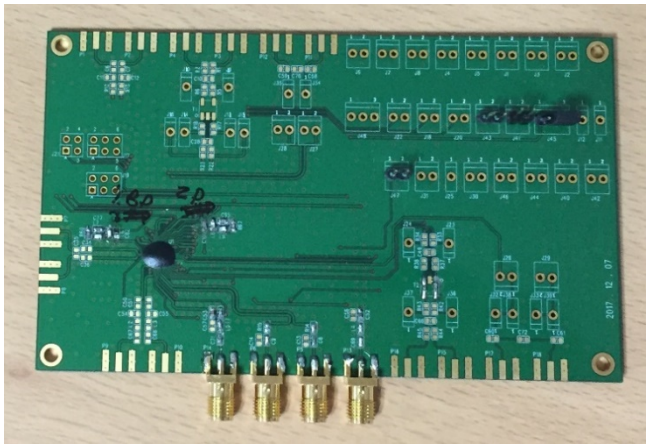

Fig. 14. The photograph of fabricated PCB.

Measured performances for insertion and return losses at the transmitter and receiver ports are illustrated along with return loss at the antenna port and isolation as shown in Fig. 15. The bandwidth of isolation with respect to over 40 dB shows 14 MHz at the center of 1.95 GHz.

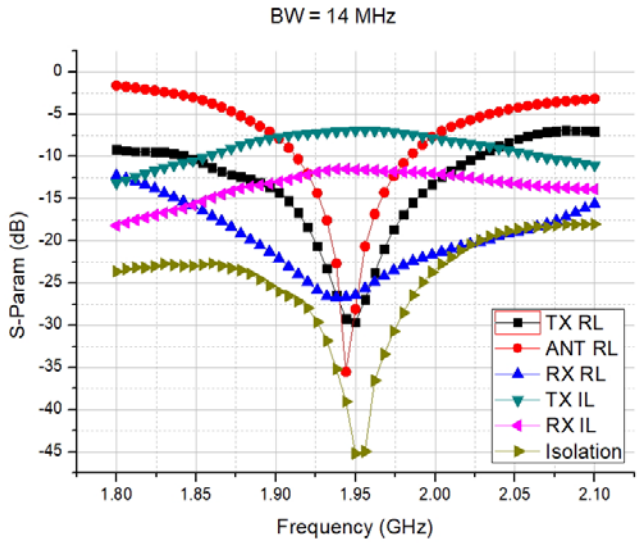

Fig. 15. Measured results for insertion loss, return loss and isolation.

III. CONCLUSION

An integrated full duplexer transceiver based on phase locked loop detects and tracks the impedance variation of the antenna and maintains and even improves isolation between the transmitter and the receiver. The TX port reflection coefficient of -29.65 dB at 1.95 GHz, the antenna port reflection coefficient of -28.09 dB, the RX port reflection coefficient of -26.41 dB, TX insertion loss of -11.58 dB, -45.2 dB the results of TX-RX isolation were obtained through measurements.

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REFERENCES

[1] M. Mikhemar, H. Darabi, and A. Abidi, ″An on-chip wideband and low-loss duplexer for 3G/4G CMOS radios,″ IEEE VLSI Circuits Symp., 2010, pp. 129–130.

[2] Sherif H. Abdelhalem, Prasad S. Gudem, Lawrence E. Larson, ″Tunable CMOS integrated duplexer with antenna impedance tracking and high isolation in the transmitter and receiver bands,″ IEEE Trans. Microw. Theory Techn., Vol. 62, No 9, Sep 2014.

[3] Kevin R.Boyle, Yun Yuan, Leo P. Lighthart, ″Analysis of Mobile Phone Antenna Impedance Variations With User Proximity″, IEEE Trans. On Antenna Prop., Vol. 55, no. 2, pp. 364-372, 2007.

[4] T.Dinc, A. Chakrabarti, H. Krshnaswamy, ″ A 60GHz CMOS Full-Duplex Transceiver and Link with Polarization-Based Antenna and RF Cancellation″, IEEE J.Solid-State Circuits, Vol. 51, no. 5,pp. 1125-40, 2016.

[5] B. Razavi, RF Microelectronics, NJ, Englewood Cliffs: Prentice-Hall, 1998.

Yeong Seok Choi received the B.S. and M.S. degress in electronics and information engineering from Korea Aerospace University, Goyang, Korea, in 2011 and 2019, respectively.

His current research areas are RF circuits for wireless communications and integrated circuit for FMCW radar transceiver.

Kun Hee Ha received the B.S. degrees in electronics and information engineering from Korea Aerospace University, Goyang, Korea, in 2019 and is currently working toward the M.S. degree. His current research area are RF circuits for wireless communications and integrated circuit for FMCW radar transceiver.

Choon Sik Cho (S′98–M′99) received the B.S. degree in control and instrumentation engineering from Seoul National University, Seoul, Korea in 1987, the M.S. degree in electrical and computer engineering from the University of South Carolina, Columbia, in 1995, and the Ph.D. degree in electrical and computer engineering from the University of Colorado at Boulder, in 1998. From 1987 to 1992, he was with LG Electronics, where he was involved with communication systems. From 1999 to 2003, he was with Pantec & Curitel, where he was principally involved with the development of mobile phones. In 2004, he joined Korea Aerospace University, Goyang, Korea. His research interests include the design of RF circuits and systems, especially for power amplifiers, transceivers, radar systems, and antenna integrated millimeter-wave systems.