A 1Gbps reference-less clock and data recovery using injection phase locked loop

Soo Wan Jin[1], Chang Zhi Yu, Dae Wung Lee, Jung Bin Lee and Jin Wook Burm
Department of Electrical Engineering, Sogang University
E-mail : [1]jinsw1122@sogang.ac.kr

***Abstract* – Injection Locking Phase-Locked Loop (IL-PLL) technique applied to 0.7 ~ 1.3Gb/s Clock and Data Recovery (CDR) is presented in this paper. Conventional CDR implemented by adding a Frequency Locked Loop (FLL) in a PLL in order to achieve a sufficiently large dynamic range. The proposed structure achieves wide input data rate range and low power consumption by implementing a FLL with digital circuits. A PLL to recover the clock and data was implemented digitally. The advantage of digital circuit design is a small area, low power and the ease of re-design. The proposed reference-less CDR is implemented in Magna Foundry 0.18um CMOS process. The measurement result is that the phase noise is about -108.57dBc/Hz at 1Mhz offset. The area of chip is a 0.55mm^2 and the power consumption with 1.8V supply voltage is 17.5mW when CDR operate at 1Gb/s of input data stream.**

***Keywords*—Injection Locking Pahse Locked Loop : IL-PLL, Injection Locking Digital Controlled Oscillator : IL-DCO, Frequency Locked Loop : FLL, Gain Controller : GC**

I. INTRODUCTION

As the 4th industrial revolution develops(Augmented Reality and Virtual Reality etc..), high speed data processing capacity becomes necessary, and serial data communication system is developing. Also, in the past few decades, high speed serial communication has been increasingly applied to various systems of optical communication networks.

The increase of data rate in the communication system said that high speed transmission and reception are required. Of course, in the past, the burden on high-speed communication was reduced through multi-link, but the attention is getting less and more attentive due to the trend of lightweight system and low power consumption of the system. Therefore, the CDR circuit is a circuit for eliminate errors caused by noise and jitter those are caused during the transmission of high speed data.

Most conventional architecture of CDR is the PLL based CDR that seem to be like a PLL. In this structure, the phase difference between input data and Voltage Controlled Oscillator (VCO) output signal is reduced and fixed, and the recovered clock retime the input data. In the transceiver systems, the performance of the most transmitters defined the requirements of performance of receiver.

The lock time of PLL becomes more important recently in CDR system. For this reason, to reduce lock time, PLL using a new technique (injection type PLL) is being studied. In the past few years, in the CDR systems, tons of papers proposed CDR structure using IL-PLL to reduce locking time and simplify architecture.

This paper is organized as follows. Section II. Describes the proposed CDR, and the block diagrams. The measurement results are shown in Section III. Finally, Section VI shows the conclusions.

a. Corresponding author; jinsw1122@sogang.ac.kr

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II. PROPOSED CDR ARCHITECTURE.

A. Proposed CDR Architecture

Various architectures have been proposed to reduce the complexity of loop structure. One of them is IL-PLL. IL-PLL is a form that locks the phase by repeating the method of fixing again the phase of the edge part of the clock in accordance with the data edge and operating it again. Fig. 1 shows the conventional IL-PLL architecture.

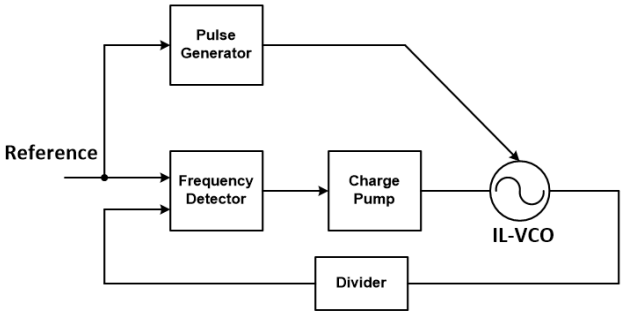

Fig. 1. Conventional IL-PLL Architecture

The operation of the IL-PLL is to lock the frequency using the conventional FLL structure and then phase lock the phase part by applying an injection pulse to the injection VCO (IL-VCO). The advantage of IL-PLLs is that it reduces data loss, since phase lock time is greatly reduced. In addition, the PLL

loop configuration is unnecessary. But to get a high performance IL-PLL, the high performance FLL is needed.

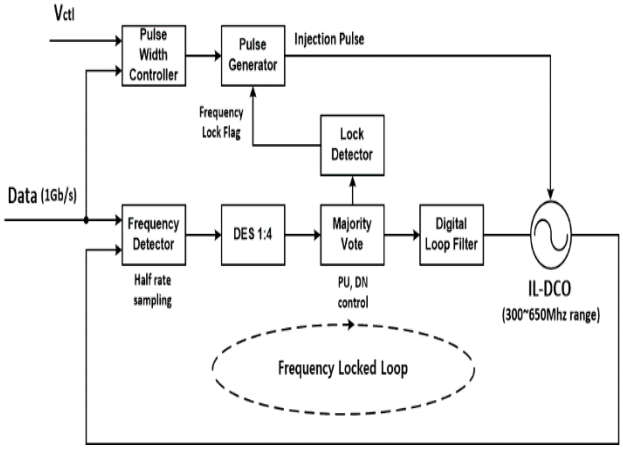

Fig. 2. Proposed Clock and Data Recovery Architecture.

The proposed Clock and Data Recovery is shown as Fig. 2. The architecture is different with other conventional dual loop CDR. The conventional CDR have 2 loop which are Phase Lock Loop and Frequency Lock Loop. So each loop needs a Gain Controller to phase or frequency lock and a Loop Filter. The proposed CDR do not need a loop filter to lock phase. Only the pulse generator to operate injection PLL is needed. So it can be reduce the total area and power consumption. To be phase locking for wide range, the injection lock loop need to control the pulse width. The pulse width made by pulse generator can be controlled by Vctl.

The FLL consists of conventional architecture. The frequency detector type is Bang-Bang Phase and Frequency Detector. DES is Deserializer which change the form of the input data stream to 4 bit data stream. Through majority vote and Digital Loop Filter, the IL-DCO is controlled. If the FLL is the lock state, the Lock Detector block make the Lock flag go high level to operate IL-PLL. To generate the injection pulse, the proposed architecture has a unique algorithm which is introduced later.

B. Pulse Generator

The Pulse Generator in proposed design can control pulse width by input voltages (INP and INN). The pulse generator schematic is shown as Fig. 3. To control the pulse width, the differential voltage input is needed.

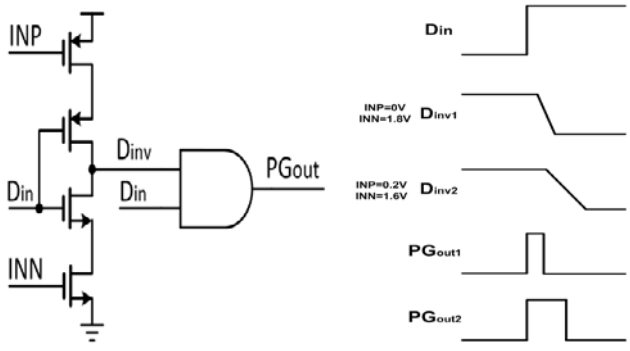

Fig. 3. Pulse Generator Schematic and Timing Diagram

The INP and INN have fully differential voltages controlled by external voltages. If the INP is higher than 0 voltage level, the pulse width become wide. In same reason, if the INN is lower than 1.8V voltage level, the pulse width become wide. The Fig. 3. Shows also timing diagram of pulse generator operation. The timing diagram in the Fig. 3 shows the variation of the injection pulse width according to the input voltages.

Fig. 4 shows a simulation result of the variation of the locking range according to the pulse width. The graph shows the range in which the FLL is locked according to the pulse width at 500Mhz. The result of the graph shows that the error occurred from wide injection pulse width can mistake a decision that the FLL is locked.

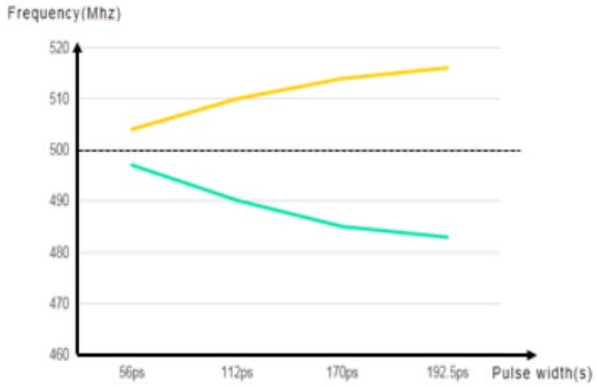

Fig. 4. Locking range versus pulse width

C. 1:4 Deserializer

A SERDES interface is a way to connect data between other points. The goal for using this is to minimize the connection nets at each point. A Deserializer is a circuit that converts serial data into a parallel data stream at the receiver. Using SERDES circuit reduces the number of pins sending and receiving data, which helped to reduce the consumption cost. In proposed architecture, serial input data is composed of 4 parallel data streams through a 1:4 Deserializer. Fig. 5 shows a block diagram of the Deserializer used in proposed architecture.

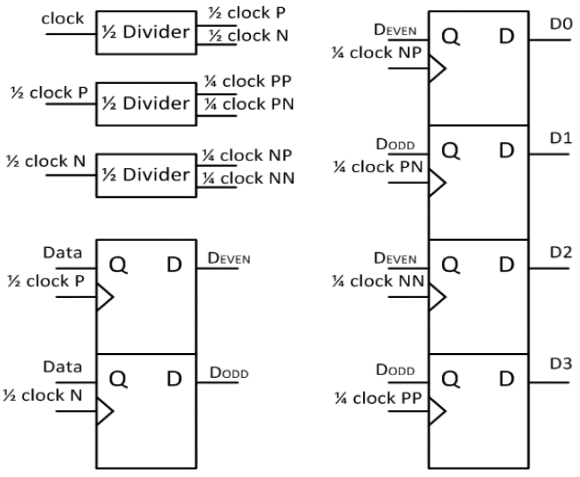

Fig. 5. 1:4 Deserializer block diagram

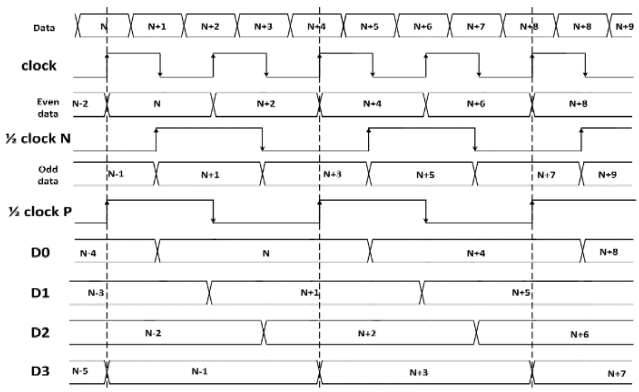

Fig. 6. 1:4 Deserializer timing diagram

Fig. 6 shows the timing data gram of the 1:4 Deserializer.

Deserializer operation is as follows. Divide the sampled data to even and odd using the Half-Rate sampling method. This division is called 1:2 Deserialization. Devide the clock by rising and falling again. A circuit that can sample four data by using the generated clock is implemented. The period of data Deserialized is increased four times from original data´s period. If data is sampled at point as shown in the dotted line again, the circuit get 4 parallel data stream.

The advantage of Deserialization is to quadruple the clock cycle, reducing the data rate. It ensures stability in subsequent circuit operations. However, changing the data rate to 1/4 causes the latency of the loop. It degrades the performance of the circuit in the feedback loop system. Therefore, it is best to use the deserializer circuit appropriately for each CDR for high performance.

D. Digital Algorithms (Mode Selection, Vote, Gain Controller, External Mode and Lock Detector)

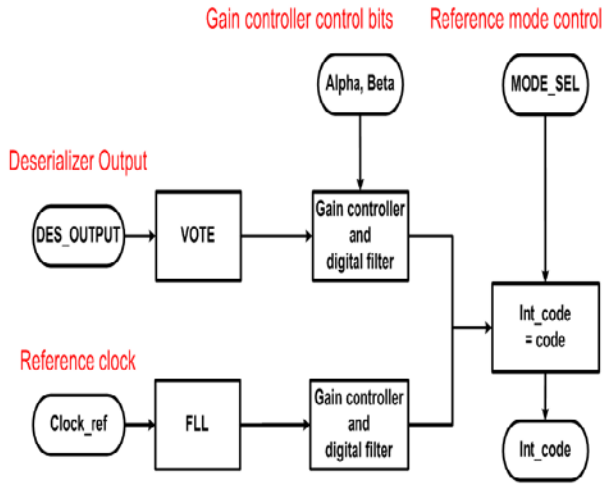

Fig. 7. Mode Selection Algorithm

The MODE_SEL bit is external control bit. If the MODE_SEL bit goes high level, the circuit select internal code that is output of Deserializer. IF the MODE_SEL bit goes low level, the circuit select reference code that is output of reference FLL. The circuit is implemented by synthesis and PNR.

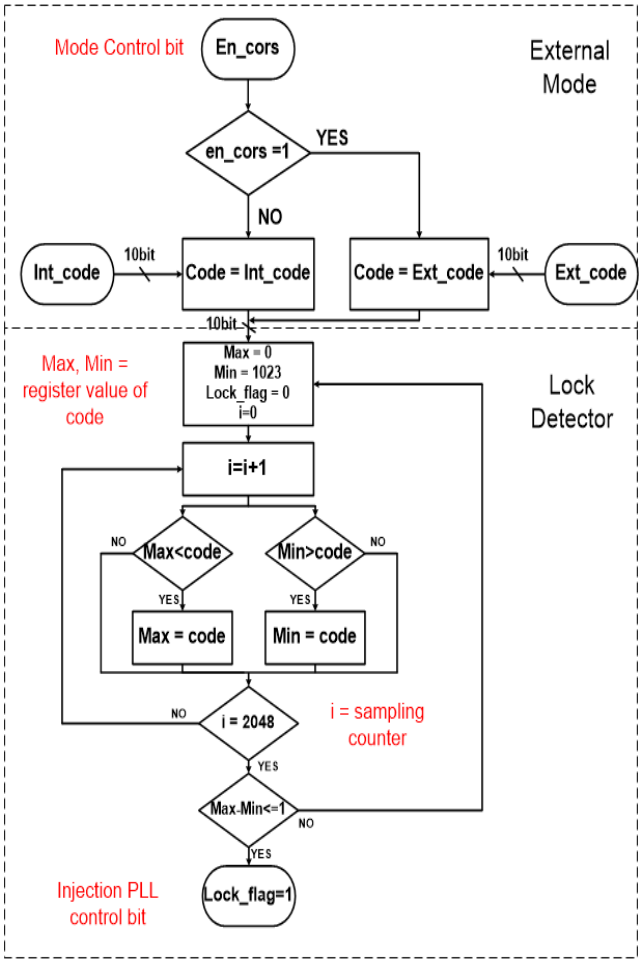

Fig. 8. External Mode and Lock Detector Algorithm

Fig. 8 shows the external mode and lock detector algorithms. The external mode is a block for verifying the performance of the DCO. It can be used to selectively confirm the DCO operating by externa and internal inputs. En_cors bit select the external or internal mode. The Lock Detector algorithms is a circuit for checking the lock state of the FLL. The operation of the lock detector is as follows. The total number of samplings time is 2048. Set the max and min variables to set the initial values to max is 0 and min is 2048(total 10bits). It is compared with input code 2048 times. After 2048 sampling, compare the difference between min and max. If the difference is less than 1, the lock detector decide that the FLL is lock state. The lock flag goes high level voltage. Since this means that the FLL is locked, it is a signal operating the PLL. The 2048 sampling time is that determine lock state. If it is determined that this is misunderstood and locked, the lock flag may become 1 even if it is not locked, and the error occurrence rate increases. In order to avoid these errors, the circuit will continue the comparison between 2048 times. As number of comparisons increases, the condition of the lock state becomes more accurate, so the probability of occurrence of error decreases. However, the smaller the number of comparisons, the shorter the lock time, but the probability that error will occur will increase. Due to such characteristics, an appropriate number of comparisons in necessary.

E. Digital Loop Filter

Fig. 9 shows the loop filter in proposed architecture.

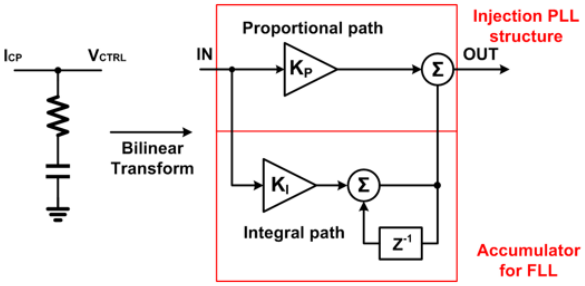

Fig. 9. Convert to digital loop filter by using bilinear transform

A 1st order analog filter is left side of the Fig. 7. Using bilinear transform, the 1st order analog filter covert to digital filter. There are two type paths in loop filter: proportional path and integral path. In conventional CDR, the proportional path is used for PLL and the integral path is used for FLL. In proposed design, the proportional path is not needed by using IL-PLL. There for the filter using in proposed design is simplified.

The filter equation is shown eq. (1) ~ (4)

Analog Filter $$H(s) = \frac{V(s)}{I(s)} = R + \frac{1}{sC} \quad (1)$$

Bilinear Transform $$H(s) = \frac{2}{T_s}\frac{(1 - z^{-1})}{(1 + z^{-1})} \quad (2)$$

Digital Filter $$H(z) = K_P + \frac{K_I 1}{1 - z^{-1}} \quad (3)$$

The Kp is proportion path coefficient. Therefore the final equation is shown as eq. (4)

$$\text{Proposed filter} = H(z) = \frac{K_I 1}{1 - z^{-1}} \quad (4)$$

The digital filter has advantages of power consumption and area. The filter block can be digital synthesis and PNR technique. The integral gain can control by external controller to change loop coefficients(beta).

F. Injection Locked Digital Controlled Oscillator

Fig. 8 shows the Injection Locked Digital Controlled Oscillator(IL-DCO) architecture.

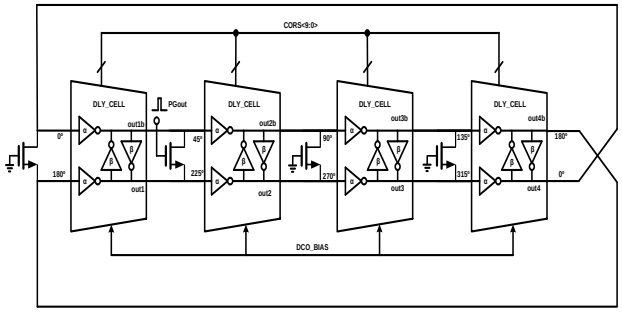

Fig. 10. Injection Locked Digital Controlled Oscillator

The Proposed IL-DCO is based by ring type Digital Controlled Oscillator(DCO). To get 8 kinds of phase, we use four delay cells(differential type). Each cell consists of latch and inverter. To control the digital controlled oscillator frequency range, we controlled the latch size ratio in the delay cell. To control the frequency, PMOS resistor Digital to Analog Converter(DAC) is needed. If the number of DCO current control bits increase, the DCO performance improve. The FLL performance in the IL-PLL is dominant. Increasing the resolution of DCO is important to improve the FLL performance. In typically, DCO performance is one of important things in CDR or PLL performance. To stable operation, the inverter and latch size ratio is 4:1. The switch is located between nodes that are 180 degrees out of phase to operate the IL-PLL. In consideration of the parasitic capacity that each node has, the dummy switches are added each nodes.

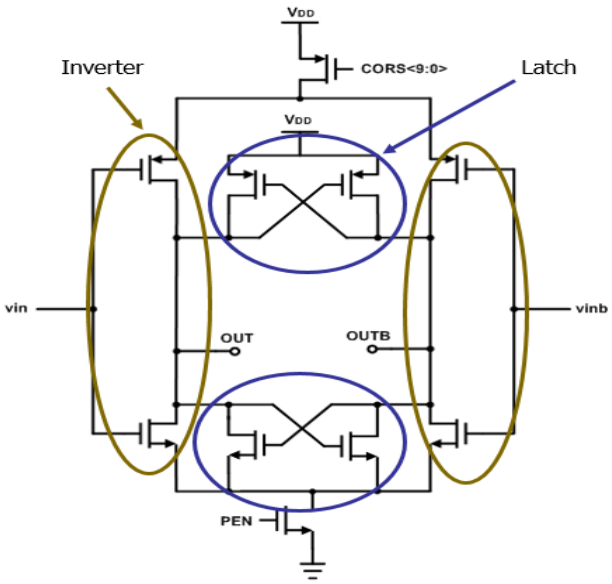

Fig. 11. One delay cell structure

Fig. 11 shows the Delay-cell structure. Each delay cell consists of inverter and latch as explained above. To get high resolution of DCO, the CORS bits is 10bits which control the frequency (195Khz/bit resolution). Total frequency cover range of DCO is 370~670 Mhz range. In the proposed design, the Fine control bits is not need because the IL-PLL is used for phase lock. PEN is a bias node to start operating DCO.

G. Design Flow

There are three parts of design levels

(1) Transistor level simulation

By using VIRTUOSO schematic editor of Cadence, we compose the schematic of transistor level and optimized the schematic with VIRTUOSO analog design environment. In the transistor level simulation, using HSPICE of Synopsys or Spectre of Cadence, the simulation will be detailed the circuit operation and performance.

(2) Physical design

The layout which is based on the schematic level is optimized by VIRTUOSO layout editor of Cadence and also verified by DRC and LVS simulation.

(3) Post layout simulation

The parasitic capacitance is not negligible in physical design level. This problem can solve by using STAR-RC XT of Synopsys. Therefore we can figure out parasitic capacitance and optimized layout level.

The design flow of overall circuit design using each design tool is shown Fig. 12.

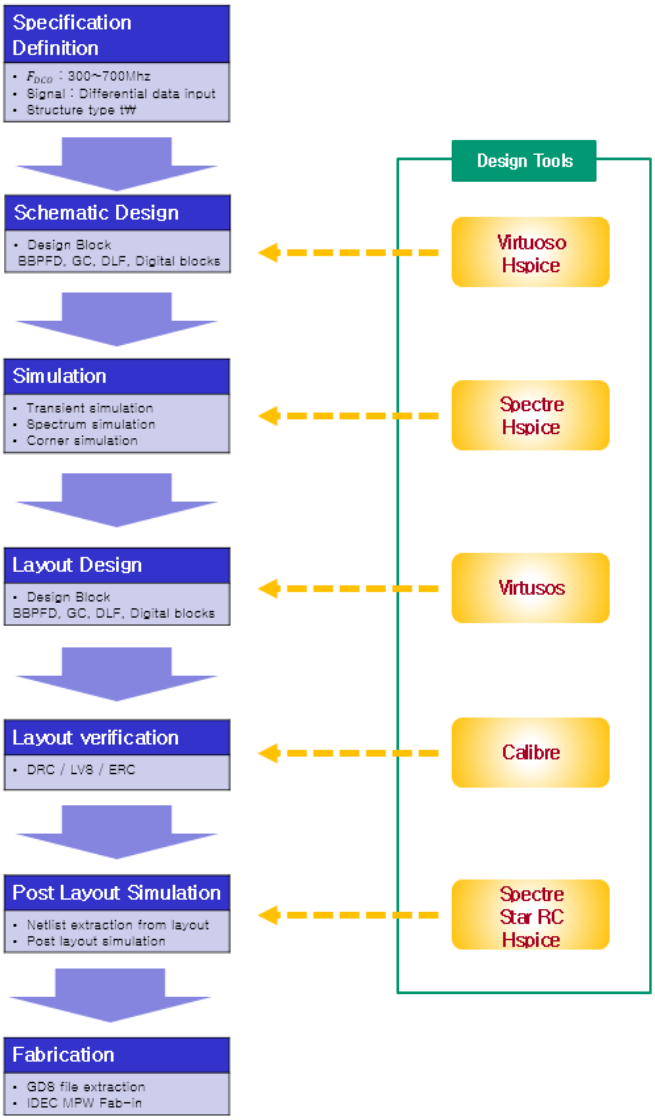

Fig. 12. Circuit design flow

This flow is very useful to any other design. First, we define the specification (architecture etc..). In second, make the block diagrams and schematics. In third, simulate and optimize each block. In forth, layout design and verification. In fifth, post layout simulation with netlist and parasitic resistance, capacitance. After all the simulations, fabricate the chip.

III. SIMULATION RESULT

A. FLL operation

The section III shows the simulation result of FLL and IL-PLL. When the CDR circuit starts, the FLL first operates for frequency locking. If the FLL operation is completed, the Lock Flag goes high level for phase locking. Fig. 13 shows the FLL operation.

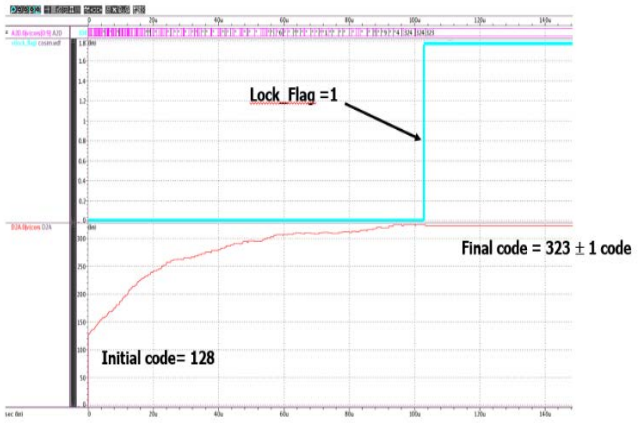

Fig. 13. FLL operation with Lock Flag

The initial code is 128 which is DCO control code. The 323 code means that the output frequency of IL-DCO is near the 500Mhz. If the DCO code keep the same code in long cycle, the Lock Flage bit goes high level. The FLL locked time is about 101.5us.

B. IL-PLL operation

Fig. 14 shows the IL-PLL operation.

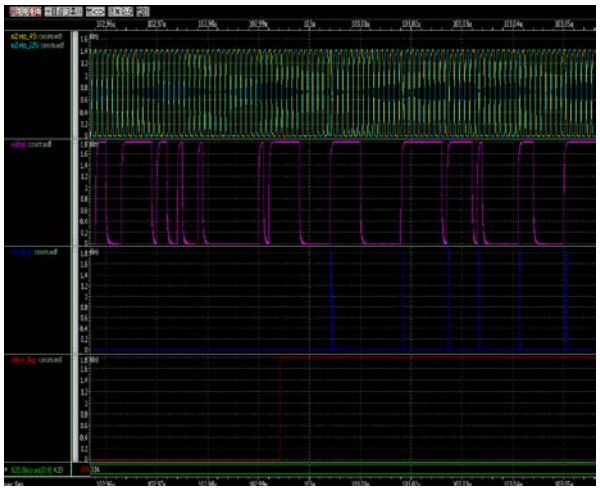

Fig. 14. Injection phase lock operation.

After FLL operation, the IL-PLL start operating. The injection pulse is generated every rising edge of input data bit when the Lock_Flage is high level. Before frequency lock, the injection pulse is not generate.

IV. MEASUREMENT RESULT

A. Chip Fabrication.

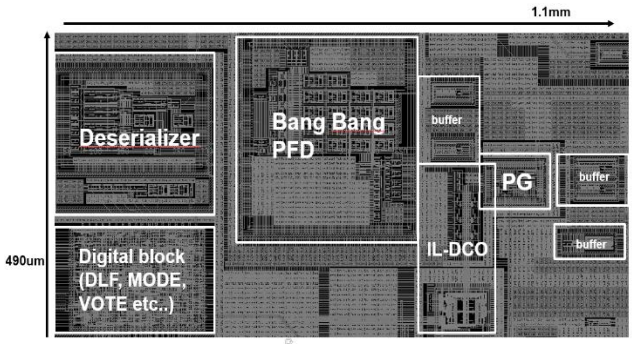

Fig. 15. Area of Fabricated Chip.

The proposed CDR circuit is designed using a Magna-chip 0.18um process. The layout of all the circuits is shown in Fig 15. The size of each block is shown. The total area of fabricated chip is 0.55mm^2. The total power consumption without buffer is 17.5mw when the power supply is 1.8V.

B. Operation of DCO.

Fig. 16 shows the DCO frequency Range. The measured frequency is 371Mhz when the cors bits is 0 and 670Mhz when the cors bits is 1023. It is in the range of 0.74 to 1.34Gb/s when converted to data rate(half rate sampling).

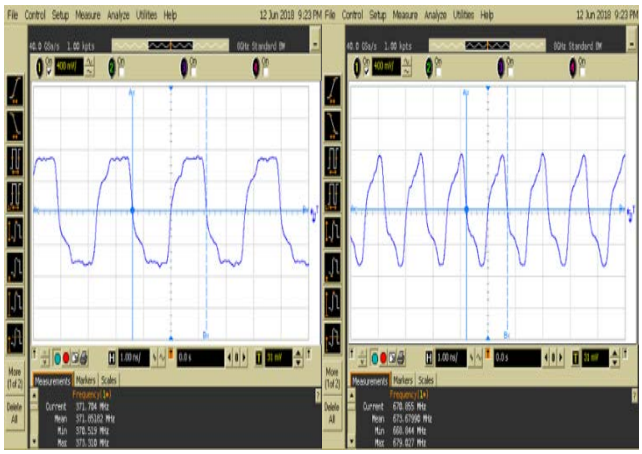

Fig. 16. Frequency Range of DCO

C. Operation IL-PLL.

Fig. 17 and 18 show spectrum and phase noise of DCO in phase lock state. Fig. 17 shows the spur in the phase lock state. It can be confirmed that an accurate tone occurs at the point corresponding to the target frequency (500Mhz). In the conventional PLL, the loop bandwidth is proportional to frequency of reference clock. By contrast in the case of the IL-PLL structure, about half of the reference clock frequency is loop bandwidth. So proposed CDR bandwidth is wider than frequency range of measurement equipment. Phase noise is about -108.57dBc/Hz at 1Mhz offset and about 99.47dBc/Hz at 100Khz offset. pulse width affects operation of FLL. The Lock Flag signal operates IL-PLL.

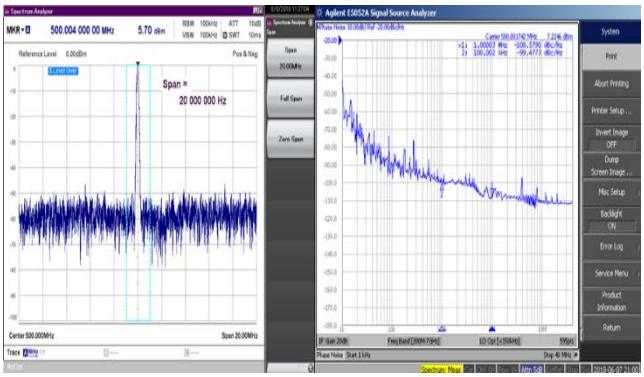

Fig. 17. Spectrum of IL-PLL Fig. 18. Phase noise of IL-PLL

Frequency ranges 300~700Mhz. The injection pulse made by pulse generator make the oscillator to be locking state. As the width of the injection pulse increases, even if the frequency is not in the locking state, it will cause an error as if there is a lock. When the injection pulse width becomes short, the operation of PLL is immediately stopped when the FLL is not in the lock state. However, as the width gets wider, frequency error can be covered a bit. Fig. 19 and 20 show the jitter according to the pulse width. The pulse width is adjustable through the voltage of VP and VN. Fig. 19 is in the case that VP is 0V and VN is 1.8V. Fig. 20 is in the case that VP is 0.1V and VN is 1.7V. The jitter is proportional to injection pulse width as shown in Fig. 19 and 20.

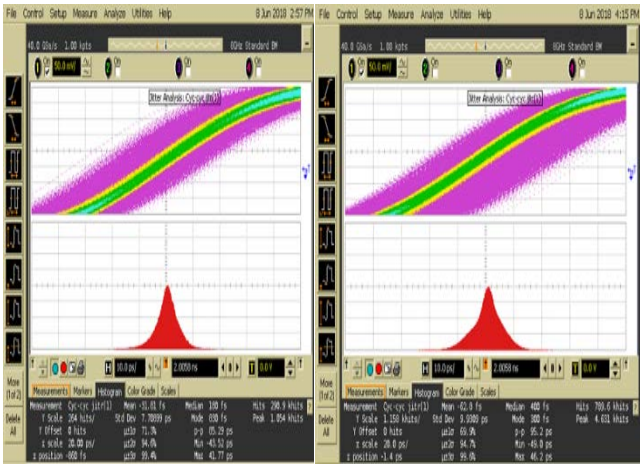

Fig. 19. Jitter (VP =0V, VN=1.8) Fig. 20. Jitter (VP=0.1V, VN=1.7)

D. Recovery Clock and Data.

The Fig. 21 and 22 show the clock and data according to the input data jitter. In general, data is transmitted by the transmission line with jitter and inter symbol interference noise. As a result, data generates loss and the sampling position is unstable. Therefore, the clock and data recovery circuit which is used for recovering clock. If the data without jitter is input, the CDR sample data without error. When data containing jitter is used as input, the CDR must have jitter tolerance. So it is to confirm the data sampling form by input jitter. Fig. 21 shows that the data without jitter.

Fig. 21. Recovered Clock and Data(None jitter)

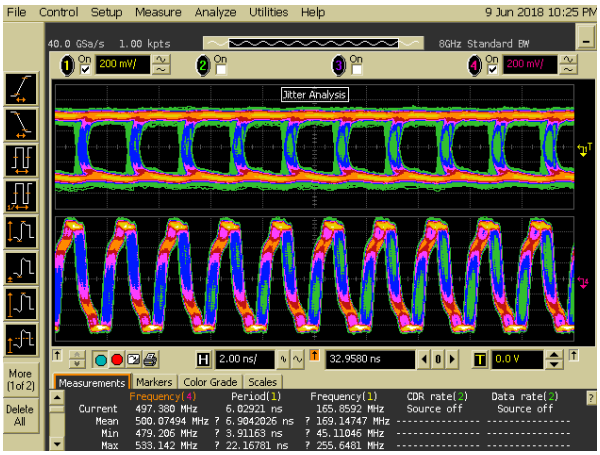

Fig. 22. Recovered Clock and Data(10Mhz offset, 0.22UI)

One reason why jitter occurs despite input without jitter is the injection pulse width, Jitter occurred in the recovered data due to the clock jitter caused by the IL-PLL operation.

Fig. 19 shows the result of sampling the data through recovered clock by input with 0.22Unit Interval (UI) jitter to 10Mhz offset.

As shown in Fig. 22, we recovered clock using data with jitter. The form of sampling the data using recovered clock creates an eye diagram with jitter.

TABLE I.
Comparison than other CDRs

	[17]	[18]	[19]	[20]	this work
Data Rate	2.0Gb/s	0.14~1.83Gb/s	0.18~3.3Gb/s	0.25~6.0Gb/s	1Gb/s
CDR type	Reference-less	Reference-less	Reference-less	Reference-less	Reference-less
Process	0.25um	0.25um	0.13um	65nm	0.18um
Phase Noise	N/A	N/A	N/A	N/A	-108.57dBc/Hz @1MHz
Oscillator type	Ring	Ring	Ring	Ring	Ring
RMS jitter	11ps	14.96ps	14.0ps	9.56ps	7.371ps
Peak-to-Peak jitter	N/A	N/A	116.0ps	57.5ps	85.29
Size	0.45mm²	N/A	N/A	0.0944	0.55mm²
Supply Voltage	3.0V	2.5V	1.2V	1.2V	1.8V
Power Consumption	90mW	N/A	75mW (180Mb/s)	13.2mW	17.6mW

The jitter performance generated by proposed design is less than other reference papers. The area of proposed architecture is including test pattern such as external mode and reference mode.

V. CONCLUSION

The proposed CDR consists of IL-PLL and conventional FLL. The IL-PLL architecture has reduced the phase locking time compared to using a conventional PLL. The Proposed architecture use the simple 1^{st}order loop filter by using only one loop(FLL). To increase the dynamic range of proposed CDR, the IL-DCO type is based on ring type oscillator. The Phase noise of designed DCO is about -62.56dBc/Hz at 1kHz offset in free-running state. The phase noise of designed DCO in phase lock state is about -108.57dBc/Hz at 1Mhz offset and about 99.47dBc/Hz at 100Khz offset. The clock rms jitter is 7.7ps and p-p jitter is about 85ps(using narrowest injection pulse width). The area of chip is a $0.55\,mm^2$. The power consumption with 1.8V supply is 17.5mW at 1Gb/s data rate.

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Soo Wan Jin was born in Eumsung, Korea in 1990. He received the B.S. degree in electronic engineering from Chungbuk University, Chungbuk, Korea, in 2015, and is pursuing the M.S. degree in electronic engineering from Sogang University in 2017. His current interests are in the design of integrated circuit, and high-speed interface applications

Chang Zhi Yu received his B.S. degree from Konkuk University, Seoul, in 2012, the M.S. degree from Sungkyunkwan University, Suwon, in 2014. He is currently working toward the Ph.D. degree in electronics engineering of Sogang University Seoul, Korea. His research interests include mixed-mode signal integrated circuit design and high-speed interface circuits.

Dae Wung Lee was born in Gunpo, Korea in 1988. He received the B.S. degree in electronic engineering from Korea Aerospace University, Gyeonggi, Korea, in 2015, and is pursuing the M.S. degree in electronic engineering from Sogang University in 2017. His current interests are in the design of integrated circuit, and high-speed interface applications.

Jung Bin Lee was born in Seoul, Korea in 1993. He received the B.S. degree in electronic engineering from Korea Aerospace University, Gyeonggi, Korea, in 2016, and is pursuing the the M.S. degree in electronic engineering from Sogang University in 2017. His current interests are in the design of Analog integrated circuit, and high-speed interface applications.

Jin Wook Burm was born in Korea in 1964. He received the B.S. degree in physics from Seoul National University, Seoul, Korea, in 1987, the M.S. degree in physics from the University of Michigan, Ann Arbor, in 1989, and the Ph.D. degree in applied physics from Cornell University, Ithaca, NY, USA in 1995. After postdoctoral work at Cornell University and Bell Labs, Lucent Technologies, Murray Hill, NJ, he joined Dept. of Electronic Engineering, Sogang University, Seoul, Korea as an Assistant Professor in 1998, where he is now a Professor. He also worked as a Principal Scientist at Pixelplus semiconductor Inc., San Jose, CA, USA for 1 year starting Aug. 2006. He worked on millimeter wave ICs and high speed GaN transistors at Cornell, and high speed optoelectronic circuits at Bell Labs. At Sogang University, his current research interest includes high speed interface circuits and CMOS implementation of various sensors.