A 4WP High Efficiency Wireless Power Transmitting Unit

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***Abstract* - This paper presents Power Managements IC for Power Transmitting Unit (PTU) of magnetic resonant A4WP application. A high efficiency Step-Up Converter with a programmable output is proposed to provide supply voltage to the external Power Amplifier (PA) with a peak power of 37.5 W. In order to implement the closed loop gain control function of the Power Trans mitting Unit (PTU) with the Power Receiving Unit (PRU), the duty cycle is controlled with the Pulse Width Modulation (PWM) signal from Bluetooth Low Energy (BLE).**

The chip is fabricated using a 0.18 μm BCD process with high power MOSFET options, and the die area is 2000 μm x 2000 μm. The measured maximum power efficiency of the Step-Up Converter and Step-Down Converter is each 92.8% at load current of 0.5 A and 93.8% at load current of 0.3 A. The output voltage of the Step-Up Converter ranges from 12 V to 25 V and that of the Step-Down converter ranges from 3.3 V and 5 V.

I. INTRODUCTION

Wireless Power Transfer (WPT) is a popular research area, especially for a mobile phone charger [1]. A rapid growth has been shown in the need for wireless battery charging systems for user convenience. Without an embedded battery, the receiver can only be activated when placed near the transmitter. With the inductive coupling method, the distance between the transmitter and receiver is limited because the power efficiency is drastically lowered when the distance is increased. The magnetic resonance method is an attractive solution, as the distance between the transmitter and receiver can be several meters [2]. Since the frequency of Alliance for Wireless Power (A4WP), a standard in magnetic resonance method, is 6.78 MHz, enhancing the DC-DC Converter efficiency, which is the largest portion of total efficiency of the transmitter, is a very challenging task. Especially, high voltage MOSFET should be used to supply high input voltage from adapter. However, there are some side effects which reduce the efficiency of the step up converter.

In this paper, by adopting both the PWM and PFM mode, the overall efficiency from light load to heavy load has been improved. The bootstrapping method has enabled Gate-to-Source Voltage (V_{GS}) of power MOSFET to maintain a sufficient margin to avoid the breakdown of High voltage MOSFET. Therefore, a wide range output of the Step-Up Converter and high efficiency of both the Step-Up Converter and Step-Down Converter can be achieved.

II. HIGH EFFICIENCY POWER MANAGEMENT IC FOR PTU OF A4WP APPLICATION

The PA operates at the frequency of 6.78 MHz in the A4WP system. The Step-Up Converter provides the high supply voltage to the PA. Its output voltage (STU_OUT) is controlled from 12 V to 25 V by the PWM signal through the Bluetooth Low Energy (BLE). STU_OUT is connected to the supply voltage of PA to adjust the output power level. 3.3 V and 5 V are needed for the supply voltage of BLE and PA, respectively. The V_{AD} voltage is 12 V from the external adaptor and is used for the 3.3 V and 5 V Step-Down Converter. The power efficiency of the transmitter is determined by these three DC-DC Converters. Therefore, they are integrated in the A4WP PTU IC to minimize the system cost and improve the power efficiency.

From Fig. 1, three power supplies are needed for transmitter and switching mode is used for high efficiency. Three types of DC-DC Converters are integrated to ensure low cost and to improve the circuit's integration. In the transmitter for A4WP, the power supply solution chip is designed into the PTU.

Fig. 1 shows the proposed top block diagram of the Power Managements IC for A4WP PTU. It is composed of a Step-Up Converter, a 3.3 V Step-Down Converter, a 5 V Step-Down Converter, Protection, Power Supply, and an Enable block. The 12 V input from the Adaptor is connected to the DC-DC Converters to generate the regulated output voltages of 3.3 V, 5 V, and 12 V ~ 25 V. The Low Pass Filter (LPF) is used to convert the PWM signal into the DC voltage (VC_{STU}). The VC_{STU} generated by LPF is connected to Feedback circuits in Step-Up Converter.

III. BUILDING BLOCKS

A. Step-Up Converter

Fig. 2 shows a block diagram of the Step-Up Converter. It

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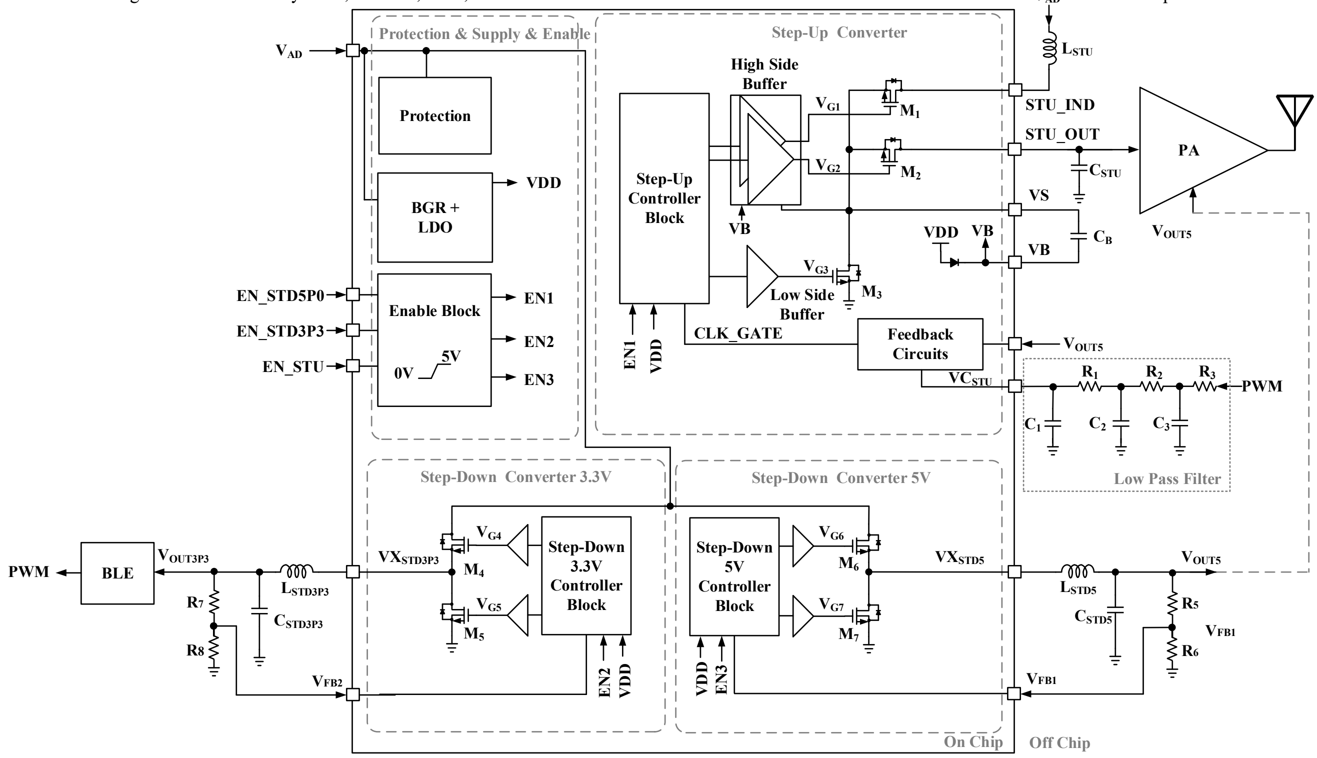


Fig. 1. Proposed top block diagram of the Power Managements IC for A4WP PTU.

senses the output voltage and regulates it over the wide output range using the high power LDMOS in the voltage mode. The synchronous type Boost Converter is implemented with the bootstrap circuit. The V_{AD} from the adaptor is applied to the Step-Up Converter to generate the regulated output of the DC-DC Converter.

In order to reduce the component size, the switching frequency is determined to be 500 kHz. The inductance and capacitance of 15 μH and 50 μF, respectively, are adopted.

Fig. 3 shows the proposed Soft-Start circuits in the Step-Up Converter. The Soft-Start circuit is designed to suppress the in-rush current of the Step-Up Converter. I_{SS} and the external capacitor, C_{S_STU}, determine the charging speed of the V_{SOFT} voltage. The V_{G1} voltage follows V_{SOFT} when V_{SOFT} is charged. When V_{SOFT} becomes higher than V_{SS_H}, V_{G1} follows VB. By slowly increasing the V_{GS} of M_1 as shown in Fig. 1, the in-rush current of the Step-Up converter can be reduced.

Fig. 4 shows the timing diagram of the proposed Soft-Start function. The Soft-start operation is started when the V_{SOFT} voltage is higher than V_{SS_L}, and is finished when V_{SOFT} becomes higher than V_{SS_H}. The V_{SOFT} voltage is applied to the high side driver when the SS_ON signal is high. On the contrary, when the SS_ON signal is low, the VB voltage is applied to the high side driver. The Soft start operation is necessary to protect IC by limiting the in-rush current.

Fig. 5 shows the proposed clock generator circuit. The proposed clock generator is composed of a sawtooth wave generating loop and duty ratio control circuit. The V_{SAW} voltage is charged by I_{SAW} and C_{SAW}. When V_{SAW} is higher than V_{SAW_R}, SAW_RE becomes high.

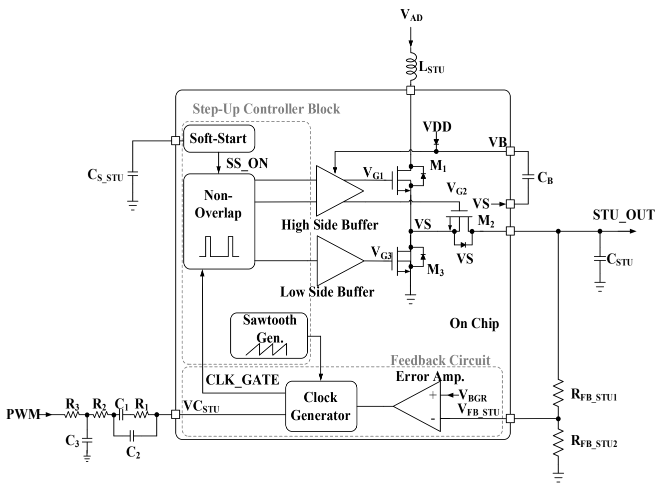


Fig. 2. Block diagram of Step-Up Converter.

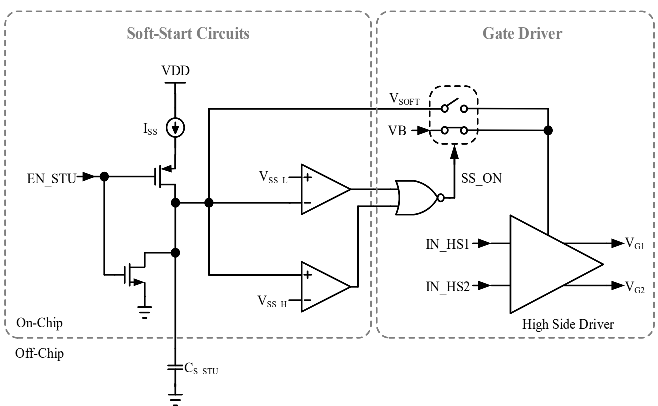


Fig. 3. Proposed Soft Start circuits of Step-Up Converter.

When SAW_RE is high, V_{SAW} is discharged and a sawtooth wave is generated. An inverter delay is added to guarantee the discharging time of V_{SAW}. The V_{SAW} voltage is compared to V_{SAW_L}, V_{SAW_H}, or VC_{STU}. To limit the switching duty ratio of the Step-Up Converter, a duty limiting circuit is added to limit the minimum duty or maximum duty. The V_{SAW_L} voltage is used to limit the minimum duty, while the V_{SAW_H} voltage is used to limit the maximum duty. When COMP1 and COMP2 are high, the CLK_GATE voltage becomes low.

Fig. 6 shows the timing diagram of the clock generator. When VC_{STU}, the feedback voltage of the Step-Up Converter, is lower than V_{SAW_L}, the minimum duty ratio of CLK_GATE is limited.

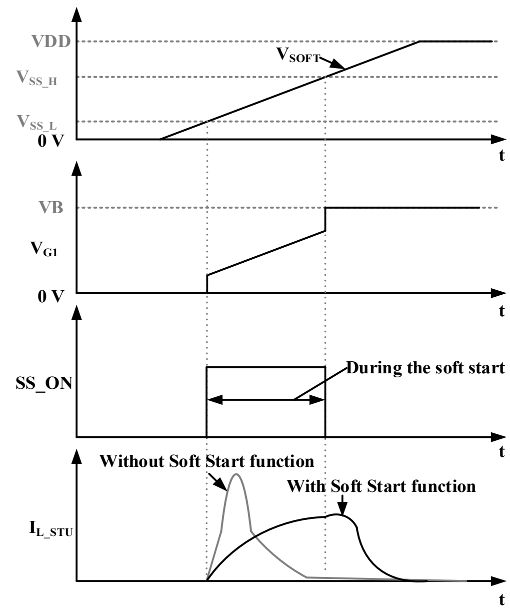


Fig. 4. Timing diagram of proposed Soft Start circuits.

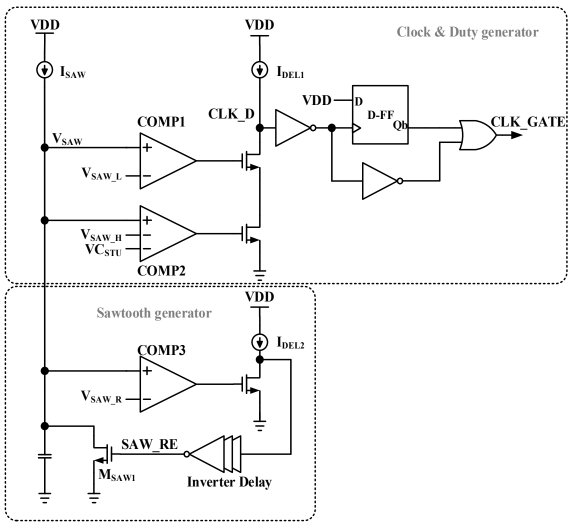


Fig. 5. Proposed clock generator circuits.

When the V_{SAW} voltage is higher than V_{SAW_L}, the CLK_GATE signal is generated from the level of VC_{STU}. When VC_{STU} is higher than V_{SAW_H}, the maximum duty ratio of the CLK_GATE signal is limited.

Fig. 7 shows the block diagram of high side buffer in the Step-Up Converter. It consists of Level Shifter and Gate Driver. The external capacitor (C_B) is connected between VB and VS. To reduce static current, the width of M_{L1} and M_{L2} must have small value. The currents of D_{L1} and D_{L2} are reduced by each of R_{L1} and R_{L2}, respectively. High side buffer is used to maintain the V_{GS} of M_2 at 5 V.

Fig. 8 shows the timing diagram of high side buffer in Step-Up Converter.

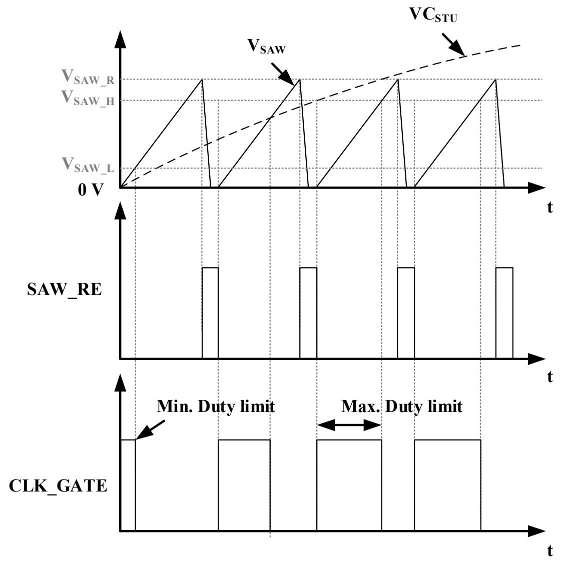


Fig. 6. Timing diagram of clock generator.

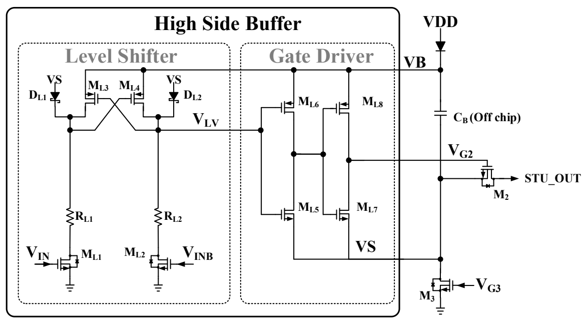


Fig. 7. Block diagram of high side buffer in Step-Up Converter.

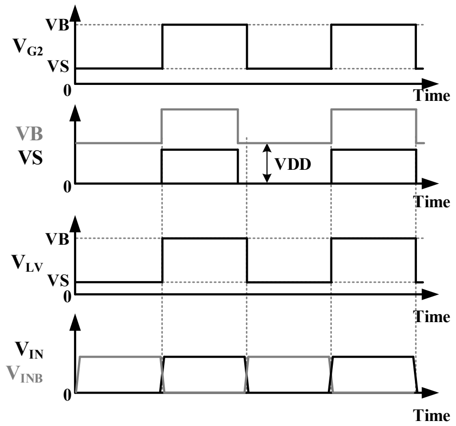


Fig. 8. The timing diagram of high side buffer in Step-Up Converter.

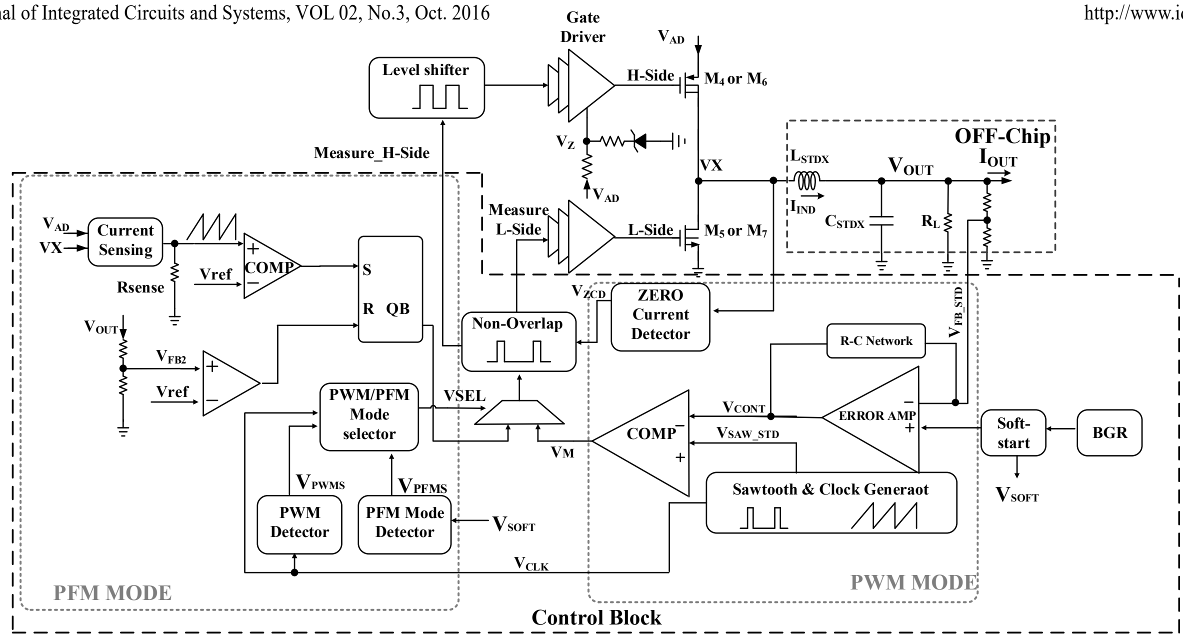


Fig. 9. Block diagram of Step-Down Converter.

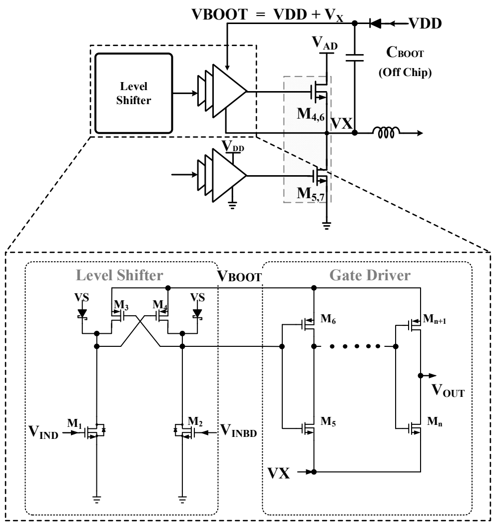
The timing diagram assumes that the forward diode voltage drop is zero. The voltage level range of V_{LV} has from VS voltage to VB voltage according to V_{IN} and V_{INB} signals. Therefore, V_{G2} voltage becomes VB voltage or VS voltage.

B. Step-Down Converter

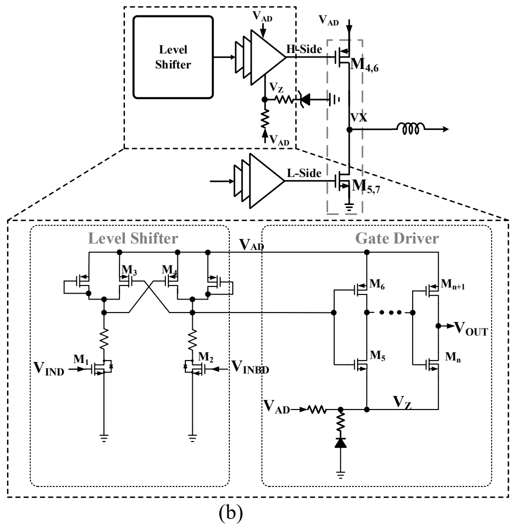
Fig. 9 shows the proposed Step-Down Converter. The bootstrapping method is recommended since the high input voltage of 12 V is used. In this paper, however, a Zener diode is used for the high side MOSFET operation. Conduction loss is the dominant loss factor in the heavy load condition. The switching loss is the dominant loss factor in the light load condition. The Step-Down Converter operates in the PFM mode until the inductor current becomes 80 mA, which is the limiting point of the Discontinuous Current Mode (DCM). When the inductor current is greater than 80 mA, the Circuit operates in Continuous Current Mode (CCM).

In PWM Mode, V_{FB_STD}, and the BGR voltage are compared through Error Amp. V_{CONT}, the output signal of Error Amp., and V_{SAW_STD} are compared with the outputs VM signal. VM is the pulse wave which has a constant duty ratio, from which the output voltage of the Step-Down Converter, V_{OUT}, is determined. The efficiency of the Step-Down Converter differs according to the load. As explained above, with a light load, the switching loss is the dominant factor. Therefore, it is necessary to slow down the switching frequency and minimize the switching loss.

Fig. 10 shows the proposed high side MOSFET operating method. The Zener diode limiting method is adapted to maintain the V_{GS} voltage of M_4 to less than 5 V. In the bootstrapping method, C_{BOOT} should be outside the chip since the size of C_{BOOT} is very large [3]. On the contrary, in the Zener diode limiting method, the high side MOSFET can be driven without C_{BOOT}. This is the main benefit of the Zener diode limiting method since chip integration is possible.



(a)



(b)

Fig. 10. Operating method of High side MOSFET (a) Conventional bootstrapping method (b) Proposed Zener diode limiting method

Fig. 11 shows the timing diagram of the Zener diode limiting method. As shown in the H-Side wave, the H-side is driven from 7 V to 12 V. The $M_{4,6}$ can be protected from the MOSFET destruction problem since the voltage is limited by the Zener diode, even if a high voltage of 12V is applied. When M_4 or M_6 is ON, the current is charged and V_{SG} maintains 5 V since the Source voltage of $M_{4,6}$ is always 12 V. When the gate voltage reaches 12 V, V_{SG} becomes 0 V and $M_{4,6}$ is OFF. In the case of VX, the gate voltage reaches 12 V when H-Side is 7 V. On the contrary, when H-Side is 12 V and L-Side is ON, the current is discharged and the V_X node becomes 0 V, since $M_{5,7}$ is ON. The output voltage is maintained by charging and discharging $M_{4,6}$ and $M_{5,7}$ respectively.

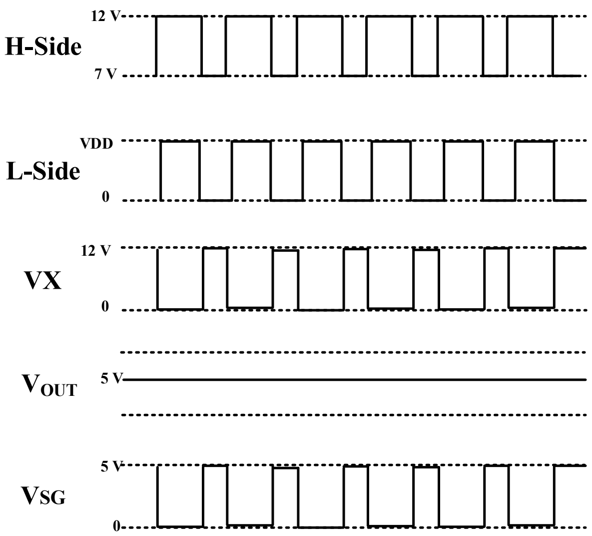


Fig. 11 Power Stage timing diagram.

Fig. 12 shows the timing diagram of the PWM/PFM mode selection. The PWM/PFM mode is changed according to the load condition. When the load is changed from a heavy load to a light load, an inductor current is detected as the DCM Mode and changed to the PFM Mode. While the load is changing to light load, the Zero Current Detector outputs a V_{ZCD} signal, and when the PFM Detector detects V_{ZCD} more than 6 times, V_{PFMS} becomes high. When V_{PFMS} becomes high, the PWM/PFM Mode Selector outputs a VSEL signal as high, and the PFM Mode is selected. The ripple of V_{OUT} becomes higher since the PFM Mode has slow frequency. However, efficiency of Step-Down Converter is improved by minimizing the switching loss. In PFM mode, the PWM mode circuit is not necessary. To reduce the current consumption of Step-Down Converter, the PWM mode circuit is disabled.

Fig. 13 shows a schematic of the Hysteresis Mode Selection Circuit. Its purpose is to prevent unstable operation when the load current is around the critical current for the PWM/PFM mode change. When the operating mode is changed from the CCM mode to the DCM mode, the VZCD signal becomes high. The Hysteresis Mode Selection Circuit changes the mode after receiving the high VZCD signal 6 times consecutively. Due to this circuit, malfunction of the DC-DC Converter can be prevented and the power efficiency can be improved. The DC-DC Converter operates in PWM or PFM modes in order to achieve high efficiency over the wide load current range.

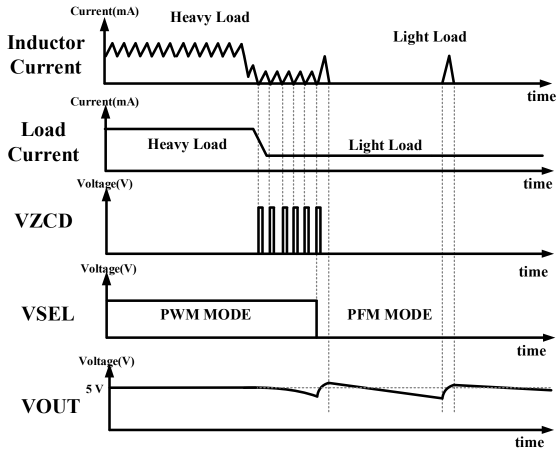


Fig.12. PWM/PFM Mode Selection timing diagram.

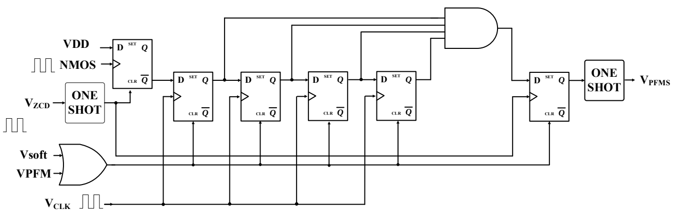


Fig. 13. Hysteresis Mode Selection Circuit.

III. EXPERIMENTAL RESULTS

The proposed chip is fabricated using 0.18 μm BCD technology, a single poly layer, four layers of metal, various options of metal-insulator-metal (MIM) capacitors, and high sheet resistance poly resistors.

Fig. 14 shows a chip microphotograph of PMIC for PTU IC. The die area of the PMIC for PTU is 2000 μm x 2000 μm. The routing metals are stacked to minimize the wire resistance and conduction loss. To minimize conduction loss, metal 1 to Top metal is laminated and the size of the power MOS is maximized.

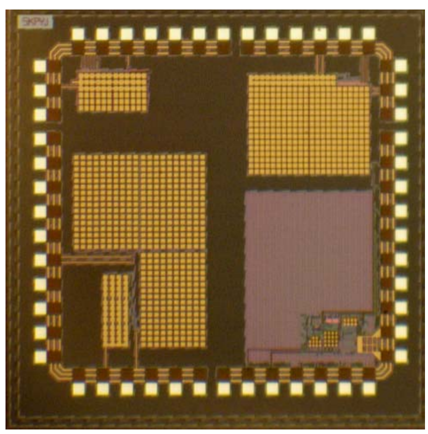


Fig. 14. A chip microphotograph of PMIC for PTU.

Fig. 15 shows the measured power conversion efficiency of the Step-Up Converter with respect to the load current when the output voltage is 20 V. It is reduced by 1.5 % due to the resistance of the PCB trace and bond wire of the package compared with the post layout simulation result. The measured peak power conversion efficiency is 92.8 %.

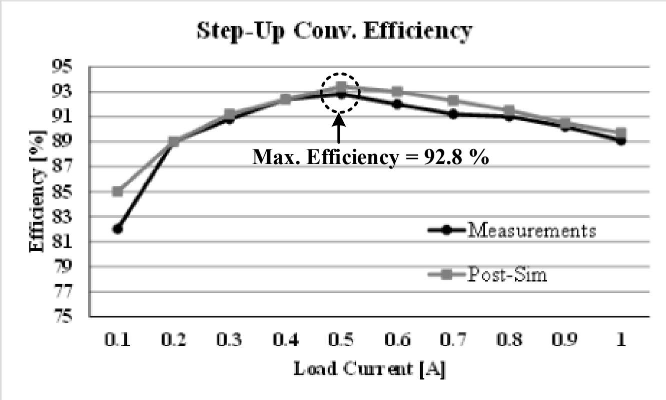


Fig. 15. Measured power conversion efficiency with respect to load current.

IV. CONCLUSIONS

This paper presents a Power Transmitting Unit (PTU) for magnetic resonant A4WP application. A high efficiency Step-Up Converter with a programmable output is proposed to provide the supply voltage to the external PA with the peak power of 37.5 W. In order to implement the closed loop gain control function of the PTU with the PRU, the duty cycle is controlled with the PWM signal from the Bluetooth Low Energy (BLE).

This chip is fabricated using a 0.18 μm BCD process with high power MOSFET options, and the die area is 2000 μm x 2000 μm. The measured maximum power efficiency of the Step-Up Converter and Step-Down Converter is 92.8% at a load current of 0.5A and 93.8% at a load current of 0.3A, respectively. The output voltage of the Step-Up Converter ranges from 12 V to 25 V. The output voltage of the Step-Down converter is 3.3V and 5V respectively.

ACKNOWLEDGMENT

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