

# A DLL-based reference-less CDR with ISI jitter reduction scheme for clock-embedded signaling in 65nm process

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**Abstract** - A DLL-based reference-less CDR for clock-embedded signaling in 65nm CMOS is presented. The proposed receiver operates in mixed mode and the supply voltage is 1.0 V. To save the channel for forwarded clock and eliminate the external reference, clock-embedded signaling scheme is used in this proposal. DLL-based architecture is adopted to save the power consumption. To accomplish a 10Gb/s data rate, inter-symbol-interference (ISI) jitter reduction technique is presented. ISI jitter reduction reduces the bit-error rate (BER) of the receiver by enlarging the sampling margin. To save the power consumption, new deskew method which is done by sub-DLL is presented to use D-flip flops instead of sense-amps. The sub-DLL also gives tolerance to PVT variations to the receiver. The post-layout simulation results, which were done with the Samsung 65nm process model, verify the operation of the proposed schemes.

## I. INTRODUCTION

Channel loss in high frequency signals, induced by skin effect and dielectric loss, is the main bottleneck to increase data rate in communication systems. To deal with the channel loss, the importance of clock and data recovery (CDR) circuits are being stressed. Recently, many reference-less CDR circuits has been reported to remove the bulky external reference frequency [1]-[5]. Also due to its simplicity and flexibility for different applications, reference-less architecture is quite popular in industry.

In display industry, the state of the art display interfaces are support 8K (8192×4320) resolution in LCD TV systems. Moreover the advent of virtual reality (VR) technology which needs over 4K (4096×2160) resolution displays, accelerates the high data BW demands in mobile display area. For instance, the 4K resolution display interface should support over 10Gb/s as shown in Fig. 1. In intra-panel interfaces, point-to-point transmission with clock-embedded signaling (CES) scheme is widely used. Fig. 2 illustrates the data packet in CES scheme. Clock embedded signaling eliminates the forwarded clock path by combining data and reference clock thus the receiver can operate in

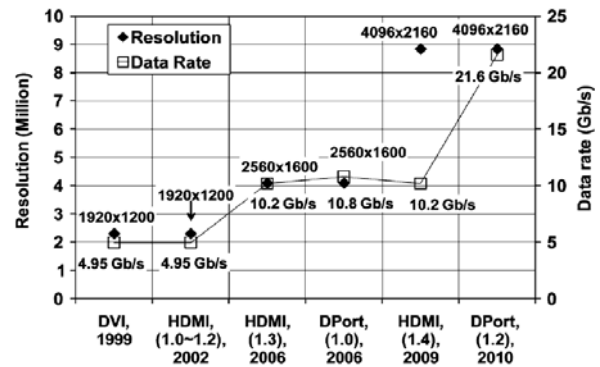


Fig. 1. Maximum resolutions and data rates of the display interfaces [6].

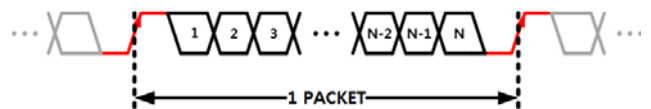


Fig. 2. Clock embedded signaling.

reference-less mode. DLL-based reference-less CDR circuits has been used in intra-display interfaces. There are several benefits from DLL-based architecture; loop stability and low power. As it has no feedback loop, DLL-based architecture is free from loop stability issue. And generally, DLL-based CDRs consume less power than PLL-based ones.

Inter-symbol-interference (ISI) effect is the main concern in establishing DLL-based systems as the data bandwidth demand approaches 10Gb/s. As data rate goes high, ISI jitter effects on clock-embedded signal disturbs DLL-based system to operate precisely. DLL-based CDRs suffer from high bit error rate (BER) caused by clock and data jitter induced by ISI and random noise. Unlike DLL-based CDR, the loop of PLL-based CDR filters out clock and data jitter. Therefore, PLL-based CDRs exhibit lower BER performance than DLL-based CDRs when clock-embedded signal suffers from ISI effect. Furthermore, embedded-clock extraction failure, which stops the DLL-based CDR's operation, can occur when large ISI jitter exists. At harsh ISI environments, both DLL and PLL based CDRs need equalizer to compensate the channel loss which consumes lots of energy. But at moderate ISI conditions, which equalizers are not needed, DLL-based CDRs suffer from high bit error rate (BER) caused by clock and data jitter induced by ISI and random noise.

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In this work, the design and simulation results of a 10Gb/s DLL-based CDR with low power clock jitter reduction technique for CES application implemented in 65nm CMOS technology. A low overhead decision-feedback equalization (DFE) technique is utilized only for embedded clocks to reduce power consumption and enlarge the sampling margin. A novel deskew concept is presented which enables the use of conventional D-flop-flops (DFF) instead of sense-amps (SA). Elimination of SAs leads to less power consumption. Generally SAs consume more power than DFFs. This proposal is organized as follows. Section II reviews the previous DLL-based CDR works and discusses how ISI degrades the circuit performance. Section III describes the architecture of proposed DLL-based CDR and the operation of the circuits and explains the design flow. Section IV presents the simulation results that verifies the proposed scheme. Section V concludes this work.

II. ISI EFFECTS ON DLL-BASED CDR

A. Operation of the DLL-based CDR

Fig. 3(a) illustrates the overall block diagram of DLL-based CDR and Fig. 3(b) shows the clock-embedded signal which contains both training period and receiving period. As shown at Fig. 5(a), clock-embedded signal is composed of N bit data and embedded clock bits. In this figure, the overhead of embedded clock is 2bit. To increase the effective data in one packet, smaller embedded clock bit is preferred. At the beginning of the operation, the receiver receives training pattern as shown as Fig. 3(b) and that pattern used for reference of DLL. Sub voltage-controlled delay line (VCDL) is used for compensate the delay of clock extraction block. Sub VCDL aligns the reference clock with CLK<X> which generated by VCDL. Fig. 4 shows the flow chart, which describes the consecutive operation of the DLL-based CDR. Fig. 5 explains the clock extraction and data recovery of DLL-based CDR with assuming the delay of clock extraction & sub VCDL is zero. At training period, clock extraction block bypasses the training pattern to lock the DLL. After the DLL is locked, clock extraction block use two clocks generated by DLL to make the window which used for AND operation with embedded clock (Fig. 5(a)). If the clock extraction success, VCDL makes clocks and the samplers use that clocks for data recovery. Clock extraction block makes new window and generate reference clock from the next data packet. If the extraction fails, VCDL stops making sampling clocks and the whole receiver stops. So clock extraction, which makes the reference of DLL, must always success for CDR to keep operating. To ensure safe embedded clock extraction, the window which generated by the VCDL clocks must stay in correct position.

B. ISI effects on DLL-based CDR

As mentioned before, small overhead bit is preferred to increase the data portion of one CES packet. But small overhead makes the data and embedded clock closer and causes larger ISI jitter at clock-embedded signal. Moreover, as the data rate demand goes high, channel loss which causes ISI also becomes larger due to skin effect. As shown

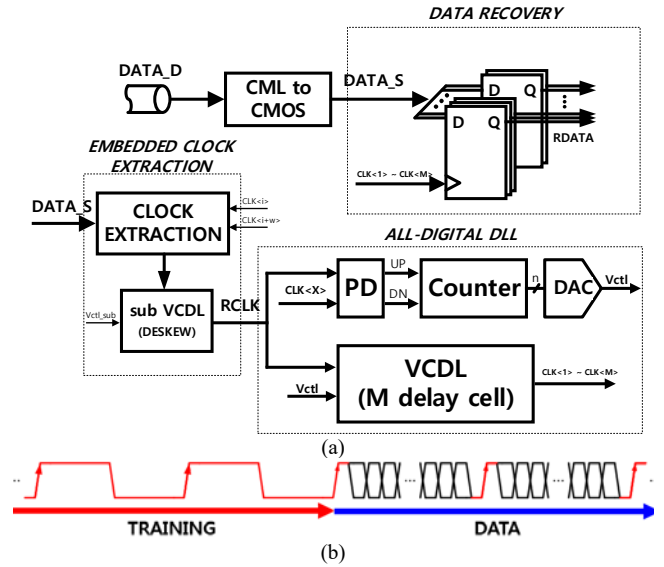


Fig. 3. Architecture of DLL-based CDR; (a) block diagram (b) timing diagram

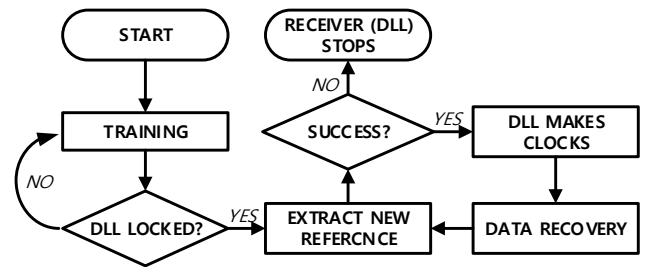


Fig. 4. Flow chart of operation of DLL-based CDR.

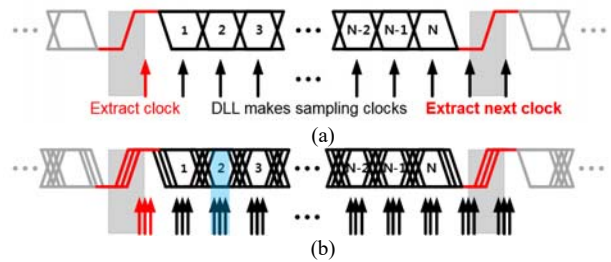


Fig. 5. Timing diagram of CES data and DLL clocks when (a) without ISI, and (b) with ISI.

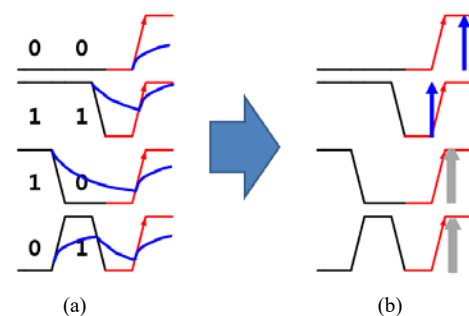


Fig. 6. ISI effects on the embedded clock when signal passed (a) before and (b) after buffer.

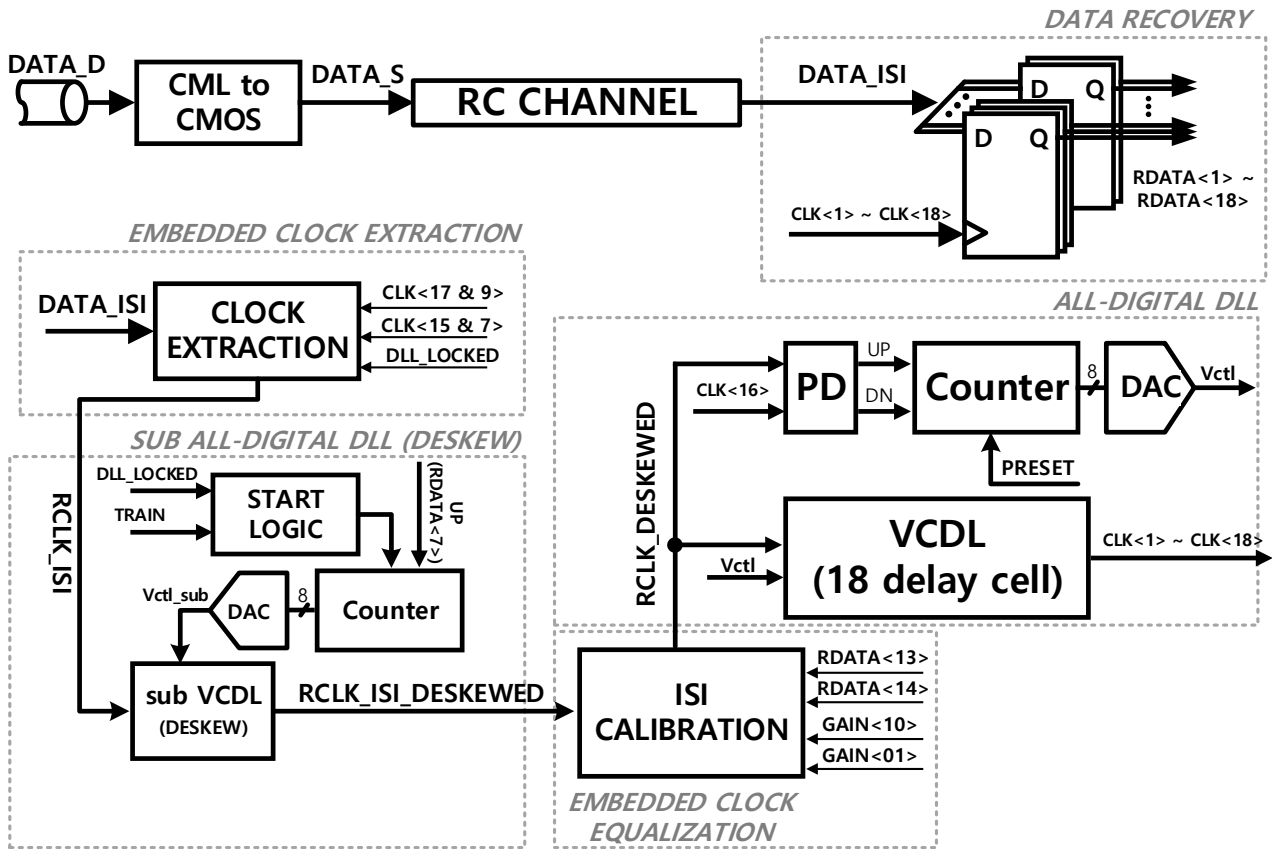


Fig. 7. Overall architecture of proposed DLL-based CDR.

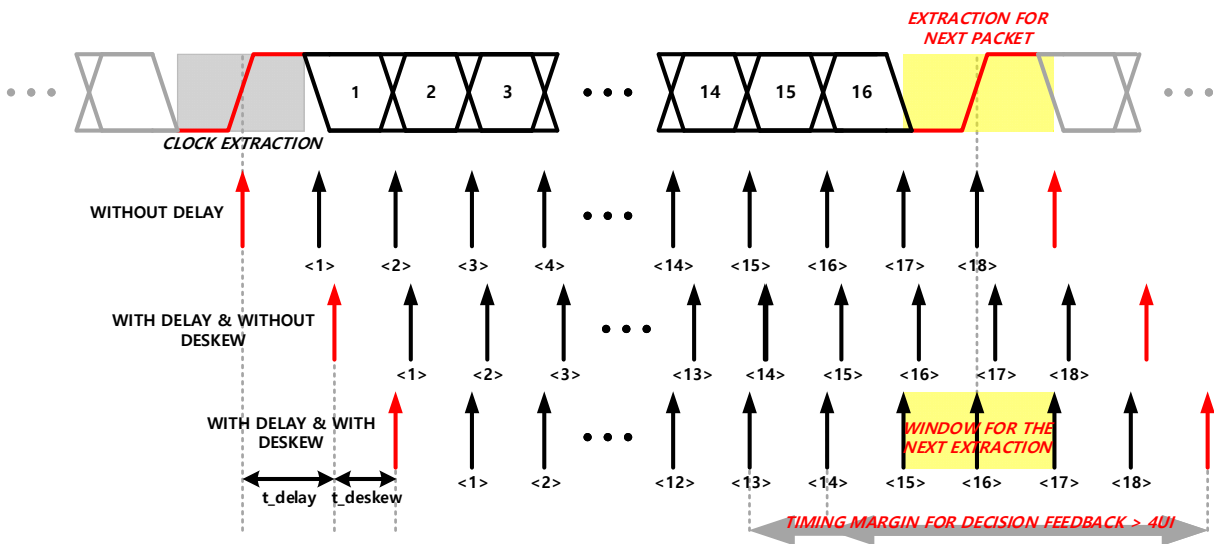


Fig. 8. Timing diagram of CDR's operation, deskew, and window generation.

as Fig. 6, the symbols which positioned near the embedded clock cause ISI jitter. Fig. 5(b) illustrates the ISI effects with 2bit overhead. Even if the extraction block succeed to extract the clock, sampling clocks which generated by VCDL have same amount of ISI jitter as much as reference clock has. Moreover, the last clock generated by VCDL has more jitter than the reference because of the accumulation of random jitter caused by non-idealities and random noise;

quantized error, power noise, mismatches, and deskew error. So when ISI exists, sampling margin reduces. The reduction of sampling margin degrades the CDR's BER. So we should overcome ISI effects to design DLL-based CDR operating at high data rate. There are many reports about equalizers which compensate the channel loss to overcome ISI effect on signal [7], [8]. However equalizers consume power even more than the DLL-based CDR [2].

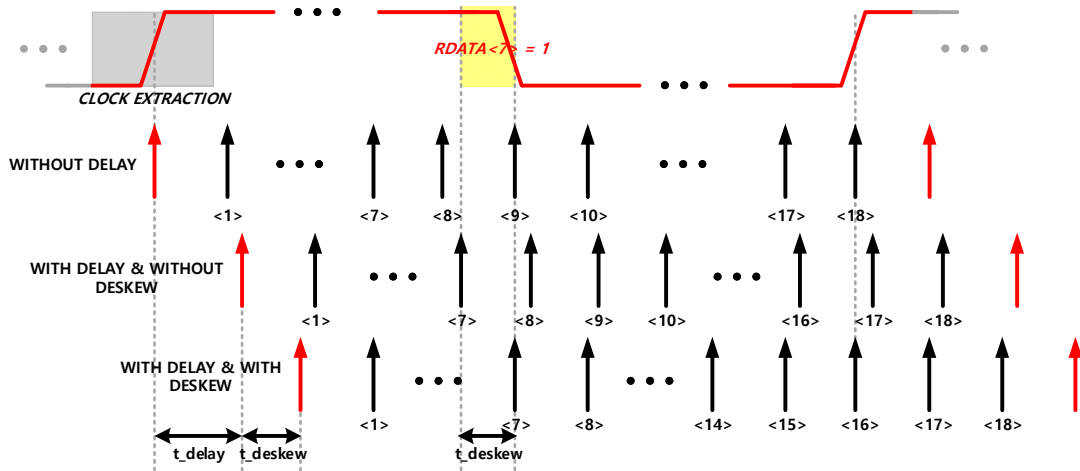


Fig. 9. Timing diagram of the sub-DLL's operation.

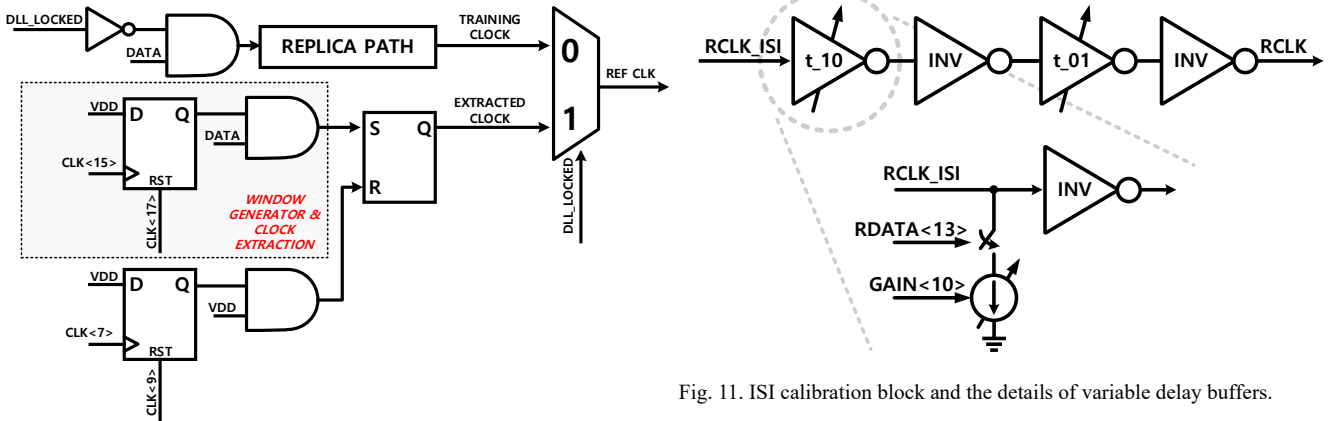


Fig. 10. The clock extraction circuit.

Fig. 11. ISI calibration block and the details of variable delay buffers.

### III. PROPOSED WORK

#### A. Overall architecture of proposed DLL-based CDR

Fig. 7 illustrates the overall block diagram of the proposed DLL-based CDR. And Fig. 8 shows the timing diagram of over receiver's operation. On-chip RC channel is implemented to simulate the channel loss which gives ISI effects on CES signal. There are two DLLs, the main DLL is used for making sampling clocks and the sub-DLL is used for deskewing the delay made by clock extraction & equalization path. The 16<sup>th</sup> clock made by VCDL is aligned with the next embedded clock by the sub-DLL's operation. The deskew operation is done during training period. After the main DLL locked, "DLL\_LOCKED" signal changes and the start logic of sub-DLL stops the counter and the "t\_deskew" value is memorized in the counter's value of sub-DLL. After training period, ISI calibration block compensates ISI jitter by aligning the extracted clock. The aligning is done by changing inverter's delay through looking the sampled symbol value. The samplers, recovers the data, are implemented by DFFs. The proposed deskew operation enlarges the timing margin for decision feedback to ISI calibration block more than 4UI. So, we can save power consumption by using DFFs instead of Sense-Amps.

#### B. Deskew operation of sub-DLL

The sub-DLL's deskew operation is illustrated in Fig. 9 and the block diagram of the DLL is shown in Fig. 7. Sub-DLL's deskew operation is done by making the sum of delays 2UI ( $t_{\text{delay}} + t_{\text{deskew}} = 2\text{UI}$ ). At the beginning of operation, the counter values of two DLLs are initialized to make the delay of the DLLs minimum. The RDATA<7>, which is the sampled data by the CLK<7>, is used to the UP information of the counter. As the counter's value goes high, the delay of sub-DLL becomes larger until RDATA<7> is LOW. When RDATA<7> becomes low, sub-DLL fixes the counter value. The deskew delay "t\_deskew", which is the tuning range of sub-DLL, is designed to vary from 0.5UI to 2UI at 10Gb/s. Because of this tuning range, sub-DLL can compensate the variation of extraction block delay ("t\_delay") caused by PVT variations.

#### C. Clock extraction

Clock extraction block is implemented as shown as Fig. 10. The DFF is used to make the window for extract the embedded clock. The 15<sup>th</sup> and 17<sup>th</sup> clock are used to make window. After the window generation, AND gate extracts the embedded clock position by doing AND CES data with window. SR-latch makes the final extracted clock. CLK<7> and CLK<9> are used for reset pulse. In training period,

CES data is bypassed and the replica path makes the bypassed clock delay and the extracted clock delay same. After the main DLL locks, “DLL\_LOCKED” signal changes and the replica path turns off.

*D. ISI calibration by variable delay buffers*

ISI calibration block uses the recovered data to compensate the ISI jitter. ISI jitter is deterministic as shown as Fig. 2. Therefore ISI jitter can be compensated by giving different delays according to the data pattern. Proposed ISI calibration method aligns the embedded clock with the “00” data pattern clock which is the blue one in Fig. 12. The variable delay buffer, illustrated in Fig. 11, receives the sampled data and uses that information to change its delays. For example, if the data pattern is “10” (RDATA<13> = 1 and RDATA<14> = 0), the current source of the t<sub>10</sub> buffer makes the inverter under skewed and the latter variable delay buffer operates as non-skewed inverter. The delay variation amount is determined by the amount of current which controlled by the external gain. The switches and current sources is implemented by NMOS.

*E. Design flow*

Our goal is the implementation of a 10Gb/s low power CDR for CES applications with ISI conditions. We chose the DLL-based CDR architecture to take the advantage of low power consumption characteristic of DLL-based CDR. And we simulated the ISI effects on DLL-based CDR by introducing on chip RC channel. Proposed ISI calibration block and deskew block are also verified by simulation. The whole circuit was post-layout simulated with the process parameters of the Samsung 65nm CMOS process.

IV. RESULTS AND DISCUSSION

The channel is simulated by RC network. Fig. 13 shows the RC channel effects and the ISI on CES DATA. The operation of ISI calibration block was verified by simulation at 10Gb/s as shown as Fig. 14. The ISI calibration block reduced 22ps (0.22UI) of ISI jitter in the simulation. The deskew block operated successfully. The recovered clocks which are generated by extracted clock show that the deskew operation was done accurately. Fig. 15, the post-layout simulation results, verifies the design goal of proposed circuit, which is to enlarge the sampling margin.

The proposed work is fabricated in Samsung 65nm CMOS process. Fig. 16 shows the die photo and the active area is 310 × 210μm<sup>2</sup>. Table 1 shows the summary of performance which is the result of the post-layout simulation.

Bit-error-free operation is not accomplished in 10Gbps which is the target data rate. We are going to revise the chip to verify the operation of calibration circuit at 10Gbps.

V. CONCLUSIONS

A 10Gb/s reference-less DLL-based CDR with ISI calibration technique for CES applications is proposed in this work. To accomplish low power consumption, sub-DLL

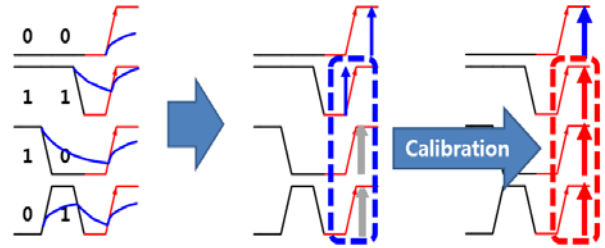


Fig. 12. ISI calibration by sampled data.

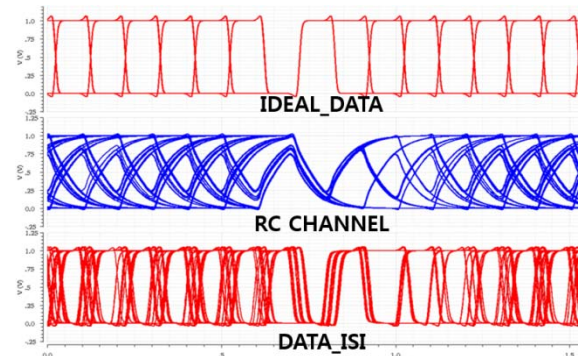


Fig. 13. Simulation results of the ISI caused by RC network

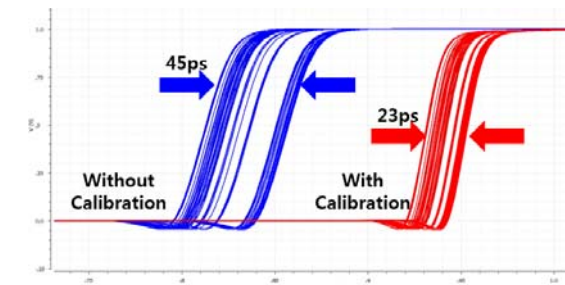


Fig. 14. Simulation results of the recovered clocks with and without calibration.

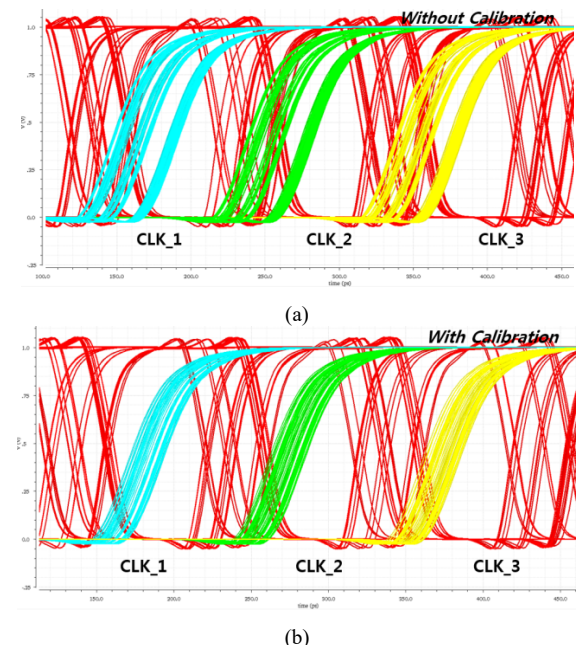


Fig. 15. Simulation results shows the sampling margin (a) without calibration and (b) with calibration.

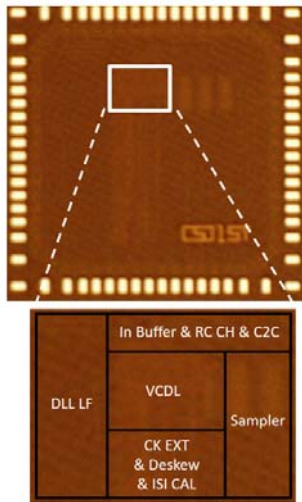


Fig. 16. Die photo.

TABLE I.  
Performance summary (\*post-layout simulation result).

Technology	Samsung 65nm CMOS	
Data rate	10Gbps*	
Supply Voltage	1.0 V	
Power Consumption*	ISI calibration	0.41 mW
	DLL	3.73 mW
	Etc.	3.18 mW
	Total	7.32 mW
Area	0.0651mm <sup>2</sup>	

performs proposed deskew scheme. The timing margin for decision feedback enlarged by proposed deskew concept, and the timing margin for decision feedback eliminates the need of Sense-Amps which consumes power larger than D-flip flops. The ISI jitter reduction technique was implemented by the variable delay buffers. The buffer’s power consumption is much smaller than conventional DFE schemes. Even if the channel loss is big, this scheme relaxes the equalizer’s power overhead. Several post-layout simulations were done to verify the proposed schemes.

ACKNOWLEDGMENT

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