A 32GHz Transformer Based Differential SPST CMOS switch

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Abstract **- A 32GHz transformer based single-pole single-throw (SPST) switch is presented, that is integrated with a low noise amplifier (LNA) in a 65-nm bulk CMOS process. The proposed switch has a series resonance structure at shunt path between differential signal lines to increase isolation when the switch is in off state. It reduces the insertion loss of an entire system by embedding the post matching circuit (LNA input matching network) when the switch is in on state. The measured insertion loss difference between LNA and proposed SPST switch integrated LNA chip is less than 1.35 dB at 30-36 GHz, and the isolation is 25 dB at 32 GHz. The core area of SPST switch is 350 um x 220 um.**

I. INTRODUCTION

Upcoming various millimeter-wave (mm-wave) systems need small size and low loss switches to have reconfigurable circuits. For example, beamforming front-end ICs in mm-wave 5G mobile communication system have to use the switches for antenna to select transmit and receive paths. They have to be carefully designed to have low insertion losses at on state and high isolations at off state, which influence seriously on communication qualities.

The performances of switches at mm-wave frequency are degraded due to the effects of parasitic ground path's inductances. The switch performance is also determined by the product of Ron resistance and Coff capacitance. By reducing the Ron in the case of the series switch, one can reduce the insertion loss, and one can improve the isolation by reducing the Coff. However, the switch performance degrades as frequency increases because Coff capacitance's impedance is in inverse proportion to the frequency, which degrades is

olations. Also, as explained in Fig. 1, shunt switch's performance is largely limited by the parasitic ground path's inductance at the mm-wave frequency because the impedance of the ground inductor (Zshunt in Fig. 1) is proportional to the frequency.

Therefore, the series-shunt structure is commonly used only at a few GHz frequency [1]. To overcome these performance limitations of transistor based switches at high frequencies, the switches with quarter-wave transmission lines are conventionally used as shown in Fig. 2 [2]. However, the transmission line based structure is too large at the mm-wave 5G communication frequencies of ~30GHz to be used in integrated circuits. Therefore, there must be strong demands for small size and low loss switches.

In this paper, we propose a transformer-based SPST switch that includes the input matching network of a following LNA. By including the matching network of the LNA, one can implement the size-efficient and low loss SPST switch.

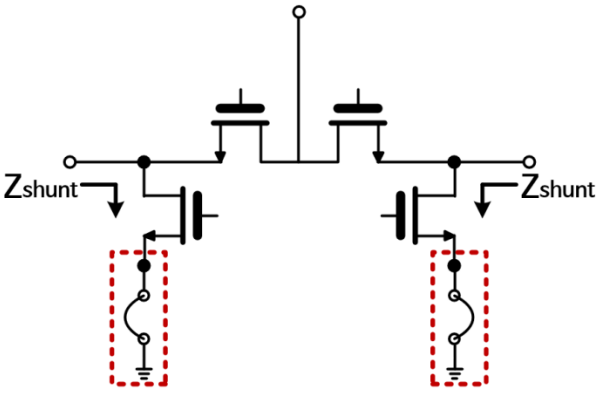

Fig. 1. Transistor based switch structure (series-shunt)

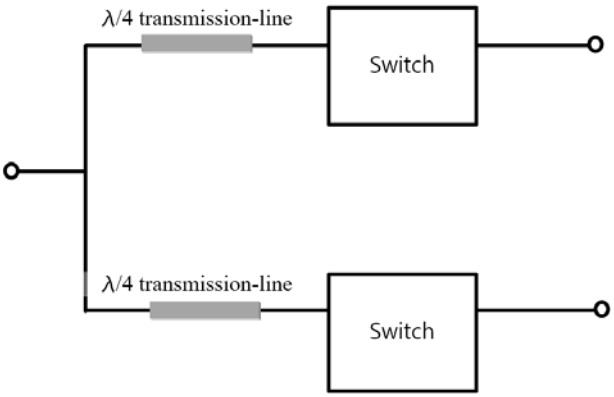

Fig. 2. Quarter-wave transmission line based switch structure.

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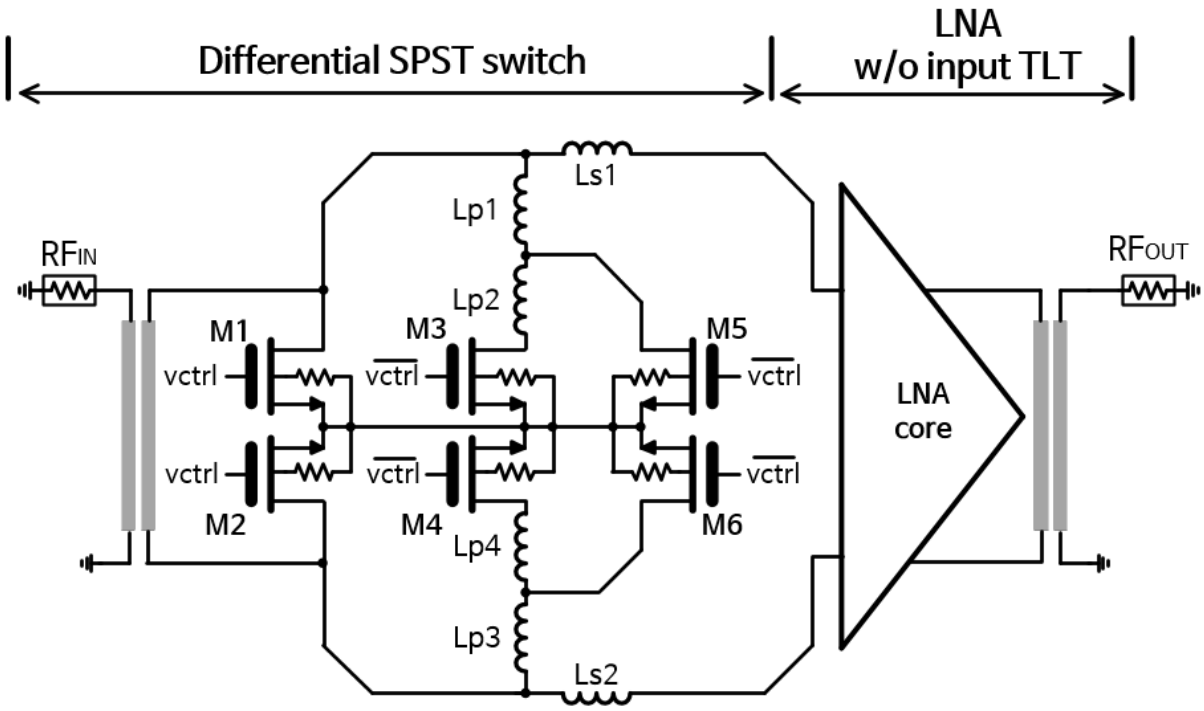

Fig. 3. Schematics of the proposed SPST switch

TABLE I.
Transistor parameters and inductance of the proposed SPST switch

Transistor name	Transistor size W/L[um/um]	Inductor name	Inductance[pH]
M1, M2, M3, M4	96/0.06	Lp1, Lp3	100
M5, M6	192/0.06	Lp2, Lp4	90
		Ls1, Ls2	160

II. CIRCUIT DESIGN

Fig. 3 shows the schematic of the proposed SPST switch that has a transformer based differential structure with a following LNA. The proposed SPST switch consists of a single to differential transmission-line transformer and shunt switch network. The transistor parameters of the switch and inductor size are listed in Table I. Also, Fig. 4 shows equivalent circuits represented by a simplified model of transistors with R_{on} and C_{off}.

A. Pass mode

When the switch is in on state, M1 & M2 is off and M3 – M6 is on in Fig. 4 (b). In this condition, one can ignore L_{p2}, M3, L_{p4}, and M4 because of low R_{on} impedance of large size transistor M5 and M6. Finally, 1:1 transformer, L_{s1} & L_{s2}, L_{p1} & L_{p3}, and off capacitances of M1 & M2 form the input matching network of the following LNA to make low loss and small size switch.

As mentioned above, the switch operates as an input matching network of the following LNA. There are no additional matching network between the switch and the LNA that results in the reduction of the insertion loss and the chip size compared to conventional SPST switches.

B. Isolation mode

Also, as shown in Fig. 4 (c), by using differential structure, one can ignore the effects of ground path's parasitic inductances that degrades the isolation of shunt switch. To make use of the virtual ground, perfect differential signals must be introduced. A large decoupling capacitor at the center tap of the secondary transformer is introduced to make good virtual ground. This allows to make good differential signals and results in better isolation.

To improve the isolation of the switch further, the series resonance at shunt path between the differential signal paths is introduced at the frequency when the switch is in off state. Finally, due to the shunt transistors (M1 and M2) and series resonance path (Lp1, Lp2, M3 and Lp3, Lp4, M4), the proposed switch can have good isolation.

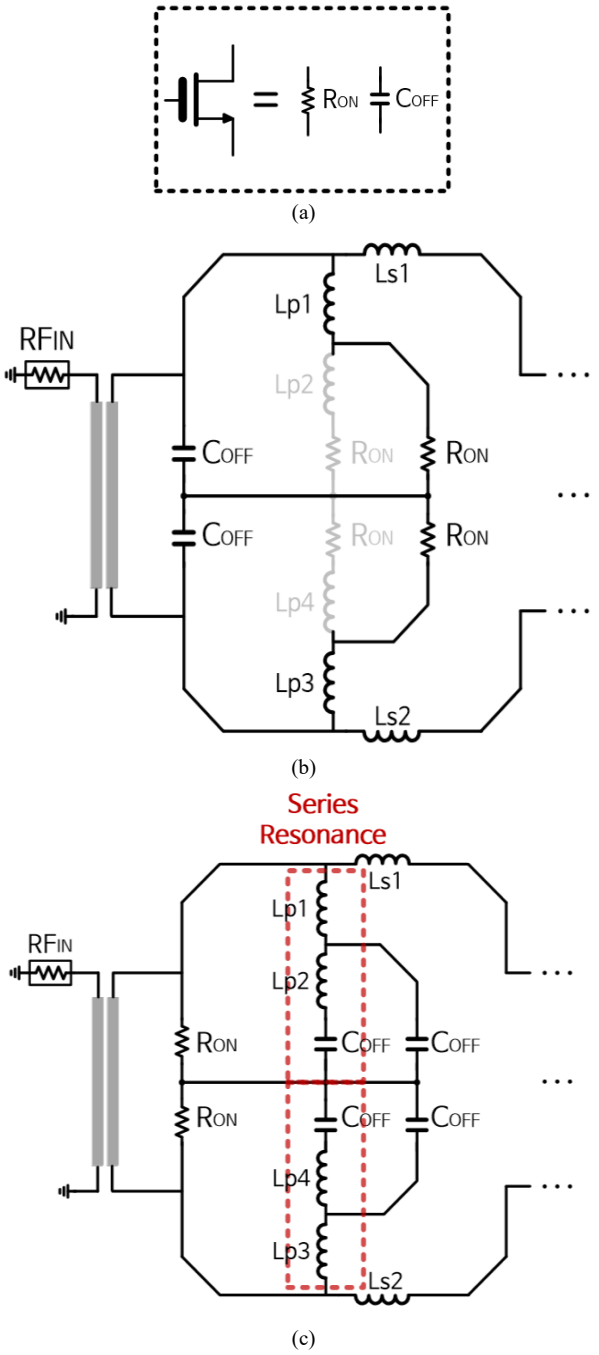

Fig. 4. Equivalent circuits of the proposed SPST switch
(a) Simplified transistor model (b) Pass mode (c) Isolation mode

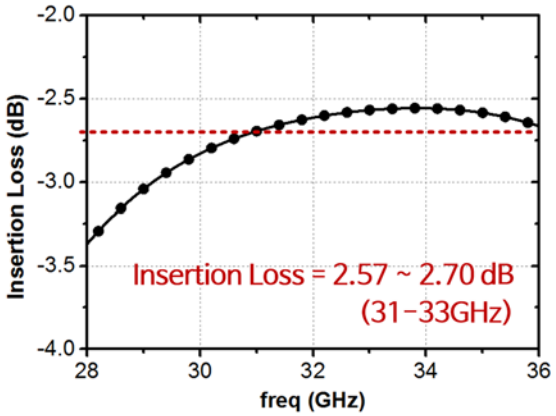

Fig. 5. Simulation results of insertion loss

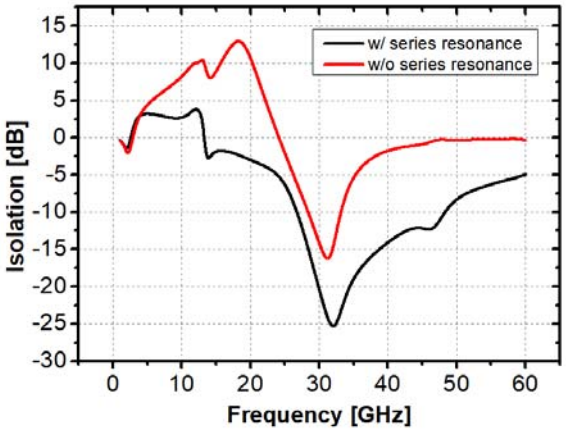

Fig. 6. Simulation results of isolation

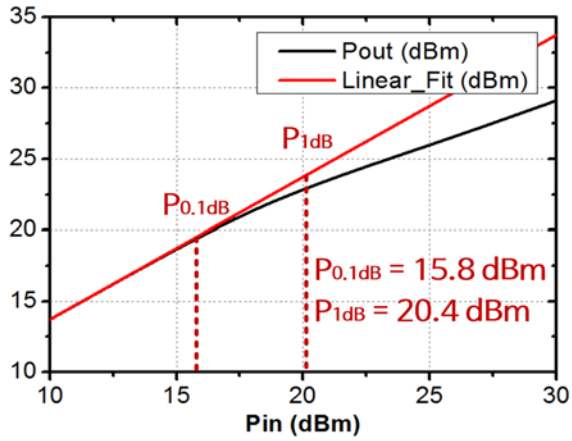

Fig. 7. Simulation results of P1dB & P0.1dB

As in Fig. 5, the simulation results of the insertion loss that includes input matching network of the following LNA is about 2.53 ~ 2.70 dB that corresponds to only about 1.2 dB loss without the loss of the input matching network. This is considerably low compared to those of separate switches.

Also, as in Fig. 6, the isolation is about 25.9 dB when the switch is in off state. Due to the series resonance of the shunt path, additional 10 dB isolation at 32GHz is achieved. Also, the P_{1dB} is 20.4dBm and $P_{0.1dB}$ (=0.1dB compression point) is 15.8dBm as in Fig. 7. This high $P_{0.1dB}$ is enough to meet linearity of various systems. By using the embedded concept and series resonance, the proposed switch has low loss, size efficient, high isolation, and high linearity.

III. IMPLEMENTATION AND MEASUREMENT

The proposed SPST switch was implemented in a 1P9M 65nm CMOS process. Fig. 8 shows a microphotograph of the proposed switch. The area of the switch core is 350um x 220um ($0.077mm^2$). S-parameter measurements are done using a 67-GHz Anritsu 37397D VNA.

Fig. 10 shows the insertion loss of the switch by subtracting the gain of LNA and switch integrated LNA. The SPST switch integrated LNA shows only additional 1.35 dB loss compared to the gain of LNA. This is because of the

TABLE II.
Comparison table with the prior works of SPST switches

Parameters	This work	[3]	[4]	[5]
Technology(nm)	65nm	65nm	130nm	65nm
Frequency (GHz)	30-36	57-66	35	54-84
Insertion loss (dB)	< 1.35 (Difference between LNA and SPST + LNA)	1.6 -2.2	1.0, 1.8, 2.6	1.7
Isolation (dB)	25 @ 32GHz	27	10, 32, 26	35
P1dB (dBm)	*20.4	11	15, >22, 12	10.5

* Simulation

matching circuit embedded structure of the switch. Fig. 11 shows the measured results of switch isolation that is more than 25 dB at 32 GHz. The isolation is improved by introducing the series resonance to the shunt path at the center frequency of 32GHz that is well agreed with the simulated result.

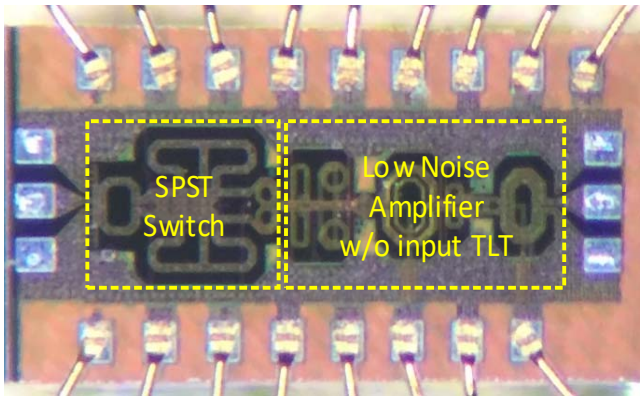

Fig. 8. Chip microphotograph

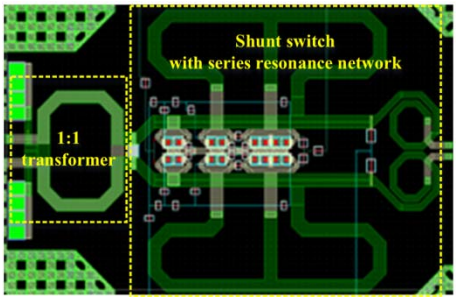

Fig. 9. Switch core layout

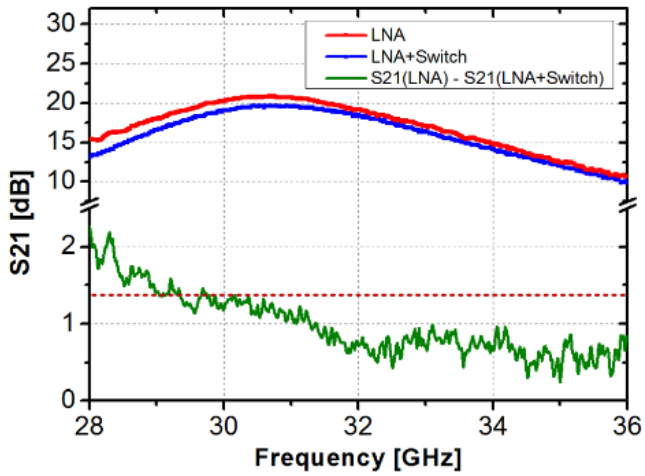

Fig. 10. Measured results of insertion loss difference between LNA and SPST integrated LNA

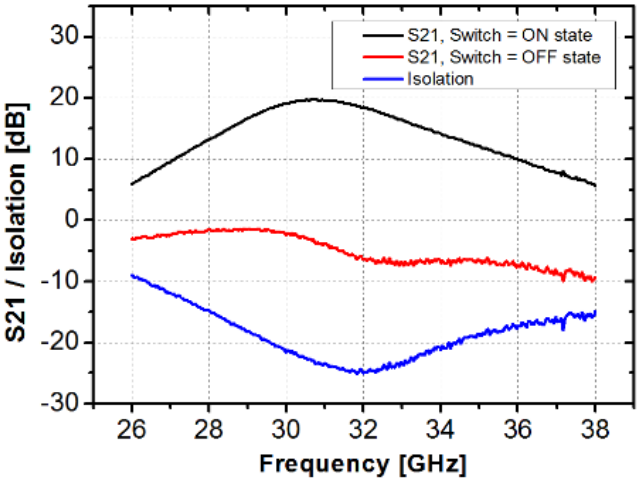

Fig. 11. Measured results of switch isolation

IV. CONCLUSIONS

A transformer-based differential SPST switch that is integrated to the LNA is presented. The switch includes the LNA input matching network and resonance network that improves the insertion loss and isolation. The switch shows the additional insertion loss of less than 1.35 dB by comparing the LNA with an input matching network at 30 to 36 GHz and the isolation of 25 dB at 32 GHz.

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