# A 600 GHz Varactor Doubler using CMOS 65nm process

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***Abstract*** **- Varactor and active mode doublers are fabricated and compared in 600 GHz frequency range in terms of output power using CMOS 65nm technology. In designing a frequency multiplier, active mode is generally preferred, since it can provide high conversion efficiency and bandwidth. On the other hands, varactor mode is rarely used when active mode is available because of its severe operation instability, though it can provide high conversion efficiency theoretically. However, in the high frequency range such as 600 GHz band which is far above the cut-off frequency of 65nm NMOSFET, there is possibility that varactor mode outperforms active mode. As a result of measurement, output power of -19.25 dBm is obtained for the varactor mode doubler which is larger than the active mode doubler by the amount of 3.5 - 6 dBm in different measured frequency. The result is fairly acceptable in 600 GHz frequency considering the process technology.**

## I. INTRODUCTION

Generating power near the frequency of 1 THz is one of the major problems in terahertz applications. Since terahertz source using semiconductor process provides good integration, many research have been done to approach operation frequency of near 1 THz. Recently, high-end technologies such as InP HBT and InP HEMT process offer near -10 dBm of multiplier at 600 GHz. CMOS process is also considered to be one of the good candidates for terahertz applications for its low cost. Hence CMOS terahertz frequency multiplier is studied in this paper which always provides highest operation frequency.

The frequency multiplier mode can be categorized as varistor, varactor, and active mode. A varistor mode multiplier utilizes DC I-V characteristics for a non-linear device. In this case, duty cycle of 25% is the best output waveform of the circuit for extracting second harmonic. So maximum conversion efficiency for varistor mode is limited to 25%[1]. Varactor mode multiplier, which uses C-V characteristics of a device, can offer 100% conversion efficiency in ideal case[2]. But in reality, it is hard to obtain such high conversion performance because of its unstable operation. Even if it is successfully fabricated with high conversion efficiency, it gives narrow bandwidth. This tendency can be observed in commercial products where varistor mode multiplier shows wide bandwidth and low power while varactor mode gives high power with narrowband operation[3]. Active mode multiplier also uses I-V characteristics of a device similar to varistor mode. Unlike varistor mode, it can provide high conversion efficiency and wide bandwidth simultaneously. Therefore active mode multiplier is usually preferred in most of the cases.

To design a multiplier circuit with CMOS 65nm process for high operating frequency such as 600 GHz, however, using active mode may not be the right choice for high output power since the cut-off frequency of a standard NMOSFET device is around 200 GHz. ADS[4] Harmonic

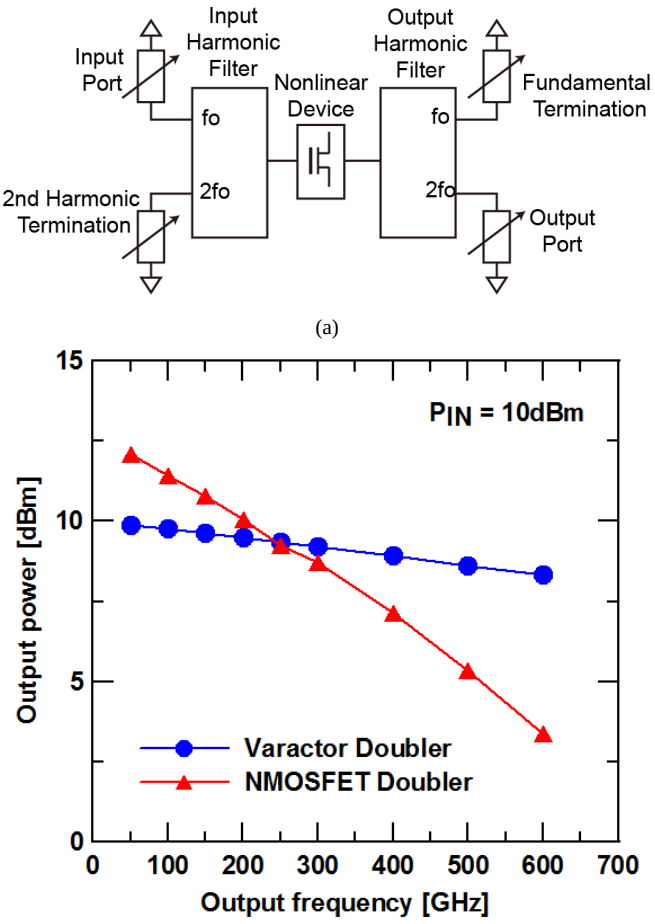


Fig. 1. (a) Block diagram for ideal doubler simulation using harmonic filter and (b) output power for doublers using varactor and active devices.

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Balance simulation with ideal harmonic filter is performed to compare output power of active and varactor mode doublers as shown in Fig1(a). NMOSFET is chosen for active mode device while accumulation thin oxide varactor is for varactor mode. Gate width for both varactor and NMOSFET devices is chosen as 6um and 30um respectively to show its characteristic clearly. Ideal harmonic filter is composed of two in/out ports that allow only single harmonic component and one in/out port that passes all harmonic components. Labels 'fo' and '2fo' on harmonic filter stand for fundamental and second harmonic respectively. And 4 terminations offer optimum impedance for each harmonic path. Simulated output power results are shown in Fig. 1(b). Input power of 10 dBm is used since it is the maximum power level that can be applied for actual measurement.

Active mode provides even conversion gain in frequency up to 200 GHz. But output power decreases rapidly when frequency goes up. If gate width for NMOSFET increases, conversion gain becomes higher in low frequency but output power decreases faster as rises. When gate width decreases on the contrary, output power drops slowly but still offers lower output power at 600 GHz compared to the varactor mode. The varactor doubler provides near 100% conversion efficiency in low frequency and it is fairly maintained in high frequency. In spite of the varactor mode doubler shows better output power above 250 GHz, it is more safe to use active mode multiplier even in high frequency.

However, in very high frequency such as 600 GHz, where output power of active mode doubler drops too much, varactor mode doubler is worthwhile to be considered. And there is an example for varactor mode doubler at 480 GHz which offers high output power compared to other CMOS multiplier circuits[5]. In this paper, simple active and varactor doubler is fabricated and measured at 600 GHz.

## II. CIRCUIT DESIGN

For target frequency 600 GHz, circuit design should not depend too much on non-linear device model unless extra modeling with measurement result is performed, since extrapolation result can be severely deviated from actual operation. Every design parameter takes into account enough margin for unstable operation especially for the varactor doubler and narrowband design is avoided.

As a varactor device for frequency multiplication, standard mode varactor and accumulation mode varactor are considered. The standard mode varactor is constructed by combining drain and source terminal of a NMOSFET, while accumulation mode varactor is provided by manufacturer. The vertical profile for two different types of varactor is shown in Fig. 2[6]. Single-port S-parameter simulation is done for both varactors with same gate dimension as shown in Fig. 3. Non-linearity characteristic can be speculated by normalized C/Cmin ratio at 300 GHz which is the input signal frequency for the doubler circuit. Large capacitance ratio offers high non-linearity for multiplication. And loss can be estimated by series resistance components. In Fig. 3(b), resistance for accumulation mode varies 1 to 3 Ω with control voltage while standard mode varies 21 to 28 Ω.

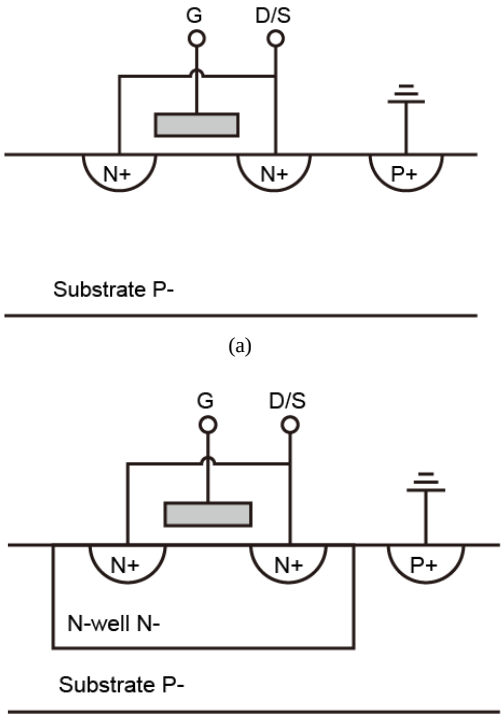



Fig. 2. Vertical profile for (a) standard mode varactor and (b) accumulation mode varactor.

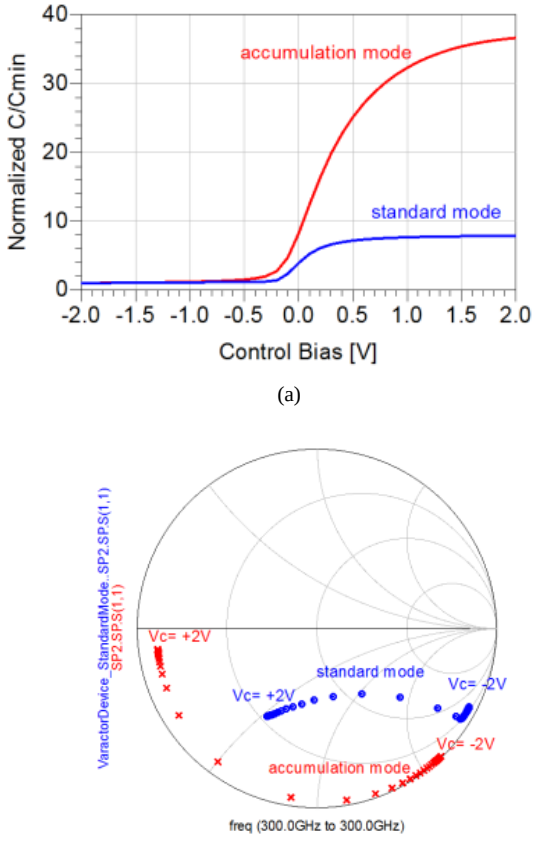
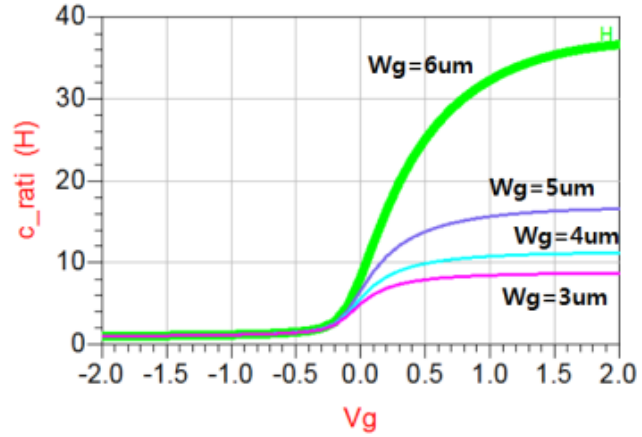
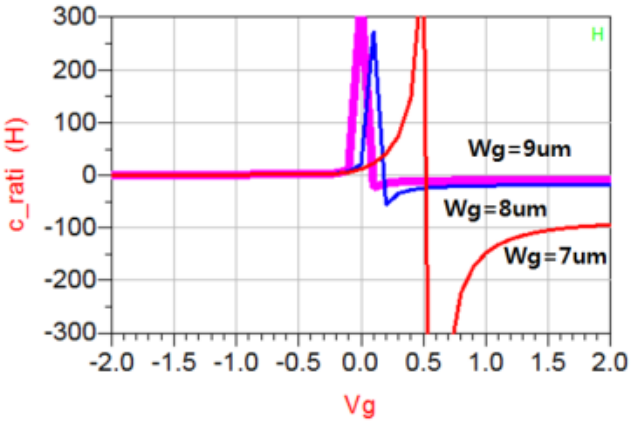



Fig. 3. (a) Normalized C/Cmin and (b) input impedance for a standard mode varactor and accumulation mode varactor.




(a)



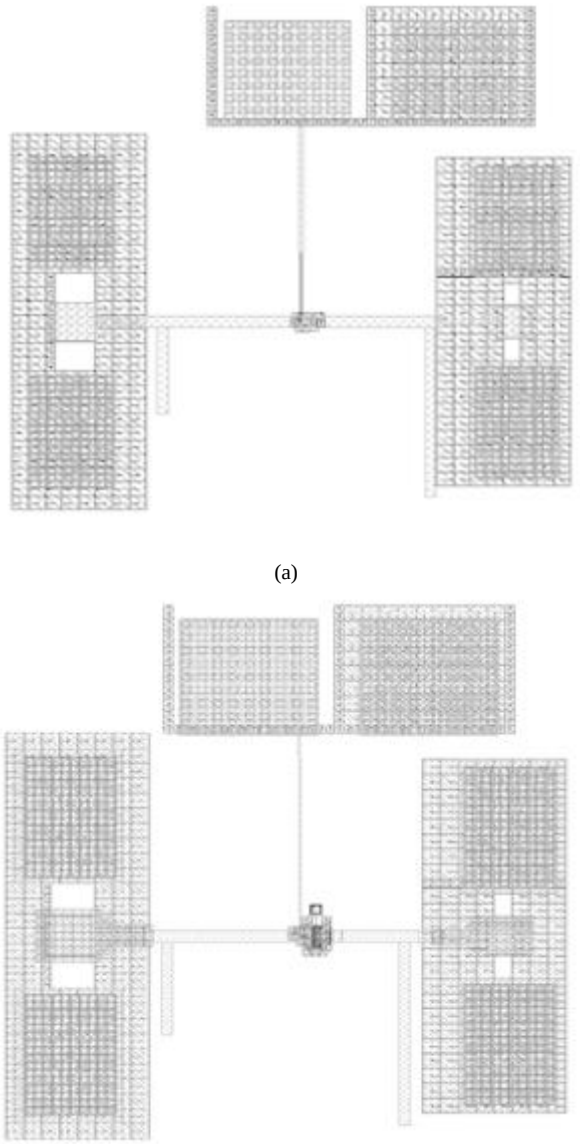

(b)

Fig. 4. Normalized C/Cmin of accumulation mode varactor when gate width is (a) 1 to 6 um and (b) 7 to 9 um.

Therefore accumulation mode varactor is chosen for its high non-linearity and low loss.

Gate width for accumulation mode varactor is chosen as large as possible until self-resonance occurs at 300 GHz range. As shown in Fig. 4(a), large gate width provides high non-linearity until 6 um of gate width. But if enlarged further, self-resonance occurs as in Fig. 4(b) and it gives unstable operation for doubler circuit. So the gate width is chosen as 6 um. For active mode doubler, gate width of NMOSFET is set to 10 um. Since I-V multiplication offer stable operation, gate width for active mode doubler is optimized for output power directly by simulating ideal doubler operating at 600 GHz.

For both active and varactor mode doubler, harmonic matching network is constructed with simple T-shape transmission line as shown in Fig. 5. Metal layer with 3 um thickness is used for transmission line which is the most thickest metal that manufacturer can provide. All of circuit structure including interconnection between device and transmission lines are simulated using 3D EM simulator HFSS[7] which is more convenient to realize complex via structure and small ground slot around devices. Custom input and output RF pads are designed to offer 50 ohm in 300 GHz and 600 GHz respectively.



(a)

(b)

Fig. 5. Layouts for (a) varactor mode doubler and (b) active mode doubler.

Bias voltage for varactor doubler is set to -0.2V though large amount of negative bias offers larger output power. Because quadratic relation between input and output power is broken when ideal doubler is optimized with larger than -0.4V of control voltage which may lead to unexpected operation. Gate and Drain bias voltage for active mode doubler is set to 0.5V(pinch-off) and 1.4V respectively, that is class B operation for I-V multiplication.

## III. MESUREMENT RESULTS

Output power for the varactor and the active mode doubler is measured with setup shown in Fig. 6. To generate 300 GHz input signal for input, Agilent 12.5 GHz signal generator is multiplied by factor of 24 with VDI amplifier-multiplier chain(AMC). And it applied to the input of the doubler circuit through 2-inch WR3.4 waveguide and WR3.4 Casacde waveguide RF probe. Output power from

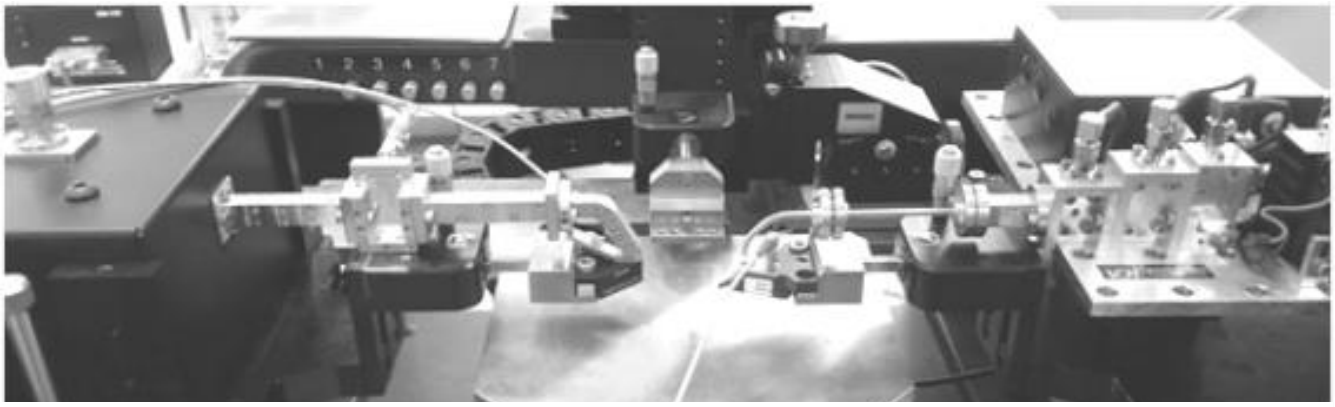
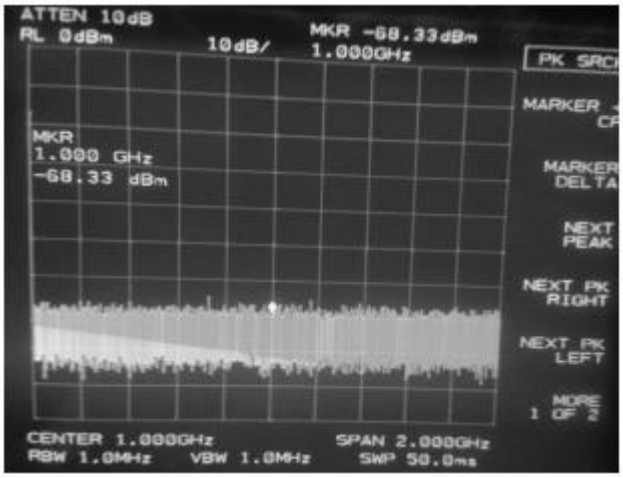


Fig. 6. Output power measurement setup picture for doubler circuit(Low frequency signal generator and spectrum analyzer is not included).

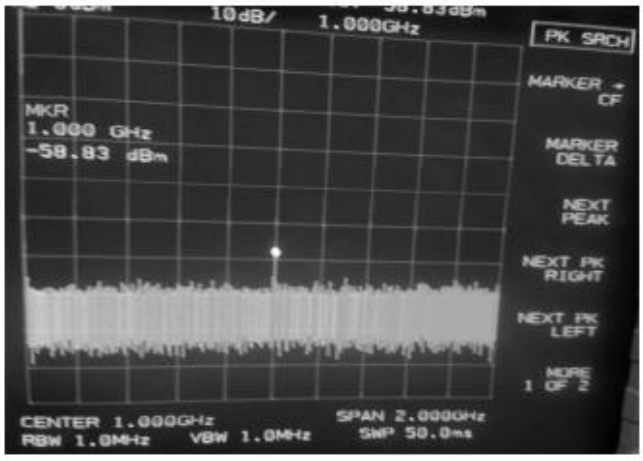
the doubler circuit is detected by VDI WR1.5 sub-harmonic mixer through WR1.5 GGB waveguide RF probe and WR1.5 2-inch waveguide which cut off the fundamental frequency component from the circuit output. Agilent spectrum analyzer shows final output power results from the 1 GHz IF signal. The LO power for subharmonic mixer is applied by VDI WR3.4 frequency extender with Agilent 67 GHz network analyzer. Fig 7 shows output spectrum derived from the measurement setup. Output power in 600 GHz can be observed clearly.

For input path loss, WR3.4 2-inch waveguide and RF probe give 3 dB and 3.5 dB respectively which are measured with 300 GHz AMC and Erickson power meter. Calculated total input path loss is 6.5 dB. Compared to input path loss, output path loss is hard to estimate since there is no 600 GHz source for known standard. For this reason, several loss assumption is done. WR1.5 RF probe gives 7 dB which is provided by manufacturer. Roughly 6 dB loss is assumed for the WR1.5 2-inch waveguide since its electrical length is twice longer when than WR3 2-inch waveguide which introduce 3 dB loss. Conversion loss for WR1.5 sub-harmonic mixer, which is given by manufacturer, supposed to provide 10 to 11 dB in measurement frequency range when WR3 LO power is near 0 dBm. But only -6.3 to -9.3 dBm of LO is applied to the mixer in the frequency range. Since most of the conversion loss is proportional to LO power, 17.3 to 19.9 is assumed. Total assumed loss for output path is 31.3 to 33.9 dBm in measured frequency points. This calculation may contains error but resulting output power shows pretty good agreement with Erickson power meter. Meanwhile, Erickson power meter could not be used for comparing varactor and active mode doubler since it could detect output power for varactor doubler only because of sensitivity limitation.

Measured output power versus frequency is shown in Fig8. For every frequency point, different level of input power is applied since maximum available input power from AMC chain varies with frequency. As a results overall shape for frequency response is overwhelmed by output power of




(a)




(b)

Fig. 7. Spectrum analyzer windows when (a) there is no output signal and (b) 600 GHz output signal exists.

AMC chain. Measured results from three different die-chip are demonstrated for each doubler circuit. Varactor doubler shows maximum output power of -19.25 dBm at 595 GHz. And it offers almost same amount of output power even with die-chip variation. Active doubler gives -22.81 dBm at best and die-chip variation is quite severe. If output power results are averaged for three die-chip, varactor doubler provide higher output power by the amount of 3.5 to 6.6 dBm in measured frequency range.

Measured output power and input power relation is shown in Fig. 9. Near quadratic behavior between input and output power can be observed from the result, which ensures that both circuits work properly for frequency doubling. It seems that the varactor doubler could not reach power saturation yet even with very high input power. So there might be possibility for getting higher output power with better design.

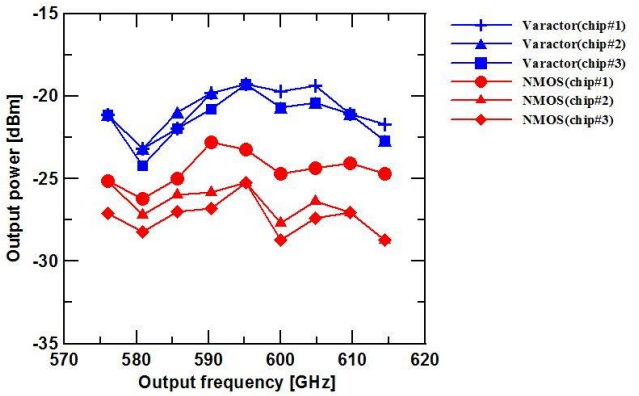



Fig. 8. Measured output power versus frequency. Maximum available source power is applied for each frequency point.

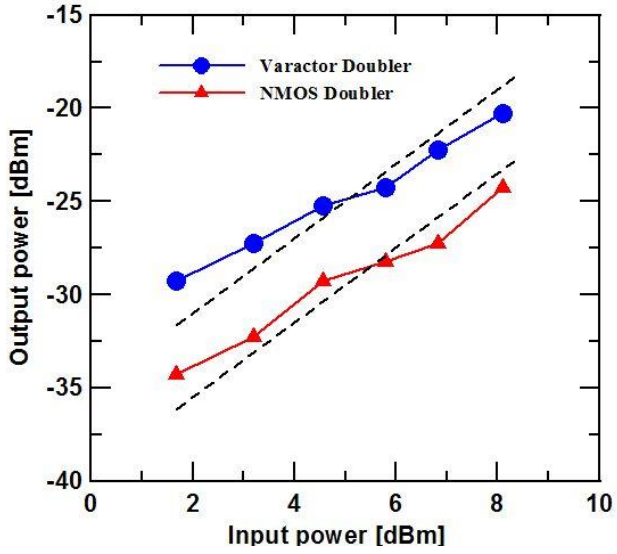



Fig. 9. Measured output power at 595 GHz with input power of 297.5 GHz.

## IV. CONCLUSIONS

Varactor and active mode doubler is fabricated and measured. The maximum output power of -19.25 dBm is achieved for varactor mode, which is 3.5 to 6.6 dBm higher than that of active mode doubler. Further increase in output power of varactor doubler may be realized by figuring out characteristic for non-linear varactor device.

## ACKNOWLEDGMENT

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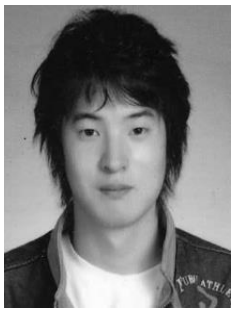

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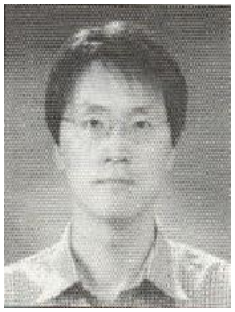

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