# A Linear CMOS Power Amplifier with Inter-stage Transformer

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***Abstract* - We designed the power amplifier using CMOS process. The gain reduction by the bonded-wire and the low breakdown voltage problem of the device in the CMOS process are alleviated by applying a differential cascode structure. In order to reflect the distortion of the linearity in the driver stage, it is designed as 2-stage. An RC-feedback network was applied to the power stage to achieve low output impedance as well as high output power and efficiency. It is implemented using Magna/SKhynix 0.18μm 1P6M CMOS process. The total size is 0.7 x 1.7 mm² including pads. No oscillation occurred in all the measured bands. As a measurement results, output power and PAE were about 23 dBm / 13% in the CW signal, 20 dBm / 10% in the LTE signal, 18 dBm / 3% in the WLAN signal.**

## I. INTRODUCTION

Today, mobile communications like 5G demand faster data transfer rates. To satisfy this requirement, the signal with high Peak-to-Average Power Ratio(PAPR) and wide bandwidth is used. Therefore, to meet these specifications, the power amplifier must satisfy the linearity indexes such as ACLR and EVM while maintaining high output power and efficiency.

Furthermore, various types of wireless communication such as Bluetooth and IOT as well as data transmission speed are popularized. Therefore, demand for various RF blocks is expected to increase.

Fig. 1. shows a typical RF block diagram. While most of the blocks are fabricated using CMOS processes, a large number of power amplifiers are being fabricated using compound semiconductor processes.

However, due to the development of the CMOS process, the possibility of fabricating a CMOS power amplifier is increasing. Integration with other RF blocks is also possible. It is considered to be competitive in low manufacturing cost, smaller area, and the like. Therefore, many researches on power amplifiers using CMOS process are progressing in various fields.

In this design report, we designed the power amplifier using CMOS process and measured whether it meets the linearity index.

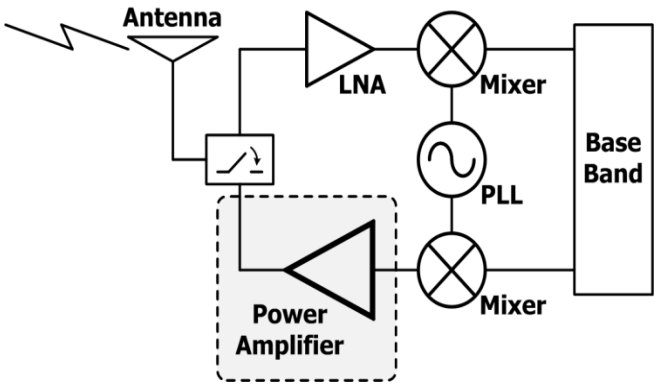


Fig. 1. RF block diagram

## II. DESIGN OF CMOS POWER AMPLIFIER

### *A. Differential cascade structure*

In designing power amplifiers, the CMOS process has some weak point on the performance compared to the compound semiconductor process. First, there is no via process to connect with back metal, so additional bonded-wire to ground is required. This additional bonded-wire to the ground affects the reduction in gain.

In this design, we tried to reduce the problem of gain reduction by using differential structure. We tried to reduce the influence of inductance of bonded-wire by virtual ground of differential structure.

The following are the lower breakdown voltages of CMOS processes compared to the compound semiconductor processes. The peak-to-peak voltage of the amplified signal at the output of the power amplifier rises to 2 ~ 3 times the VDD. When only a single device is used, the device breaks down due to the low breakdown voltage of the CMOS process. In order to solve such a breakdown voltage problem, a stack structure is widely used. In this design, we tried to reduce the breakdown voltage problem by applying the cascode structure to distribute the voltage across each device.

Fig. 2. show the circuit with the differential cascode structure mentioned above.

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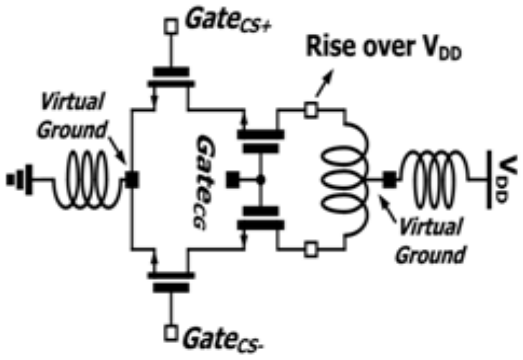


Fig. 2. Differential cascade amplifier

*B. 2-Stage power amplifier*

In order for the power amplifier to amplify sufficient output power, an appropriate power input must be provided to the power amplifier. If the input power is small, an additional driver stage should be added to amplify the input power. The driver stage of the power amplifier also has a higher output power than other RF blocks except for the power amplifier. Therefore, it is necessary to reflect the distortion of the linearity occurring in the driver stage.

If the power amplifier is to be integrated with other RF blocks in order to take advantage of the CMOS process in the future, the influence of the driver stage should be considered. So we designed a power amplifier with a driver stage to see this effect.

As shown in Fig. 2., the driver stage also requires an inductive load. In this design, a transformer is used to mitigate the asymmetry caused by the inductor in the differential structure.

A matching network was constructed for each amplifier using a transformer. The matching network consists of a transformer and a capacitor connected to each of the primary and secondary part of the transformer.

The overall block diagram of the power amplifier is shown in Fig. 3.

*C. RC-feedback network at power stage*

Power amplifiers require high supply voltage or low output impedance to have high output power. However, changing the supply voltage requires additional circuitry to convert the supply voltage. Because of this, we have to transform the impedance of 50 ohms to a low output impedance to have a high output power. However, it is difficult to obtain a high impedance transform ratio, and the larger the conversion ratio, the higher the sensitivity of the circuit. Therefore, conversion to a proper impedance is required.

The main purpose of the power amplifier is to amplify with high output power. Therefore, even if the required impedance transform ratio is not obtained, the circuit must be designed to achieve high output power and efficiency.

Obviously, the output power and efficiency are achieved at a high level, while the impedance characteristic of the output part is deteriorated. An RC-feedback circuit is applied to improve the impedance characteristics. Fig. 5.

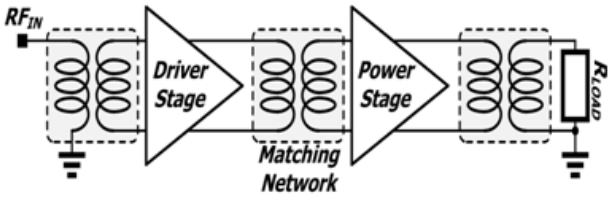


Fig. 3. 2-stage power amplifier with matching network using transformer

shows a series RC-feedback circuit connecting the gate and drain of the power stage. By applying this RC-feedback circuit, the impedance characteristic of the output is improved as shown in Fig. 4.

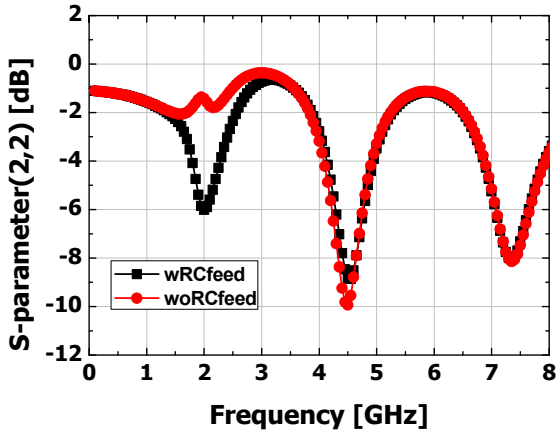


Fig. 4. S-parameter(2,2) of the 2-stage power amplifier w/wo RC-feedback circuit

*D. Design of CMOS power amplifier with RC-feedback network at power stage*

Fig. 4. shows a more detailed overall schematic. A balun for converting a single-ended signal to a differential signal was used for the input and output.

The transistor with triple well is used, and the size of transistor used is shown in the following table.

TABLE I.
Transistor parameters of the power amplifier

| Transistor name | Transistor size W/L[mm/um] |
|---|---|
| Driver, Common source | 1.0 / 0.18 |
| Driver, Common gate | 2.0 / 0.35 |
| Power-stage, Common source | 3.5 / 0.18 |
| Power-stage, Common gate | 4.0 / 0.35 |

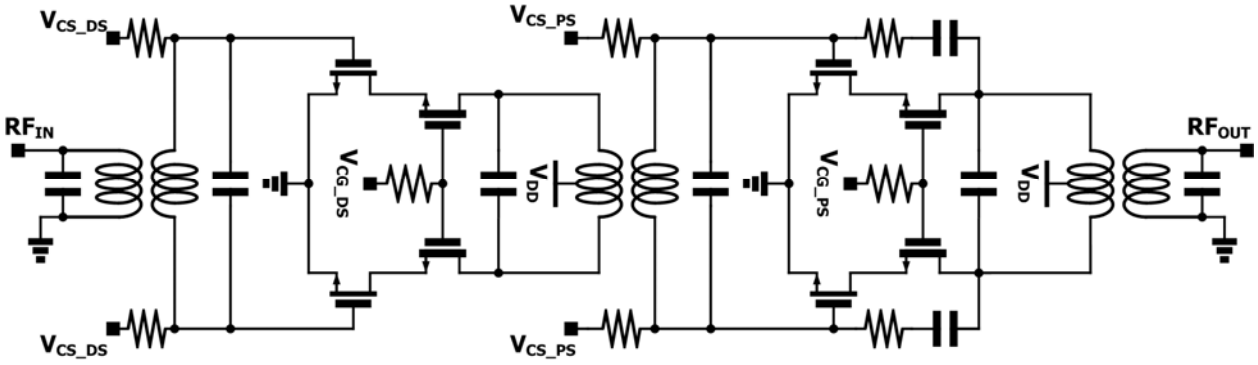


Fig. 5. Full schematic of the 2-stage power amplifier

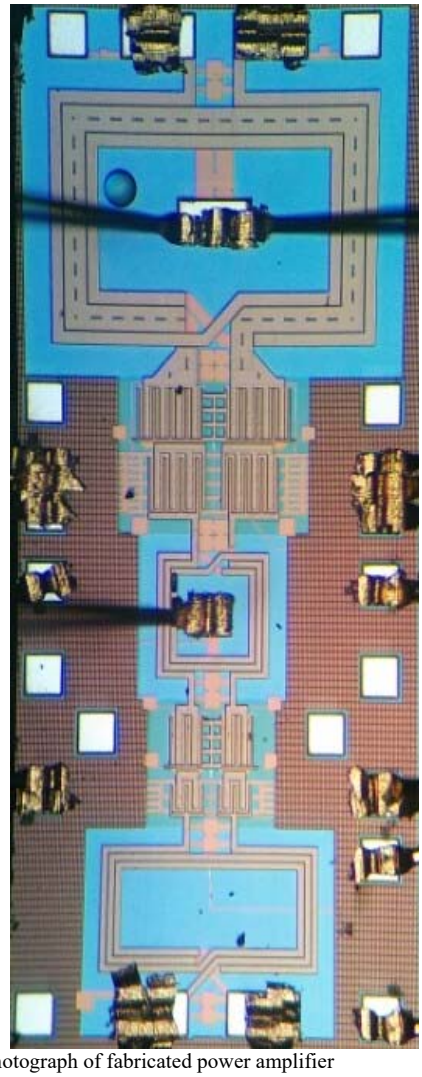

Fig. 6. Chip photograph of fabricated power amplifier

## III. EXPERIMENT RESULTS

The designed chip was fabricated using Magna/SK-hynix 0.18μm 1P6M CMOS process with 2μm UTM. The size of the chip is 0.7 x 1.7 mm² including the pads. Fig. 6. shows the chip photograph of the power amplifier.

The fabricated chip was connected to PCB via bonded-wire. The sample was measured by connecting it to a signal-generator, spectrum-analyzer, network-analyzer through a 50 Ω transmission line. The S-parameter, output power, efficiency, and linearity of the power amplifier were measured.

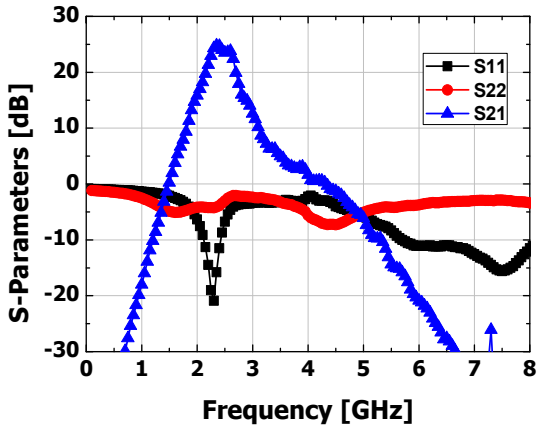


Fig. 7. Measured S-parameters of power amplifier

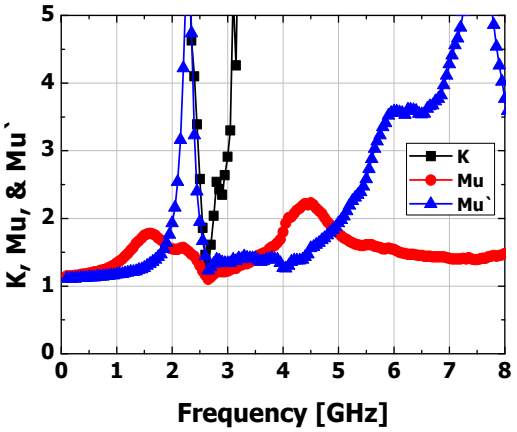


Fig. 8. Stability factor (K, Mu, Mu′) of power amplifier using measured S-parameters

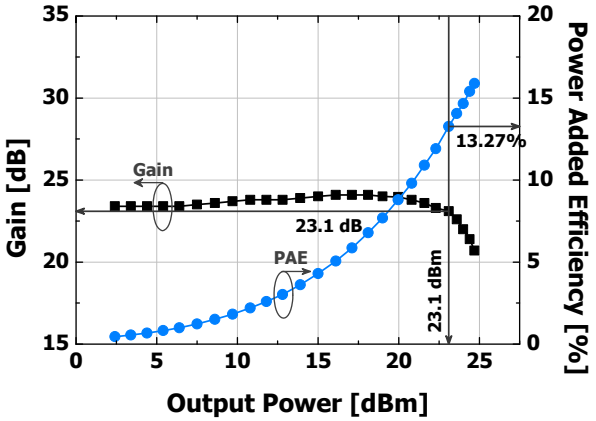


Fig. 9. Measured gain & PAE vs. output power of power amplifier using continuous signal

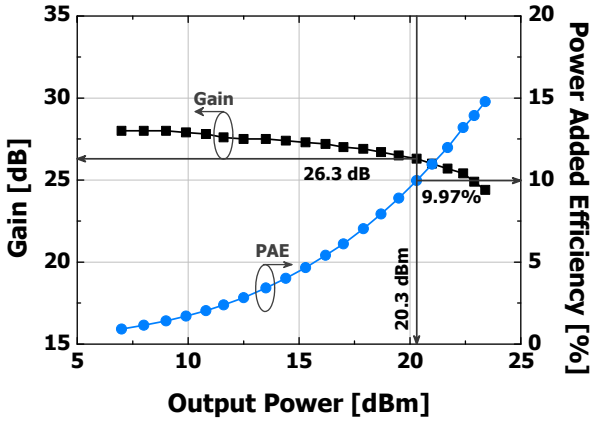


Fig. 10. Measured gain & PAE vs. output power of power amplifier using LTE 10 MHz signal

*A. Measurement results of continuous wave*

Fig. 7. shows the measured S-parameter values. At 2.3 GHz, S11 is about -20 dB, S22 is -4 dB, and S21 is about 24 dB. The results show that the parasitic component generated while constructing the power cell of the transistor slightly deviates from the target frequency.

Fig. 8. shows the stability factor of the measured s-parameter values. As shown in the figure, the stability factor measured is stable at 1 or more over the entire frequency range. Also, no oscillation signal was generated during spectrum measurement.

Fig. 9. shows the gain and PAE according to the output power in the CW signal.

The saturation power of the measured CW signal is approximately 24.5 dBm. The output power at P1dB is about 23 dBm and the PAE at P1dB is 13 %.

*B. Measurement results of LTE*

To verify the IMD characteristics of the power amplifier, ACLR values were measured using an LTE 10 MHz call. Fig. 10. shows the gain and PAE according to the output power in LTE signal. The maximum output power satisfying the linearity of the LTE signal is about 20 dBm, and the PAE at this time is about 10%.

You can see the ACLR value measured in Fig. 10. Despite the symmetrical layout using a transformer, it can be confirmed that the data of low and high is different as the output power increases.

Fig. 12. shows the captured image of the measurement device at a value that meets linearity.

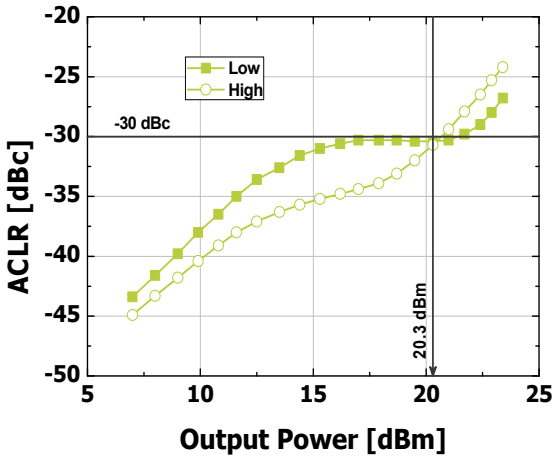


Fig. 11. Measured ACLR vs. output power of power amplifier using LTE 10 MHz signal

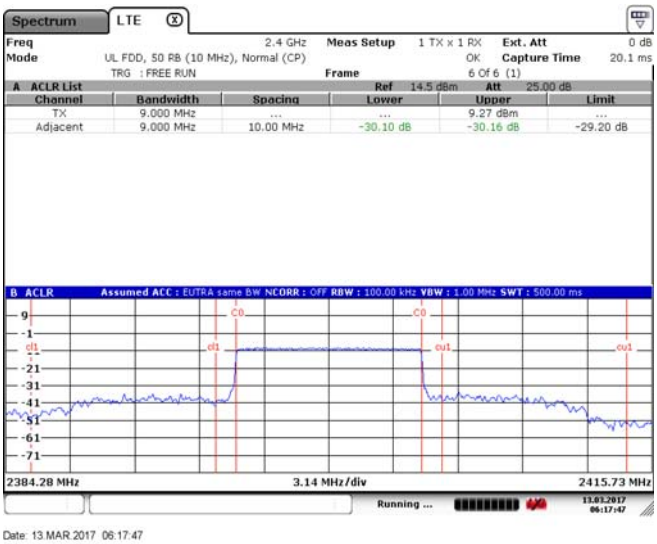


Fig. 12. Captured display of measured LTE ACLR results with 10 dB attenuation at spectrum analyzer

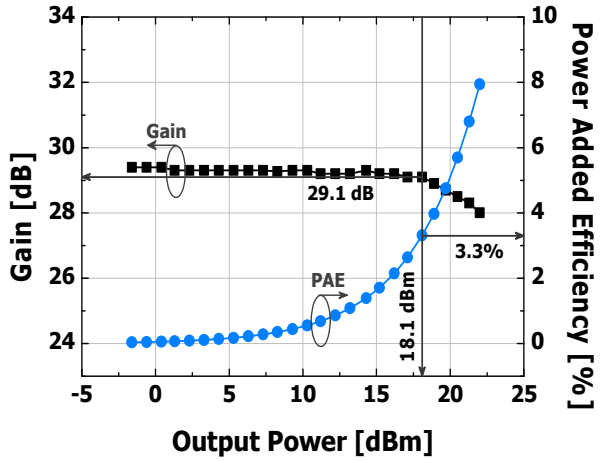


Fig. 13. Measured gain & PAE vs. output power of power amplifier using WLAN 20 MHz signal

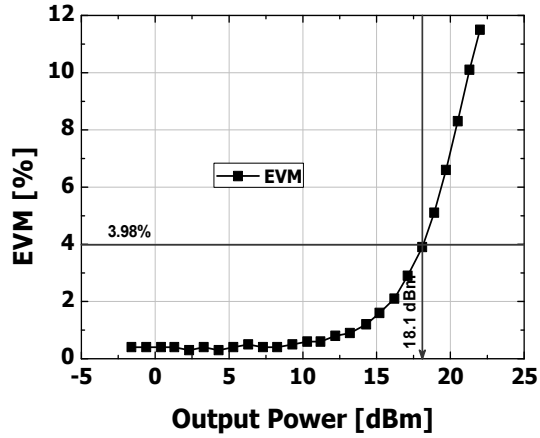


Fig. 14. Measured EVM vs. output power of power amplifier using WLAN 20 MHz signal

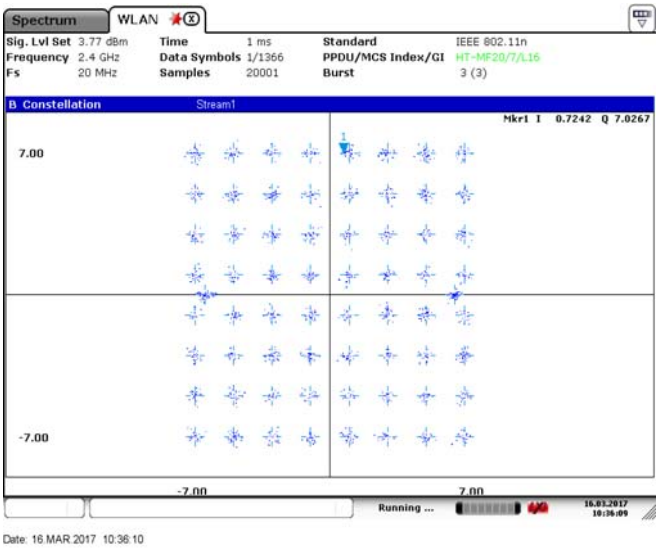


Fig. 15. Captured display of measured constellation WLAN 20 MHz at spectrum analyzer

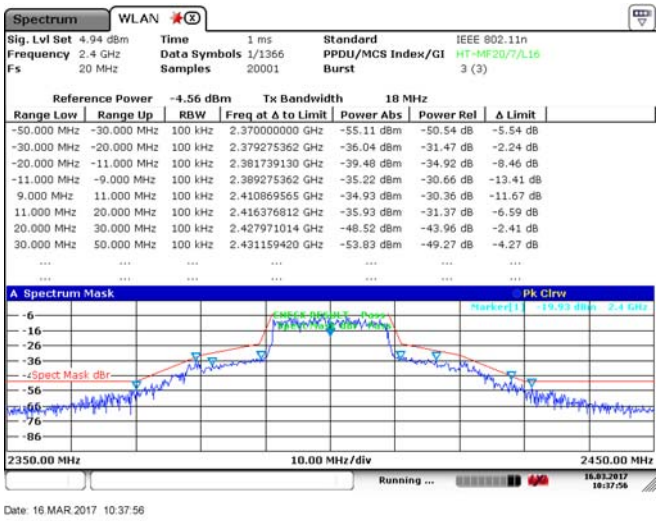


Fig. 16. Captured display of measured spectrum mask WLAN 20 MHz at spectrum analyzer

### *C. Measurement results of WLAN*

To verify the data error characteristics of the power amplifier, EVM values were measured using a WLAN 20 MHz 64-QAM signal. Fig. 13. shows the gain and PAE according to the output power in WLAN signal. The maximum output power that satisfies the linearity of the WLAN signal is about 18 dBm and the PAE at this time is about 3%. In the measurement of the WLAN signal, the bias value increased to satisfy the EVM value. Thus, the overall efficiency is reduced due to the higher quiescent current.

The measured EVM value can be seen in the fig. 14. In Fig. 15. and 16., you can see the captured constellation and spectrum mask image of the measurement device at a value that meets linearity.

## IV. CONCLUSIONS

We designed the power amplifier using CMOS process. The gain reduction by the bonded-wire and the low breakdown voltage problem of the device in the CMOS process are alleviated by applying a differential cascode structure. In order to reflect the distortion of the linearity in the driver stage, it is designed as 2-stage. In order to ensure high output power and efficiency as well as output impedance, an RC-feedback network was applied to the power stage. It is implemented using Magna/SKhynix 0.18μm 1P6M CMOS process. The total size is 0.7 x 1.7 mm² including pads. No oscillation occurred in all the measured bands. As a measurement results, output power and PAE were about 23 dBm / 13% in the CW signal, 20 dBm / 10% in the LTE signal, 18 dBm / 3% in the WLAN signal.

## ACKNOWLEDGMENT

This work was supported by the IDEC (IC Design Education Center).

## REFERENCES

[1] King-Chun TSAI and P. R. GRAY, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 7, pp. 962-970, 1999.

[2] I. Aoki, S. D. Kee, D. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 316-331, 2002.

[3] T. Joo, B. Koo, and S. Hong, "A WLAN RF CMOS PA With Large-Signal MGTR Method," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1272–1279, 2013.

[4] Y. Aoki, K. Kunihiro, T. Miyazaki, T. Hirayama, and H. Hida, "A 20-mA quiescent current two-stage W-CDMA power amplifier using anti-phase intermodulation distortion," *IEEE Radio Frequency Integrated Circuits (RFIC) Systems, Dig.*, pp. 357-360, 2004.

[5] H. Jeon et al., "A 40% PAE linear CMOS power amplifier with feedback bias technique for WCDMA applications," *IEEE Radio Frequency Integrated Circuits (RFIC) Systems, Dig.*, pp. 561-564, 2010.

[6] K. Onizuka, S. Saigusa, and S. Otaka, "A 1.8 GHz linear CMOS power amplifier with supply-path switching scheme for WCDMA/LTE applications," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 90–91, 2013.

[7] J. Jang, C. Park, H. Kim and S. Hong, "A CMOS RF Power Amplifier Using an Off-Chip Transmission Line Transformer With 62% PAE," *IEEE Microwave and Wireless Components Letters*, vol. 17, no.5, 2007.

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