Design of a 2.4 GHz Dual-mode CMOS power amplifier

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Abstract - **This paper presents a dual-mode CMOS power amplifier operating at 2.4 GHz. We propose a dual mode power amplifier which allows power to be delivered through different paths depending on the mode. We use one output matching network. In order to compensate to the disadvantages of using other techniques, a dual-mode operating only with bias control was designed. It is fabricated with Magna Hynix 0.18 ㎛ CMOS process. When continues wave (CW) signal is input, saturation power is measured to be about 21.6 / 12.9 dBm at high power mode / low power mode and power added efficiency (PAE) is measured to be about 7.38 / 6.13% at HPM / LPM. Also, gain is measured to be about 17.4 / 8.3 dB at HPM / LPM.**

***Keywords*—Bias control, Dual-mode CMOS power amplifier, Low-power power amplifier design**

I. INTRODUCTION

Recently, the performance index required for the Radio Frequency (RF) system has been improving with the advancement of the technology of the wireless communication system, and studies have been progressing accordingly. In order to develop the various performance of the power amplifier, various circuits are added to make a circuit suitable for the system. It is also necessary to consider industrial demand like size and cost. Therefore, power amplifiers (PAs) should be manufactured with a complementary metal-oxide semiconductor (CMOS) process.

As mentioned above, additional circuits are being added to improve the performance of the power amplifier. In addition, in order to operate in various power modes, some power amplifiers are designed to combine their powers. However, adding circuitry takes up additional area and increase the entire cost. This paper suggests a power amplifier that can reduce these disadvantages. We have one output transformer and tuned capacitor values for matching. Power amplifiers (PAs) should be manufactured with a (CMOS) process. However, CMOS has some process problems. Because of small band gap energy, CMOS has a low breakdown voltage. In addition, it is very difficult to use no substrate through via because the intensity of the silicon is low. To overcome these issues, we have used cascade structure and differential configuration. On the top of that, in order to use differential configuration, a transformer was needed. We have used transmission line transformer (TLT). Many papers have suggested a way to combine multiple power amplifiers to operate multiple modes of power. However, there are disadvantages such as size and power consumption, and so on. So we tried to minimize the disadvantages by sharing the high power mode (HPM) and the low power mode (LPM) of the transformer which occupies quite big area. In addition, RC feedback was added to fine-tune the S-parameter. Also, the operation of HPM and LPM is made through the switching of the gate bias.

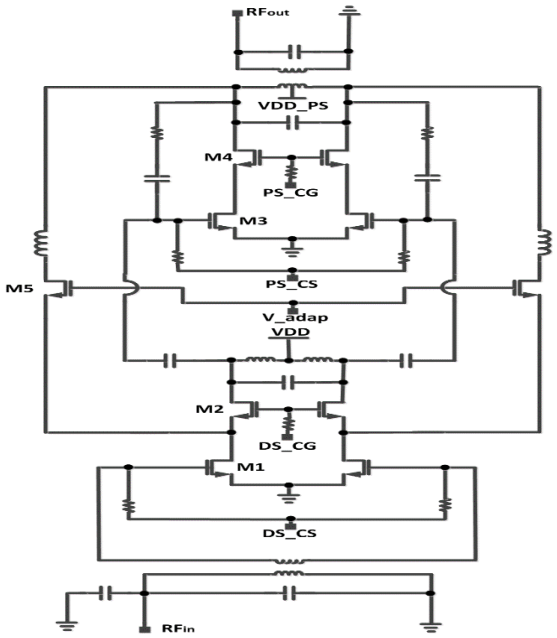

Fig.1. Schematic of proposed Power Amplifier

In Section II, a method is described to gain the dual-mode and CMOS power amplifier. Also, we propose the path and operation of the power amplifier according to the mode. Finally, we will suggest the structure and size of output transformer and input transformer for dual mode operation. In Section III, the chip implementation and measurement results are presented.

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II. DUAL-MODE CMOS POWER AMPLIFIER

A. Dual-Mode PAs

A CMOS process is used to implement a dual-mode Power Amplifier. CMOS power amplifiers (PAs) has many disadvantages compared to compound semiconductors. Through-via hole is one of them. To overcome this issue, CMOS PAs is used differential configuration to create a virtual ground. In addition, it cannot produce sufficient output power by a low breakdown voltage. In order to compensate for this, a cascode structure was selected. Designed with the cascode structure, high output power can be achieved. Fig.1 shows the schematic of the proposed dual-mode CMOS power amplifier.

We built a dual-mode power amplifier with one output transformer and bias control. The shape of the output transformer used for the most demanding matching process in producing dual-mode is shown in Figure 2. The size of the output transformer is 500x300 μm^2. Figure 4 shows the operational path for each mode. At High Power Mode, 0 V is applied to V_adap, M5 is off, and it operates in a two stage structure. When PA operates at low power mode, the transistors except the common source M1 of the drive stage used in HPM are off. Thus, M1 and M5 operate at low power with a cascode structure.

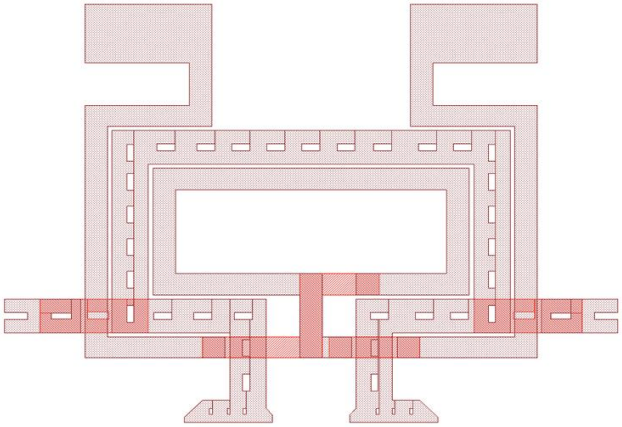


Fig.2. Proposed Output Transformer

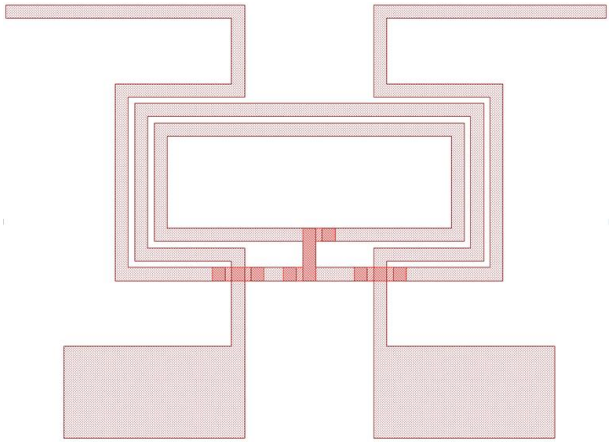
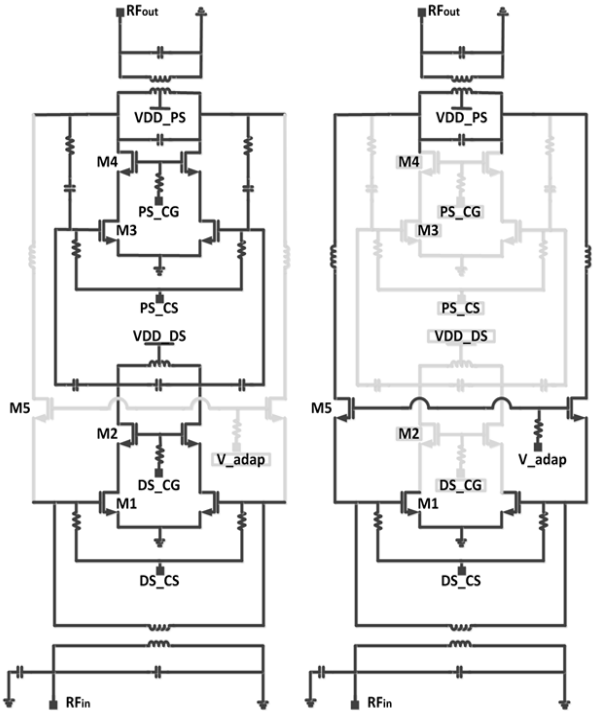


Fig.3. Proposed Input Transformer



(a) (b)

Fig.4. Operational path of the proposed dual-mode PA
(a) High Power Mode, (b) Low Power Mode

The total width of the common source transistor used to design drive stage of the power amplifier was 2.0 mm. And, the common gate transistor was 2.6 mm. We used 16 and 20 multi widths of 128. The total width of the common source transistor used to design power stage of the power amplifier was 3.1 mm. And, the common gate transistor was 3.8 mm. We used 24 and 30 multi widths of 128. And total width of M5 is 2.0. The size of the input transformer is 300x150 μm^2 and the size of the output transformer optimized for matching is 500x300 μm^2. TABLE I summarizes the transistor and transformer parameters of the proposed dual-mode power amplifier. The length of the transistor used in the common source is 0.18 μm and the length of the transistor used in the common gate is 0.35μm. The proposed structure is achieved not by combining two power amplifiers at the output stage but by controlling the number of transistors operating in each mode. In this process, the bias must be switched to control the operation of the transistor. In case of HPM, it operates in 2 stages. In case of LPM, it operates as 1stage and controls power.

TABLE I. Transistor and Transformer parameters of the proposed power amplifier

Device name	Size [W/L]
Drive Stage Common source transistor[M1]	2.0 mm/0.18 μm
Drive Stage Common gate transistor[M2]	2.6 mm/0.35 μm
Power Stage Common source transistor[M3]	3.1 mm/0.18 μm

Power Stage Common gate transistor[M4]	3.8 mm/0.35 μm
Low Power path Common gate transistor[M5]	2.0 mm/0.35 μm
Input transformer	300×150 μm^2
Output transformer	500×300 μm^2

B. Simulation Results

We built a dual-mode power amplifier with bias control with only one output transformer. The bias is Vdd, Common Gate CG, Common Source CS, and V_adap. Dual-mode operation operates by bias control. On the simulation, PS_CG / PS_CS / DS_CG / DS_CS / V_adap of high power mode is applied 2.4 / 0.6 / 2.0 / 0.6 / 0 (V). For low power mode operation, PS_CG / PS_CS / DS_CG / DS_CS / V_adap is applied at 0.0 / 0.0 / 0.0 / 0.7 / 2.3 (V). On the measurement, PS_CG / PS_CS / DS_CG / DS_CS / V_adap of HPM is applied at 2.4 / 0.73 / 2.0 / 0.75 / 0.0 (V). For low power mode operation, the PS_CG / PS_CS / DS_CG / DS_CS / V_adap is applied at 0.0 / 0.0 / 0.0 / 0.6 / 1.6 (V). Also, VDD is applied at 3.0 / 2.8 (V) for each mode measurement. Table II summarizes the bias used for simulation when a continue wave (CW) signal is input. We used a 6-layer while taking the thickness of the path where the signal passes. However, higher voltages were required for the operation of the transistor during the measurements. So the bias of the measurement is higher than the simulation. Figure 5 & 6 show the simulation result of S-parameter. It can be confirmed that S11 and S22 representing the reflection of the signal are low. As a result of simulation, S11 / S22 / S21 of HPM are -8.3 / -13.0 / 27.98 dB at 2.4 GHz. For low power mode operation, S11 / S22 / S21 are -7.29 / -4.72 / 15.14 dB at 2.4 GHz.

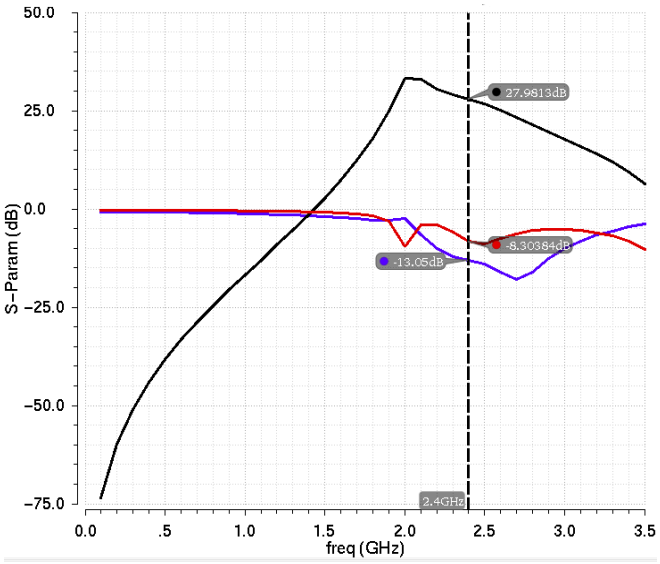


Fig.5. Simulation result of S-parameter [High Power Mode]

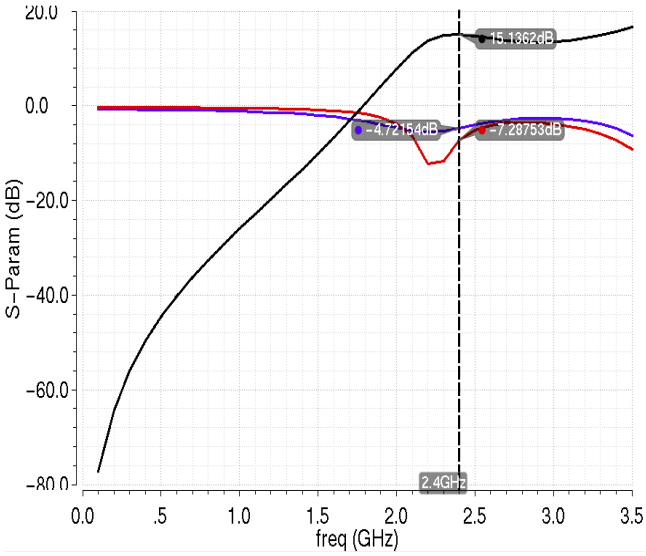


Fig.6. Simulation result of S-parameter [Low Power Mode]

TABLE II. Single-tone result of power amplifier “Simulation Bias Control”

Spec name	Result [HPM/LPM]
Vdd_PS	3.0 / 2.8 (V)
Vdd_DS	3.0 / 0.0 (V)
PS_CG	2.4 / 0.0 (V)
PS_CS	0.6 / 0.0 (V)
DS_CG	2.0 / 0.0 (V)
DS_CS	0.6 / 0.7 (V)
V_adap	0.0 / 2.3 (V)

Figure 7 & 8 are Simulation presenting Output Power (Pout) versus Gain and at HPM and LPM. The saturation output power of each mode is 27 / 18.5 dBm. The gain is 28.5 / 16 dB as a result of the simulation.

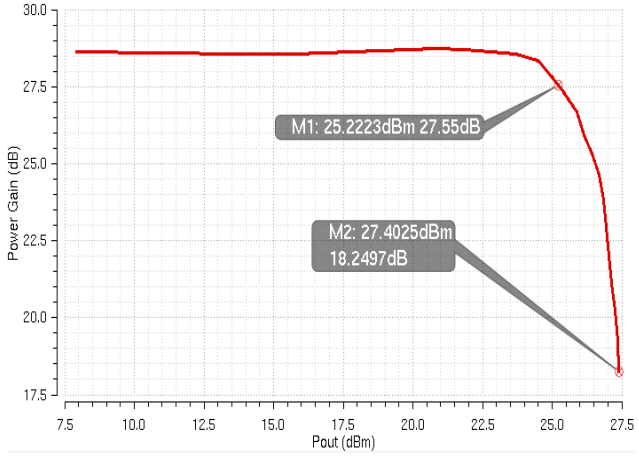


Fig.7. Simulation presenting Output Power (Pout) vs Gain at 2.4 GHz [High Power Mode]

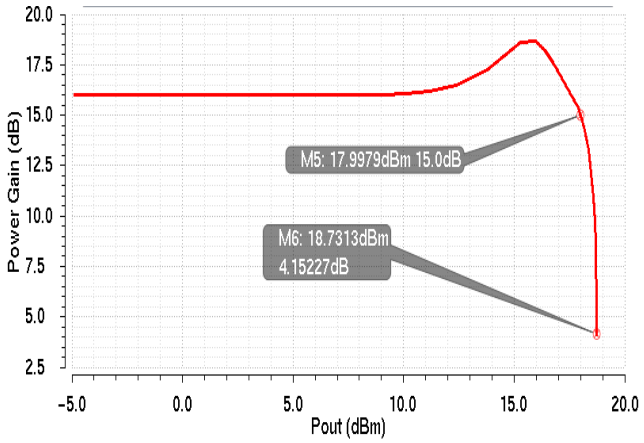


Fig.8. Simulation presenting Output Power (Pout) vs Gain at 2.4 GHz [Low Power Mode]

Figure 9 & 10 are Simulation presenting Power Added Efficiency (PAE) versus Input Power (Pin) at each mode. The maximum value of Power Added Efficiency (PAE) of each mode is 26.5 / 10.6%. The advantages of operating as both modes can be found in efficiency. The efficiency at 18.5dBm when operating with HPM is 7.7%. The efficiency at 18.5dBm in LPM is 10.6%. That is, the efficiency in the low power mode can be increased more linearly. TABLE III summarizes the simulation results for each mode. Each mode is determined by the bias.

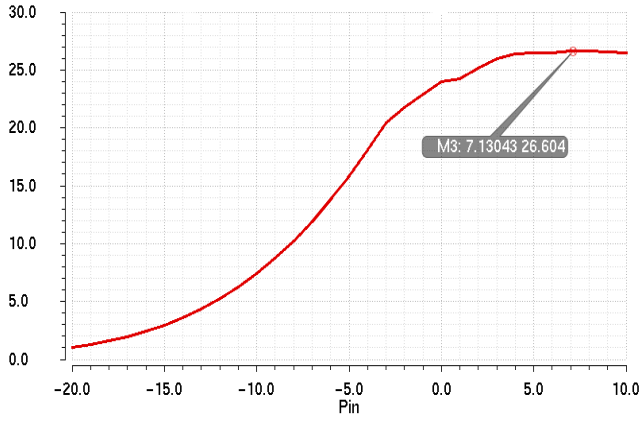


Fig.9. Simulation result of PAE vs Pin [High Power Mode]

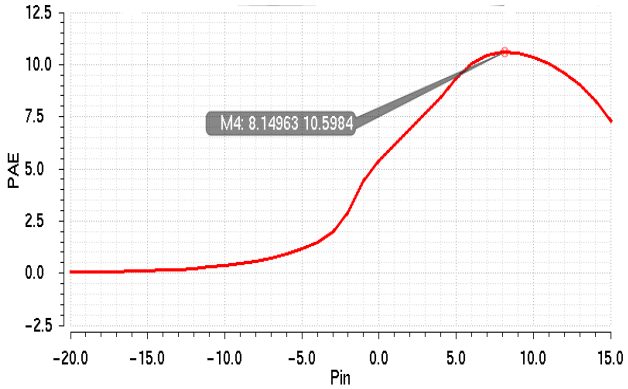


Fig.10. Simulation result of PAE vs Pin [Low Power Mode]

TABLE III. Single-tone simulation result of power amplifier "Simulation Results"

Spec name	Result [HPM/LPM]
S11	-8.3/-7.3(dB)
S21	28.0/15.1(dB)
S22	-13.0/-4.7(dB)
Gain	28.5/16(dB)
Pout	27.0/18.5(dBm)
P1dB	25.2/18.0(dBm)
PAE	20.3/15.3(%)

Figure 11 is layout of proposed power amplifier. The total area of chip including PAD is 1050 × 1370 μm^2

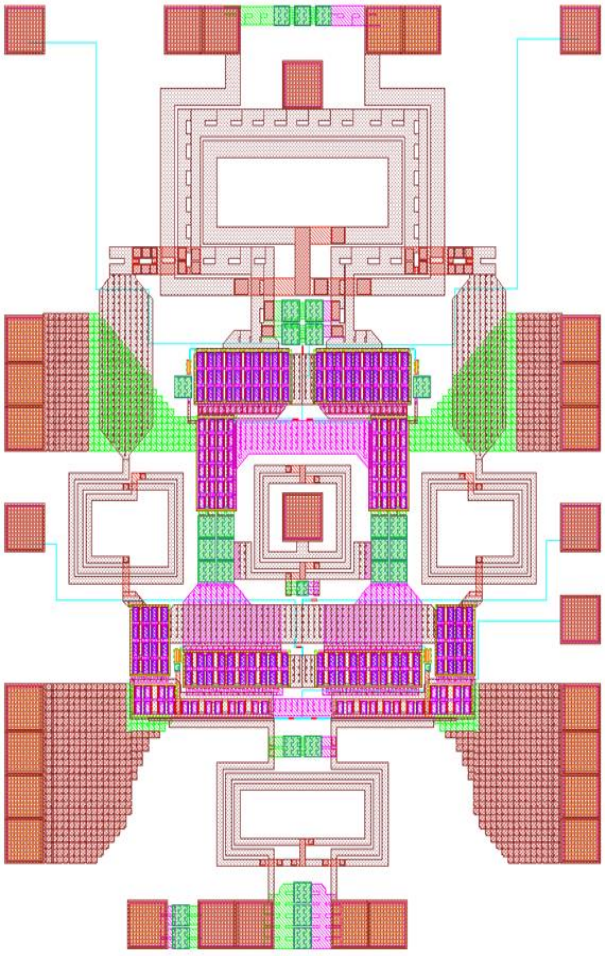


Fig.11. Layout of proposed Power Amplifier

III. MEASUREMENT RESULTS

As a result, we implemented a dual-mode CMOS power amplifier operating at 2.4 GHz. For the measurement, a pad was added around the chip, and the chip was attached to the PCB chip and measured. PCB was fabricated to be as close as possible to 50 ohms on a Smith chart at frequencies of 2.4 GHz. Figure 14 shows the photograph of the implemented PA. The total area of chip including PAD is 1050 × 1370 μm^2. The power supply was used to supply power to each bias input. As a result, Pout in each mode was 21.6 / 12.9 dBm at 2.09 / 2.37 GHz. The gain in each mode was 17.4 / 8.3 dB at 2.09 / 2.37 GHz. The PAE was 7.38 / 6.13% in each mode. And the PAE at 12.4 dBm was 1.15 / 6.13% in each mode.

TABLE IV. Single-tone result of power amplifier Measurement Bias Control

Spec name	Result [HPM/LPM]
Vdd_PS	3.0 / 2.8 (V)
Vdd_DS	3.0 / 0.0 (V)
PS_CG	2.4 / 0.0 (V)
PS_CS	0.73 / 0.0 (V)
DS_CG	2.0 / 0.0 (V)
DS_CS	0.75 / 0.6 (V)
V_adap	0.0 / 1.6 (V)

IV. CONCLUSION

This paper is for a dual-mode CMOS Power Amplifier operating at 2.4 GHz. We designed a dual-mode power amplifier with one output transformer. Especially, output transformer and matching network suitable for dual mode are designed. Performances have improved with additional circuits. However, disadvantages occur such as the increase of the total area size and high power consumption by adding circuits. We designed the power amplifier to minimize these disadvantages. We have achieved a saturation output power of 21.6 / 12.9 dBm in each mode. And power added efficiency (PAE) is measured to be about 7.38 / 6.13% in HPM / LPM. Also, PAE is measured to be about 1.15 / 6.13% at 12.4 dBm. And the measured gain is 17.4 / 8.3 dB in each mode.

ACKNOWLEDGMENT

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