Design of a High-Hole-Mobility Ge Transistor for Si-Driven Heterogeneous Integrated Circuits

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Abstract - **A high-hole-mobility transistor (HHMT) with an intrinsic Ge channel is optimally designed and its DC and high-frequency performances are investigated by technology computer-aided design (TCAD) simulation. An HHMT with a Ge channel and AlGaAs barrier on the Si substrate is characterized with a particular interest in the barrier design. More specifically, barrier doping concentration, total barrier thickness, and high-doped barrier thickness are considered as the critical design variables. A permissibly optimized device demonstrates cut-off frequency (f_T) of 20 GHz and maximum oscillation frequency (f_{max}) of 80 GHz at a channel length of 90 nm. The Ge HHMT with an AlGaAs barrier has the potential to be a component in the heterogeneously integrated monolithic circuits made of Si, group-IV alloys, and III-V compound semiconductors where electronic and optical devices can be simultaneously integrated with enhanced device performances.**

I. INTRODUCTION

Recently, Ge technology is gaining great deal of interest owing to its high electron ($\sim$3,900 cm^2/V·s) and hole ($\sim$1,900 cm^2/V·s) mobilities [1], which make Ge a candidate channel material for extending Si complementary metal-oxide-semiconductor (CMOS) technology. The most recent technology roadmap is mentioning Ge and III-V explicitly as the complements of Si in the advanced logic technologies in the near future [2]. However, in any case, there is sparse possibility of replacing Si platform, owing to cost-effectiveness and processing maturity of Si technology. In this paper, a high-hole-mobility transistor (HHMT) with an intrinsic Ge channel, which can be embedded in Si/Ge/III-V heterogeneous integrated circuits (ICs) and used in various electronic and photonic devices, is proposed and optimally designed by technology computer-aided design (TCAD) simulation. The optimally designed device demonstrates a 20-GHz cut-off frequency (f_T) and 80-GHz maximum oscillation frequency (f_{max}) at a channel length of 90 nm, which ensures the potential for use in the low-power high-speed

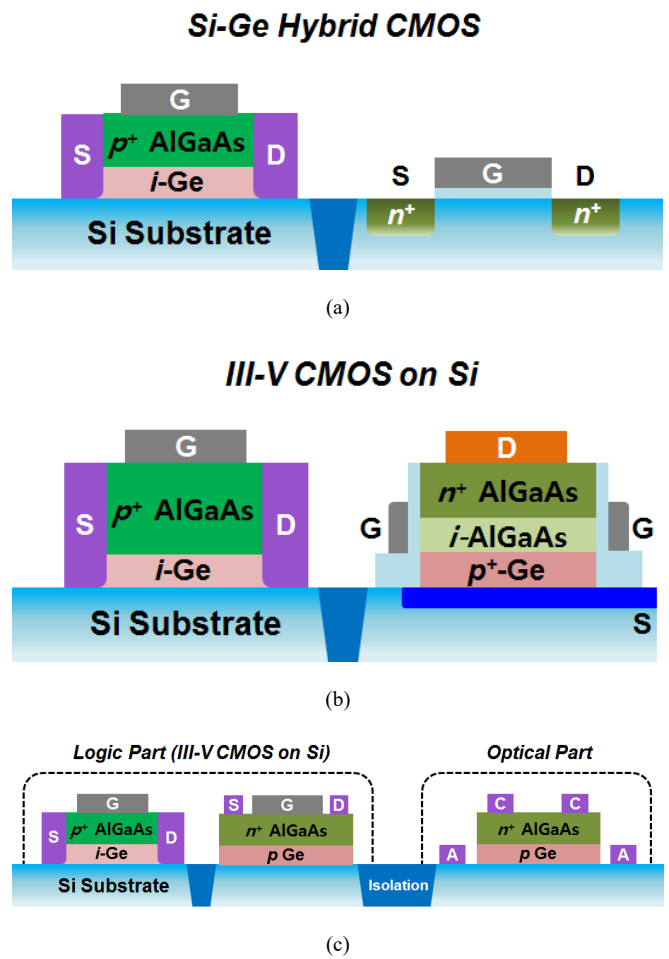heterogeneous ICs having wide applicability.

Fig. 1. Heterogeneous integration on the Si substrate. (a) Si/III-V hybrid CMOS: Si NMOSFET and Ge HHMT (*p*-type counterpart). (b) III-V CMOS on Si: *n*-type Ge vertical TFET and Ge HHMT. (c) Monolithic integration of CMOS and photonic circuits: logic part with Ge HHMT, and AlGaAs junctionless FET/optical part with 1,550-nm Ge LED, and related components.

II. SIMULATION APPROACH

A. Monolithic integrated circuits with Ge devices

Various possible approaches for heterogeneous integration

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of Si and non-Si materials can be schemed, as shown in Fig. 1(a) through 1(c). The Ge HHMT can be embedded as a *p*-type transistor to create a CMOS logic block in all the cases shown in the figures. Fig. 1(a) shows a Si-Ge hybrid CMOS circuit with a Si *n*-type MOS field-effect transistor (NMOSFET), with the Ge HHMT as the *p*-type counterpart [3–5]. The Ge HHMT can be co-integrated with a Ge-source tunneling field-effect transistor (TFET) to build a Si/Ge/III-V CMOS circuits, as shown in Fig. 1(b) [6–7]. The very-large-scale integration (VLSI) technology pursues evolutions both inside and outside the transistor. For the former, ways of more ideal switching characteristics featuring low-power and high-speed operation capabilities are sought, and for the latter, optical interconnect replacing the conventional metallic interconnect is widely studied [8–12]. The goal is to find a breakthrough for the extended use of Si CMOS in the high-density high-speed three-dimensional (3-D) VLSI systems. The optical interconnect consists of optical components including optical source, photodetector, modulator, and resonator, as well as the optical waveguide, that process electrical and optical signals. Therefore, intense research has been made to study various techniques for merging Si and non-Si with direct energy bandgap by novel material, device structure, and processing developments [13–17]. In order to satisfy the technical requirements, the optical components need to be brought together with Si. Fig. 1(c) shows one of the realizable ICs where a non-Si CMOS part is constructed by combination of Ge HHMT and Ge-buffered AlGaAs junctionless transistor, with the optical part composed of a light-emitting diode (LED) [6, 18–19]. As demonstrated in Fig. 1(a) through 1(c), the Ge HHMT can be very useful in building various heterogeneous ICS as the *p*-type electron device, with the advantages of process simplicity and compatibility with both Si and III-V semiconductor.

B. Design variables

Figure 2 shows the schematic of the simulated Ge HHMT with the design variables. In a previous study, DC characteristics were optimized in terms of primary variables including channel length, Ge channel thickness, and Al fraction in the AlGaAs barrier [6]. It is confirmed in this work that AC characteristics can be further optimized by controlling barrier dimension. The Ge HHMT with AlGaAs barrier in Fig. 2 has the structure of metal-semiconductor field-effect transistor (MESFET) where the barrier plays a role of isolating channel and gate as the gate oxide in the MOSFETs and its engineering is one of the crucial factors in determining the high-frequency performances of the device [20]. The design variables include the doping concentration of the AlGaAs barrier (N_B), the thickness of barrier (T_B), and the thickness of the partially high-doped region (T_{HB}) in a fixed T_B. The thickness of intrinsic Ge channel is fixed to 10 nm, and the two-dimensional hole gas (2DHG) is formed along the interface between the AlGaAs barrier and the Ge channel. In the simulation works, the Al fraction was kept to be 0.3 since there is a previous literature where Ge LED operated by Γ-Γ transport between direct-bandgap AlGaAs and indirect-bandgap confining the electrons near $k = 0$ in the momentum space is reported [19]. In order to obtain higher accuracy in the simulation results, complementary including

the field-dependent mobility model, concentration-dependent mobility model, Shockley-Read-Hall recombination model, and quantum-effect models were activated simultaneously. The doping concentrations of source/drain (S/D) junctions
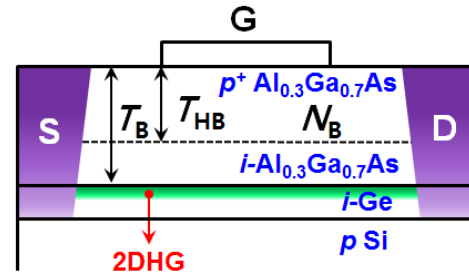

Fig. 2. Schematic of the Ge HHMT with AlGaAs barrier and the design variables.
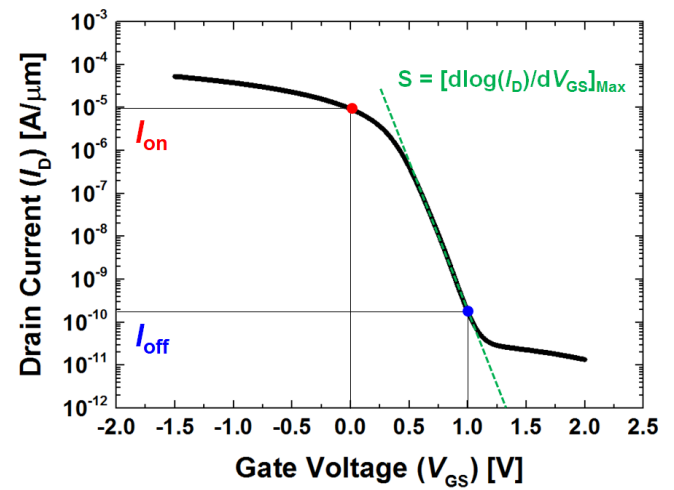

Fig. 3. Transfer characteristic curves at V_{DS} = -1.0 V.

and the Si substrate are *p*-type 1×10^{19} cm^{-3} and *p*-type 1×10^{15} cm^{-3}, respectively. The modeled electron affinity (χ) of Al$_{0.3}$Ga$_{0.7}$As as a function of the Al fraction is 3.74 eV [21], and that of Ge is 4.0 eV, which determines the conduction and valance band offsets in the Ge/ Al$_{0.3}$Ga$_{0.7}$As heterojunction. Fig. 3 shows the drain current (I_D) vs. gate-to-source voltage (V_{GS}) transfer curve at the high drain voltage (V_{DS}) of -1.0 V. It is revealed from the curve that the designed Ge HHMT is operated in the depletion mode so that a positive V_{GS} is required to cut off the channel. The on- and off-state currents (I_{on}, I_{off}) are obtained at V_{GS} = 0 V and 1.0 V, respectively. This confirms that the full on/off voltage swing can be confined to a magnitude within 1 V for low-power operation.

In the following simulation results, subthreshold swing (S) is defined as the reciprocal of the maximum instantaneous subthreshold slope (SS), as shown in Fig. 3. As mentioned in the previous part, T_B and T_{HB} are controlled as design variables. Although AlGaAs barrier can be prepared by an epitaxial growth technique during the device fabrication, an intrinsic AlGaAs region can be intentionally grown between the Ge channel and the high-doped AlGaAs barrier to keep the channel from being doped by thermal diffusion during the epitaxial growth of high-doped upper AlGaAs layer.

Therefore, the effects of T_{HB}, or equivalently, the effects of intrinsic AlGaAs layer thickness, on DC and high-frequency device performances are studied to determine more realistic design conditions.
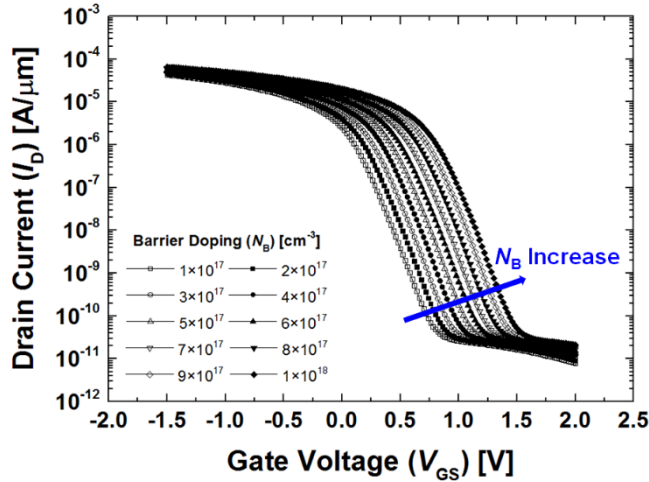

Fig. 4. Transfer curves of Ge HHMTs with different N_B's at V_{DS} = -1.0 V and T_B = 30 nm.

III. SIMULATION RESULTS AND DISCUSSION

A. Effects of barrier doping concentration

Figure 4 shows the I_D–V_{GS} transfer curves of Ge HHMT devices with different N_B values at V_{DS} = -1.0 V and T_B = 30 nm, without an intentional intrinsic AlGaAs region. N_B is varied from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}, with a step of 1×10^{17} cm^{-3}. Controlling N_B has the effect of shifting the threshold voltage (V_{th}) in the positive direction so that the device can be turned on more easily. This result can be understood by examining the graphical analysis results in Fig. 5(a) through 5(d), where the spatial energy-band diagrams of the Ge HHMTs at standby and drive modes have been obtained through device simulation. Here, the electron potential energy surfaces along the maximum valence bands are selectively shown in order to observe the behaviors of mobile holes confined in the Ge channel without being screened by the upper bands for better visibility. Figure 5(a) and (b) show the energy-band diagrams of Ge HHMT devices with a low barrier doping concentration of $N_B = 1 \times 10^{17}$ cm^{-3} in the standby and drive modes, respectively. Each mode corresponds to bias conditions of (V_{GS}, V_{DS}) = (1.0 V, -1.0 V) and (0 V, -1.0 V), respectively. Fig. 5(c) and (d) depict the energy-band diagrams of Ge HHMT devices with a high barrier doping concentration of $N_B = 1 \times 10^{18}$ cm^{-3} in the standby and drive modes, respectively. The actual electron potential energies can be read by the identically scaled color bar on the right side. The length and thickness of Ge channel are 90 nm and 10 nm, respectively, for all the devices, as indicated on the bottom grids. V_{GS} modulates the barrier height seen by the source holes toward the channel, regardless of N_B, as can be seen by the changes between Fig. 5(a) and (b) and between Fig. 5(c) and (d). Higher p-type doping elevates the energy band of the AlGaAs barrier since its Fermi level is positioned lower and it should be aligned with that of
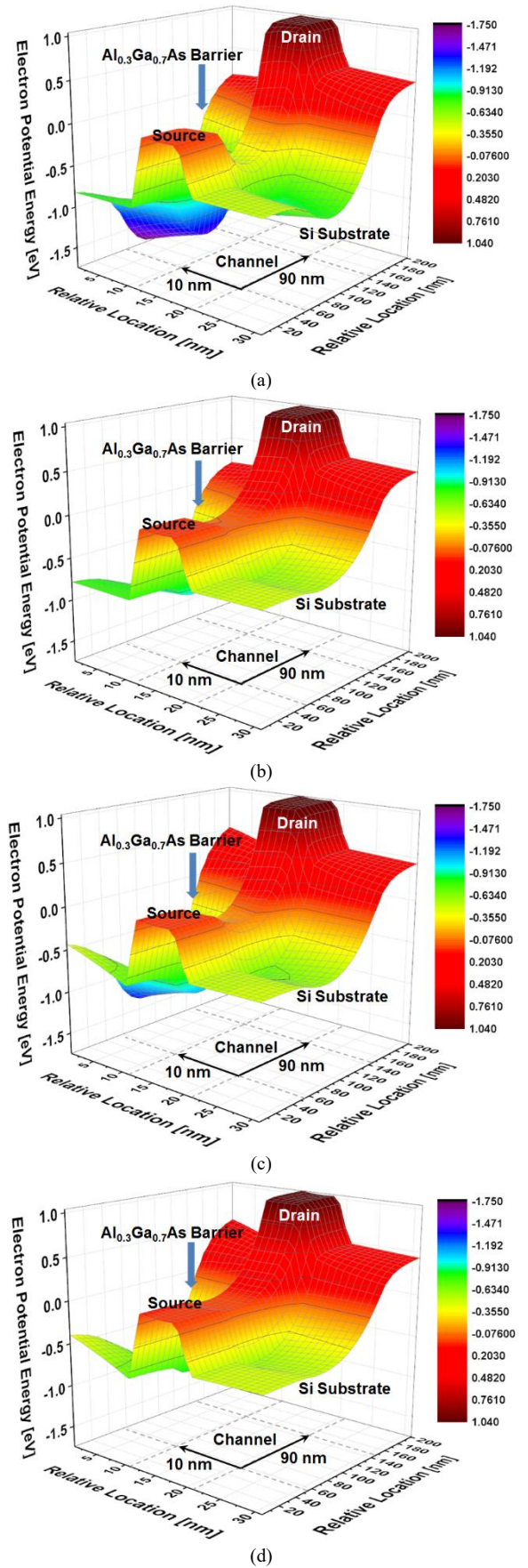

(a)

(b)

(c)

(d)

Fig. 5. Electron potential energy surfaces along the valence band maximum under different N_B and operation conditions. (a) $N_B = 1 \times 10^{17}$ cm^{-3}, standby. (b) 1×10^{17} cm^{-3}, drive. (c) 1×10^{18} cm^{-3}, standby. (d) 1×10^{18} cm^{-3}, drive.

gate metal at the interface. This interpretation is supported by comparison between Fig. 5(a) and (c) and between Fig. 5(b) and (d). The above results are projected to positive shift of V_{th} and relatively small change in I_{on}.

Figure 6 shows the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as a function of N_B when there is no intrinsic region in the AlGaAs barrier ($T_B = T_{HB} = 30$ nm).
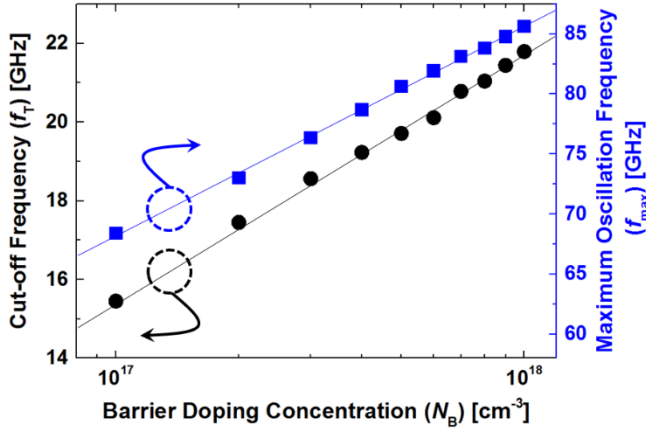

Fig. 6. Cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as a function of N_B. $T_B = T_{HB} = 30$ nm (no intrinsic region in the barrier).

Both f_T and f_{max} demonstrate monotonic increases with N_B, as shown in Fig. 6. f_T is 22.2 GHz and reduces down to 14.6 GHz, with a reduction magnitude below 10 GHz for decade reduction of N_B. f_{max} reaches 87.5 GHz at high N_B and shows relatively larger dependence on N_B. N_B affects total gate capacitance ($C_{gg,t}$) which is closely related with f_T and f_{max}, as can be revealed by Eq. (1)–(3) which originate from equations for MESFETS [20]:

$$C_{gg,t} = C_{gg} + C_{gd,p} + C_{gs,p} \qquad (1)$$

$$f_T = \frac{g_m}{C_{gg,t}} \qquad (2)$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{gd,t}}} \qquad (3)$$

In Eq. (1), $C_{gg,t}$ consists of intrinsic gate capacitance (C_{gg}), parasitic gate-to-drain capacitance ($C_{gd,p}$), and parasitic gate-to-source capacitance ($C_{gs,p}$). Here, subscript p indicates parasitic component. $C_{gd,p}$ and $C_{gs,p}$ mainly composed of outer fringing capacitances are much smaller than C_{gg} and are invariant with N_B, so that $C_{gg,t} \approx C_{gg}$ holds.

$$g_m = \frac{WC_{ox}'\mu_p}{L}\left|V_{GS} - V_{th}\right| \times (1-\alpha) \qquad (4)$$

$$C_{gg} = WLC_{ox}' \times \frac{2}{3}\frac{1+4\alpha+\alpha^2}{(1+\alpha)^2} \qquad (5)$$

Transconductance (g_m) is expressed as a function of gate overdrive as shown in Eq. (4), with a correction coefficient α.

μ_p is the hole mobility and C_{ox}' is the per-area gate oxide capacitance in the equivalent form of that in the MOSFETs, with one difference: the oxide is replaced by semiconductor material. Thus, the per-area gate oxide capacitance is expressed as $C_{ox}' = \varepsilon_s/t_b$, where ε_s and t_b are the permittivity and thickness of the AlGaAs barrier, respectively. C_{gg} can be also further refined by making use of the correction factor α as shown in Eq. (5).

f_T is expressed as a function of V_{GS} as shown in Eq. (6) by plugging Eq. (4) and (5) into Eq. (2) with an approximation of $\alpha \approx 0$ because f_T and f_{max} were extracted at the on-state (V_{GS}, V_{DS}) = (0 V, -1.0 V) and $V_{th} = 1$ V.

$$f_T \approx \frac{g_m}{C_{gg}} \approx \frac{\dfrac{WC_{ox}'\mu_p}{L}\left|V_{GS} - V_{th}\right|}{\dfrac{2}{3}WLC_{ox}'} = \frac{3\mu_p}{2L^2}\left|V_{GS} - V_{th}\right| \qquad (6)$$

f_T in Eq. (6) is further reduced as a simple function of only $|V_{th}|$ since $V_{GS} = 0$ at the drive mode. As $|V_{th}|$ gets larger, a higher f_T is obtained. Considering the above formula and the DC simulation results in Fig. 4, it is evident that higher N_B improves f_T. In Eq. (3), R_G and $C_{gd,t}$ are, respectively, the gate resistance and the total gate-to-drain capacitance as the sum of intrinsic (C_{gd}) and parasitic ($C_{gd,p}$) capacitances. $C_{gd,t}$ is mainly composed of C_{gd} which decreases with N_B due to the increased screening effect of the higher-doped AlGaAs barrier between the gate and drain junctions. In addition, higher doping in the AlGaAs barrier results in faster transfer of V_{GS} into the channel. Thus, a smaller $R_G C_{gd,t}$ product is obtained, which results in a higher f_{max} as N_B increases.

B. Effects of barrier thickness and modulation doping

Another design variable is T_B, the thickness of the AlGaAs barrier. Fig. 7(a) shows the I_D-V_{GS} curves from devices with different values of T_B. As the AlGaAs barrier gets thicker, both current drivability and subthreshold swing characteristics are degraded. As the result, it becomes more difficult to turn off the device at a small magnitude of positive V_{GS} and low-power operation capability is significantly threatened. Fig. 7(a) indicates that T_B needs to be no larger than 30 nm in order to keep the magnitude of high V_{GS} below 1 V for a sufficiently low leakage current and low-power operation of the normally-on Ge HHMT. Fig. 7(b) shows the gate leakage current (I_G) at different values of T_B. Unlike that of MOSFET structures, I_G is determined by the energy barrier seen by conduction holes in the Ge channel toward the AlGaAs barrier. I_G increases as T_B increases, as shown in the figure. If the permissible I_G is limited to 1 pA/μm, T_B should be kept below 30 nm. Since the AlGaAs barrier acts as an insulator between the gate electrode and the Ge channel in DC operations of the designed Ge HHMT, a thinner barrier provides higher gate controllability over the channel. As a result, a smaller T_B improves the DC characteristics of the Ge HHMT, including higher current drivability, smaller subthreshold swing, and lower gate leakage. This is confirmed by Fig. 7(a) and (b). In this sense, T_B would be also a critical variable for improving DC performances. Although a smaller T_B is desirable for better DC performances, T_B below 15 nm might not be practical since the effect of an

ultra-thin barrier in suppressing I_G is saturated, as can be confirmed by Fig. 7(b). Instead, it may be considerably challenging to obtain the thickness using conventional epitaxy tools with high enough repeatability and throughput.

Fig. 8 depicts f_T and f_{max} of Ge HHMT as functions of T_B. Both f_T and f_{max} increase as T_B increases and they are eventually saturated above a certain thickness. This implies that T_B should have a lower limit and it appears to be 30 nm
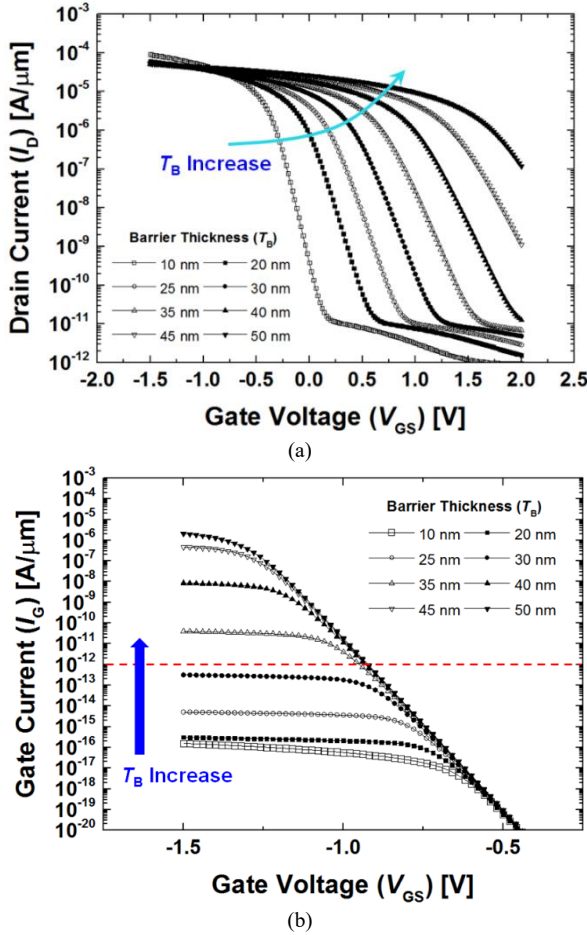

(a)

(b)

Fig. 7. Optimization of DC characteristics. (a) Transfer curves and (b) gate leakage of Ge HHMTs with different T_B's. $N_B = 10^{18}$ cm^{-3} and V_{DS} = -1.0 V.
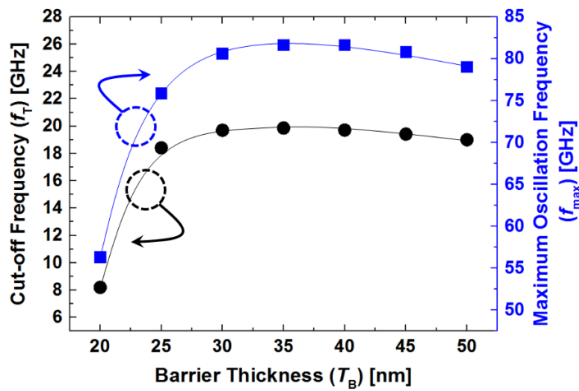

Fig. 8. f_T and f_{max} as a function of T_B. $N_B = 5 \times 10^{17}$ cm^{-3} and V_{DS} = -1.0 V. The curve with black circle and left-headed arrow depicts f_T and that with blue circle and right-headed arrow indicates f_{max}.

under the given condition of $N_B = 5 \times 10^{17}$ cm^{-3} at V_{DS} = -1.0. Above this thickness, the characteristic frequencies become rather invariant with T_B. This result would provide an optimized T_B in conjunction with the results in Fig. 7(a) and (b). For a sharp logic switching by a small magnitude of V_{GS} sweep between the off-state and on-state, T_B should be kept near 30 nm below 40 nm for effective suppression of I_G below 1 pA/µm. Therefore, T_B should be designed with a thickness near 30 nm to achieve both reliable DC and high-frequency device performances.
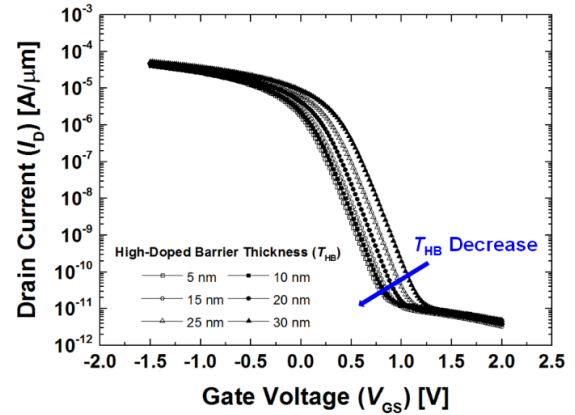

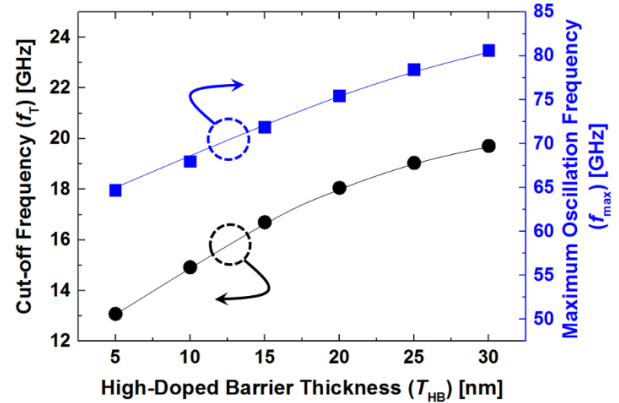Fig. 9. Transfer curves. $N_B = 5 \times 10^{17}$ cm^{-3} and T_B = 30 nm at V_{DS} = -1.0 V.

Fig. 10. f_T and f_{max} as a function of T_{HB}. $N_B = 5 \times 10^{17}$ cm^{-3} and V_{DS} = -1.0 V. The curve with black circle and left-headed arrow depicts f_T and that with blue circle and right-headed arrow indicates f_{max}.

The AlGaAs barrier can be vertically segmented to have regions with high and low doping concentrations, which prevents unwanted diffusion of dopants from the barrier to the intrinsic channel region. As previously shown in Fig. 2, the thickness of the high-doping region (T_{HB}) takes a portion out of T_B and is varied from 5 nm to 30 nm while keeping T_B = 30 nm in order to investigate dependence of device performances on T_{HB}. Fig. 9 shows the I_D–V_{GS} curves at different values of T_{HB}. Although there is no significant change in the transfer characteristics, it is observed that the transfer curve moves toward the left side and I_{on} (I_D at V_{GS} = 0 V and V_{DS} = -1.0 V) is degraded as T_{HB} decreases. Therefore, for higher I_{on}, a sufficiently thick T_{HB} needs to be designed. Higher current drivability is closely related to f_T and f_{max}, as can be seen in Eq. (2) and (3). Fig. 10 depicts f_T and f_{max} as a function of T_{HB}. f_T increases from 13.1 GHz to

19.7 GHz, and f_{max} shows a monotonic increase from 64.7 GHz to 80.6 GHz as T_{HB} increases from 5 nm to 30 nm. The effects of T_{HB} on the transfer characteristics and high-frequency parameters of Ge HHMT are relatively small compare with those of N_B as can be confirmed by Fig. 4 and 7 and those of T_B demonstrated in Fig. 7(a) and 8, and less critical in device design. The weak dependencies of DC and high-frequency device performances on T_{HB} ensure that a large process margin in constructing the high-doped AlGaAs barrier region can be obtained only if the intrinsic channel is not significantly intruded by unwanted dopant diffusion.

IV. CONCLUSION

In this study, we proposed a Ge HHMT and closely investigated the effects of AlGaAs barrier doping concentration, uniformly doped barrier thickness, and high- and low-doping barrier thicknesses on DC and high-frequency device performances for optimal design. By rigorous and systematic TCAD simulation, I_{on} near 10^{-4} A/μm, I_{off} below 10 pA/μm, f_T of 19.7 GHz, and f_{max} of 80.6 GHz have been obtained. The proposed Si/Ge/III-V device has the strong potential for use in the heterogeneous integrated circuits for the advanced VLSI technology on Si platform realizing the single-chip electronics and photonics.

REFERENCES

[1] C. Claeys and E. Simoen, Germanium-Based Technologies: From Materials to Devices, Elsevier, Oxford, UK, pp. 309, 2007.

[2] Process Integration, Devices, and Structures (PIDS) Chapter, International Technology Roadmap for Semiconductors (ITRS), 2013 Ed. Online available at http://www.itrs.net.

[3] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," IEDM Tech. Dig., pp. 1–4, Dec, 2006.

[4] S. Takagi and M. Takenaka, "High Mobility CMOS Technologies using III-V/Ge Channels," IEEE Nanotechnology Materials and Devices Conference (NMDC), no. MP-CK-3, Oct, 2013.

[5] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High-Mobility Ge PMOSFET With 1-nm EOT Al_2O_3/GeO_x/Ge Gate Stack Fabricated by Plasma Post Oxidation," IEEE Transactions on Electron Devices, vol. 59, no. 12, pp. 335–341, Feb, 2012.

[6] S. Cho, I. M. Kang, K. R. Kim, B.-G. Park, and J. S. Harris, Jr., "Silicon-compatible high-hole-mobility transistor with an undoped germanium channel for low-power application," Applied Physics Letters, vol. 103, no. 22, pp. 222102-1–222102-4, Nov, 2013.

[7] S. Cho, I. M. Kang, T. I. Kamins, B.-G. Park, and J. S. Harris, Jr., "Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation," Applied Physics Letters, vol. 99, no. 24, pp. 243505-1–243505-4, Dec, 2011.

[8] J. W. Goodman, F. I. Leonberger, S.-Y. Kung, and R. A. Athale, "Optical Interconnections for VLSI Systems," Proceeding of the IEEE, vol. 72, no. 7, pp. 850–866, Jul, 1984.

[9] D. A. B. Miller, "Optics for low-energy communication inside digital processors: quantum detectors, sources, and modulators as efficient impedance converters," Optics Letters, vol. 14, no. 2, pp. 146–148, Jan, 1989.

[10] D. A. B. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," Proc. IEEE, vol. 88, no. 6, pp. 728–749, Jun. 2000.

[11] D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proceeding of the IEEE, vol. 97, no. 7, pp. 1166–1185, Jul, 2009.

[12] S. Cho, H. Kim, M.-C. Sun, B.-G. Park, and J. S. Harris, Jr., "Process Considerations for 80-GHz High-Performance p-i-n Silicon Photodetector for Optical Interconnect," Journal of Semiconductor Technology and Science, vol. 12, no. 3, pp. 370–376, Sep, 2012.

[13] V. A. Shah, A. Dobbie, M. Myronov, and D. R. Leadley, "High quality relaxed Ge layers grown directly on Si(001) substrate," Solid-State Electronics, vol. 62, no. 1, pp. 189–194, Aug, 2011.

[14] K. W. Ng, W. S. Ko, T.-T. D. Tran, R. Chen, M. V. Nazarenko, F. Lu, V. G. Dubrovskii, M. Kamp, A. Forchel, and C. J. Chang-Hasnain, "Unconventional Growth Mechanism for Monolithic Integration of III-V on Silicon," ACS Nano, vol. 7, no. 1, pp. 100–107, Dec, 2012.

[15] J. Xie, A. V. G. Chizmeshya, J. Tolle, V. R. D'Costa, J. Menendez, and J. Kouvetakis, "Synthesis, Stability Range, and Fundamental Properties of Si-Ge-Sn Semiconductors Grown Directly on Si(100) and Ge(100) Platforms," Chemistry of Materials, vol. 22, no. 12, pp. 3779–3789, May, 2010.

[16] K. Majumdar, P. Thomas, W.-Y. Loh, P.-Y. Hung, K. Matthews, D. Pawlik, B. Romanczyk, M. Filmer, A. Gaur, R. Droopad, S. L. Rommel, C. Hobbs, and P. D. Kirsch, "Mapping Defect Density in MBE Grown $In_{0.53}Ga_{0.47}As$ Epitaxial Layers on Si Substrate Using Esaki Diode Valley Characteristics," IEEE Transactions on Electron Devices, 61, no. 6, Jun, 2014.

[17] D.-M. Keum, S. Choi, Y. Kang, J.-G. Lee, H.-Y. Cha, and H. Kim, "Temperature-Dependent Instabilities of DC Characteristics in AlGaN/GaN-on-Si Heterojunction Field Effect Transistors," Journal of Semiconductor Technology and Science, vol. 14, no. 5, pp. 682–687, Oct, 2014.

[18] S. Cho, S. H. Park, B.-G. Park, and J. S. Harris, Jr., "Silicon-Compatible Bulk-Type Compound Junctionless Field-Effect Transistor," IEEE International Semiconductor Device Research Symposium (ISDRS), pp. 1–2, Dec, 2011.

[19] S. Cho, B.-G. Park, C. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. B. Yoo, and J. S. Harris, Jr., "Room-temperature electroluminescence from germanium in an $Al_{0.3}Ga_{0.7}As$/Ge heterojunction light-emitting diode by Γ-valley transport," Optics Express, vol. 20, no. 14, pp. 14921–14927, Jul, 2012.

[20] W. Lin, Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs, Wiley Inter-Science, New York, NY, 1999.

[21] J. S. Harris, Jr., Class Notes from EE327 Properties of Semiconductor Materials, Stanford University, 2013.

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