DC Parametric Measurement Unit using Differential Difference Amplifier with a Full Operation Range

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***Abstract* - In this paper, a new DC PMU (parametric measurement unit) using DDA (differential difference amplifier) with dynamic common-mode voltage (DCMV) technique and new connection structure is proposed to overcome the structural limitations of prior PMU composed of differential difference amplifier. And the proposed PMU was implemented with 0.18um CMOS process. Since the proposed DC PMU has simple structure and there is no additional amplifier in the negative feedback loop, the system stability is guaranteed. It is confirmed that the operating range of the forcing voltage mode is 0.25~1.55V, the operating range of the forcing current mode is -20~20mA, and these forcing modes have maximum errors of 1.28% and 1.43%, respectively.**

I. INTRODUCTION

Automatic test equipment (ATE) is used to confirm the function and performance of the semiconductor chips or display devices. The ATE has AC test and DC test, and from among these the equipment for DC test is called DC parametric measurement unit (PMU) [1]. The DC PMU must have four functions such as forcing DC voltage, forcing DC current, measuring DC voltage and measuring DC current [2]. Using these functions, it can be configured in four modes such as force voltage-measure voltage (FVMV), force voltage-measure current (FVMI), force current-measure voltage (FIMV) and force current-measure current (FIMI) [3]. Conventional DC PMU consists of 5 amplifiers and 4 resistors as shown in Fig. 1[4]. This conventional structure has some design issues. First, it suffers from offsets and mismatch errors caused by several devices. The second issue is stability problem caused by using several op-amps in feedback loop. To solve these problems, the PMU using differential difference amplifier (DDA) is proposed [5]. The PMU using DDA consists of only two DDAs. And, there is no additional amplifier in the feedback loop. So, the offset and mismatch error are minimized and the system stability was guaranteed. However, the FVMI mode of the PMU using DDA has very narrow operating range due to structure limitation of instrument amplifier (IA) using DDA in [5]. To overcome the problem of prior PMU using DDA [5], in this paper, dynamic common-mode voltage technique and new connection structure are applied. It can be implemented without additional circuits and power consumption.

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II. REVIEW OF PRIOR CIRCUITS

A. Conventional DC Parametric Measurement Unit [4]

Fig. 1 shows the conventional DC PMU block diagram that consists of 5 op-amps and 4 resistors including IA using 3 op-amps [4]. The DC PMU has four functions of forcing voltage, forcing current, measuring voltage and measuring current. The op-amp A1 has two functions for forcing voltage or current. Each function can be implemented by choosing one of the two feedback loops. To force voltage or current, A1 is configured as a unity gain buffer or voltage controlled current source (VCCS) by respectively selecting the feedback loop including unity-gain buffer A5 or another feedback loop including the IA that is consists of 3 op-amps [6]. But, this conventional structure has some problem related with offset, mismatch and stability caused by several op-amps and resistors and the feedback loop including op-amps.

B. Prior PMU using DDA [5]

To solve the problems of the conventional structure, DC PMU using DDA has been proposed [5]. Fig. 2 shows the block diagram of DC PMU using DDA that consists of only two DDAs. The DDA of A6 is used to force the voltage or

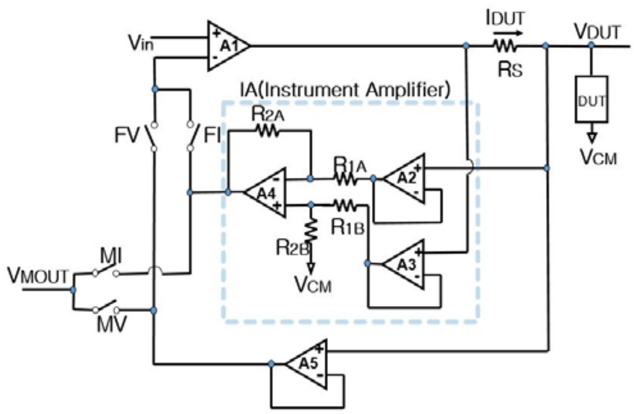


Fig. 1 Block diagram of conventional DC PMU

current to the device under test (DUT), and the DDA of A7 is used to measure the reacted voltage or current from the DUT. To perform each function, the A6 is configured as the unity gain buffer or VCCS, and the A7 can be configured as the unity gain buffer or IA. As such, each DDA has two functions and performs its role by changing the connection structure as needed [7]. Since, the conventional IA composed of three op-amps is replaced by one DDA of A7, the output error due to the offset and mismatch is minimized. In addition, the stability of the PMU using DDA was guaranteed by removing the multiple poles from many op-amps in the feedback loops [8]. But the prior PMU using DDA still has a problem of limited operating range in FVMI mode due to the structural limitations of the IA using DDA.

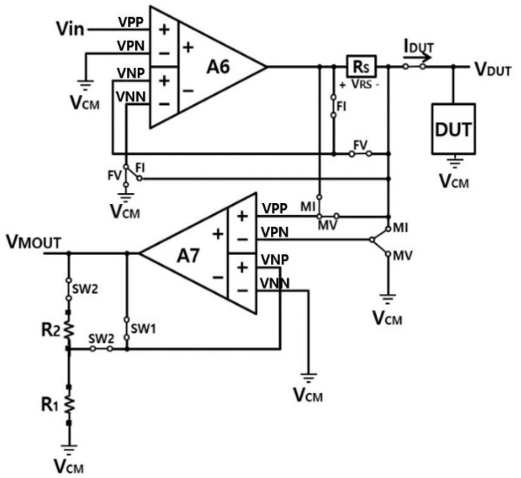


Fig. 2 Block diagram of prior DC PMU using DDA [5]

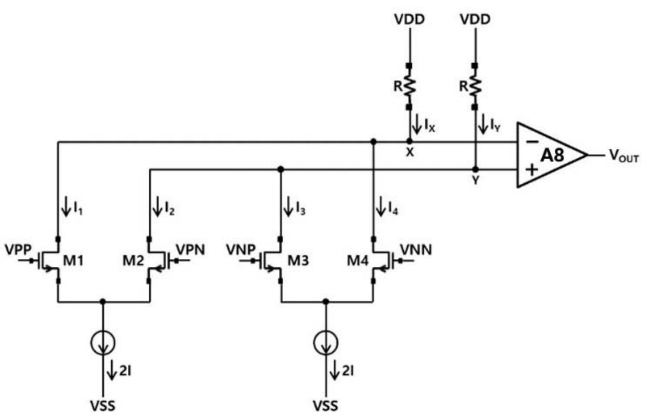


Fig. 3 Circuit diagram of differential difference amplifier

C. Structural Limitations of IA using DDA

Fig. 3 shows the simple schematic of the DDA to understand the problem of the IA used in FVMI mode [9]. The DDA consists of the input stage with two differential input pairs and one amplifier. The currents flowing in the two differential pairs have the relationship of equation (1), and the currents I_X and I_Y are expressed by the equations (2) and (3), respectively.

$$I_1 + I_2 = I_3 + I_4 = 2I \quad (1)$$

$$I_X = I_1 + I_4 \quad (2)$$

$$I_Y = I_2 + I_3 \quad (3)$$

The two input voltages of the A8, V_X and V_Y are expressed by equations (4) and (5), respectively. And these two voltages become equal due to the virtual short property of opamp [10]. Using these properties, equations (4) and (5) can be summarized as equation (6), which means that currents I_X and I_Y are equal.

$$V_X = I_X \times R \quad (4)$$

$$V_Y = I_Y \times R \quad (5)$$

$$I_X = I_1 + I_4 \;=\; I_Y = I_2 + I_3 \quad (6)$$

As shown in Fig. 2, in the FVMI mode with switches FV and MI, the change of the input voltage Vin is directly reflected in VPN of the A7 that is shown in Fig. 3. If the input voltage Vin is sufficiently low, no current flows in M2 in Fig. 3. Then, I_2 becomes zero, and the current 2I of the non-inverting differential input pair flows to I_1. Therefore, I_X and I_Y are expressed by equations (7) and (8), respectively. Solving these equations together with equation (6), the equation (9) that is the current relationship of the inverting differential input pair can be obtained. Equations (10) also can be obtained by solving the equations (9) and (1) together.

$$I_X = 2I + I_4 \quad (7)$$

$$I_Y = I_3 \quad (8)$$

$$I_3 - I_4 = 2I \quad (9)$$

$$I_3 = 2I\,, \quad I_4 = 0 \quad (10)$$

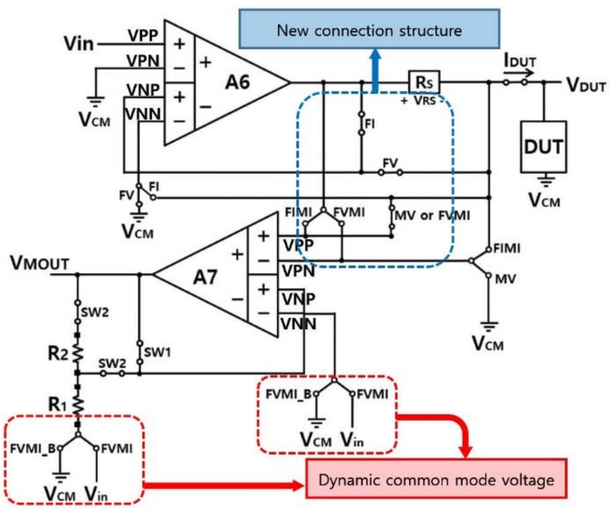


Fig. 4 Block diagram of proposed DC PMU

This means that the voltage of VNP is increased so that the total current 2I of the inverting differential flows to M3 and the output of the IA is distorted. In other words, if the input voltage Vin is high or low enough to turned off the input MOS of VPN of IA using DDA, the IA will output an incorrect result regardless of the forced voltage to VPP, which limits the operating range in FVMI mode.

III. PROPOSED DC PMU

To solve the problems of the prior DC PMU, in this paper, DC PMU using DDA with dynamic common-mode voltage (DCMV) technique and new connection structure is proposed. Fig. 4 shows proposed DC PMU block diagram.

A. Dynamic common-mode voltage

The application of the DCMV is implemented by applying the input voltage Vin to the VNN as shown in Fig. 4 instead of V_{CM} to the VNN as shown in Fig. 2. Appling of the DCMV makes the VPN and VNN equal, as well as making I2 and I4 in Fig. 3 with the same value. Because of this feature, equation (6) is again resulted in equation (11), which means that VPP and VNP have the same value by a virtual short. In other words, since the DCMV technique keeps the VPN and VNN equal, the operating range of FVMI mode is not limited as described in Section II. However, when the VPP of A7 is connected to the output of the A6 and the VPN of A7 is connected to the DUT as in the conventional structure of Fig. 2, the output of the IA (A7) with DCMV can be expressed as equation (12) where A_{IA} means the gain of IA(A7). This means that, because of the term A_{IA} ·VRS, the output of the IA (A7) becomes saturated before the input voltage Vin reaches the supply voltage VDD.

$$I_1 = I_3 \tag{11}$$

$$V_{MOUT} = V_{in} + A_{IA} VRS \tag{12}$$

B. New connection structure

To prevent the output saturation of the IA with DCMV, as shown in Fig. 4, the new connection structure which is the opposite of the conventional structure is proposed. By connecting the VPN of A7 to the output of the A6 and connecting the VPP of A7 to the DUT, the output of the IA (A7) can be expressed as equation (13), which means that the output of the IA is no longer saturated since it is always smaller than the input voltage Vin even if the input voltage becomes VDD. In other words, the FVMI mode with DCMV and with new connection structure shows the wide operating range. The measured current equation of proposed FVMI mode is shown in equation (14).

$$V_{MOUT} = V_{in} - A_{IA} V_{RS} \tag{13}$$

$$I_{MOUT} = \frac{1}{A_{IA} R_S} (V_{in} - V_{MOUT}) \tag{14}$$

IV. SIMULATION

To compare the operating range of proposed FVMI mode with that of the prior FVMI mode, simulations of the two modes under the same conditions are performed. The supply voltage and the resistor of DUT are set to 1.8V and 250Ω, respectively. Fig. 5 shows the simulation results of FVMI modes of prior PMU and proposed PMU. Proposed FVMI mode has wide operating range of 0.25~1.55V, while prior FVMI mode has the limited operating range of 0.7~1.1V.

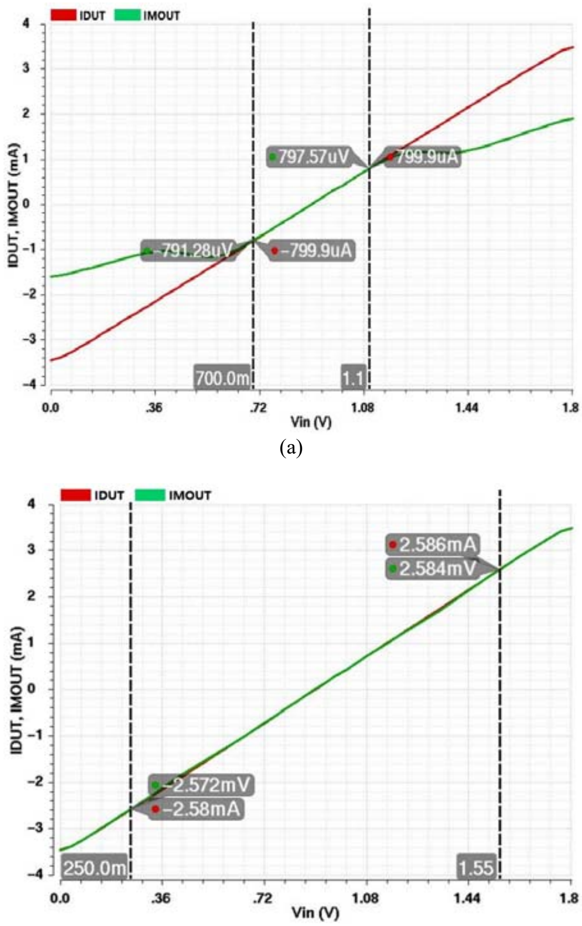


Fig. 5. Simulation results (a) prior FVMI mode (b) proposed FVMI mode

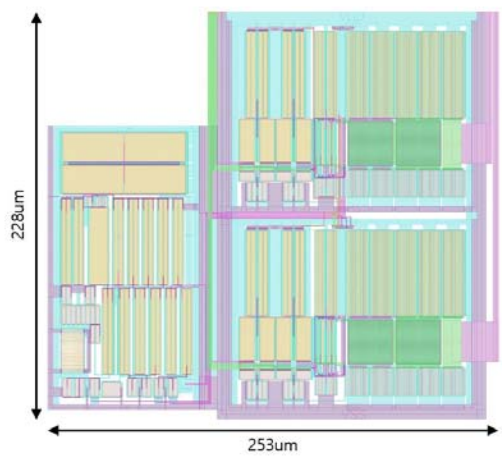


Fig. 6 Layout of proposed DC PMU

TABLE I
Performance Summary of Proposed PMU

Supply voltage	1.8 [V]			
Process	0.18um CMOS			
Common mode voltage	0.9 [V] or Input Voltage			
	force current		force voltage	
Rs	current range	max. error	voltage range	max. error
25Ω	-20~20[mA]	1.43[%]	0.25~1.55[V]	1.28[%]
250Ω	-2~2[mA]		0.25~1.55[V]	
2.5kΩ	-200~200[uA]		0.25~1.55[V]	
25kΩ	-20~20[uA]		0.25~1.55[V]	

V. IMPLEMENTATION AND MEASUREMENTS

The proposed PMU was fabricated in a 0.18um standard CMOS technology. Fig. 6 shows the chip layout, where the proposed DC PMU occupies an area of 228um x 253um. And Fig. 7 shows the test board with implemented chip. In this measurement, we have four modes of the proposed DC PMU such as FVMV, FVMI, FIMV and FIMI. The experiment results include the offset and mismatch error. However, since the proposed DC PMU uses only one DDA for forcing signal or measuring signal, the output error caused by offset and mismatch is the first-order. Therefore, it is easily possible to compensate the output error at the system level. In this paper, the simple calibration is performed using MATLAB. Fig. 8 (a) shows the VDUT and VMOUT versus Vin when force voltage-measure voltage mode. The VMOUT is the measured VDUT by the unity gain buffer consists of A7. The operating range of FVMV mode is from 0.25V to 1.55V excluding nonlinear region, and the maximum measurement error is 1.28%. Fig. 8 (b) shows the IDUT and IMDUT versus Vin when force voltage-measure current mode. The IMDUT is the measured IDUT by the instrument amplifier consists of A7. The operating range of FVMI mode is from 0.25V to 1.55V excluding nonlinear region, and the maximum measurement error is 0.8%. Fig. 8 (c) shows the VDUT and VMDUT versus Iin when force current-measure voltage mode. The operating range of FIMV mode is from -20mA to 20mA at the RS of 25Ω excluding nonlinear region, and the maximum measurement error is 0.1%. Fig. 8 (d) shows the IDUT and IMDUT versus Iin when force current-measure current mode. The operating range of FIMI mode is from -20mA to 20mA at the RS of 25Ω excluding nonlinear region, and the maximum measurement error is 1.43%.

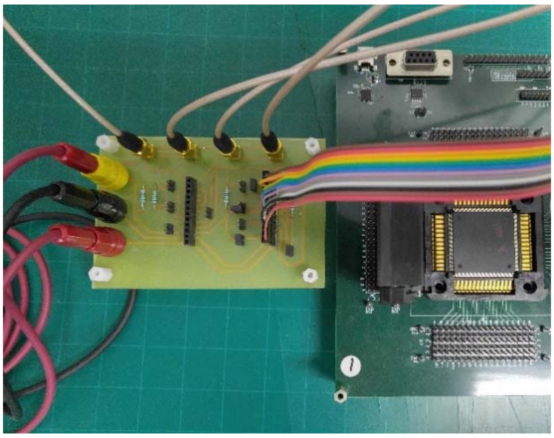
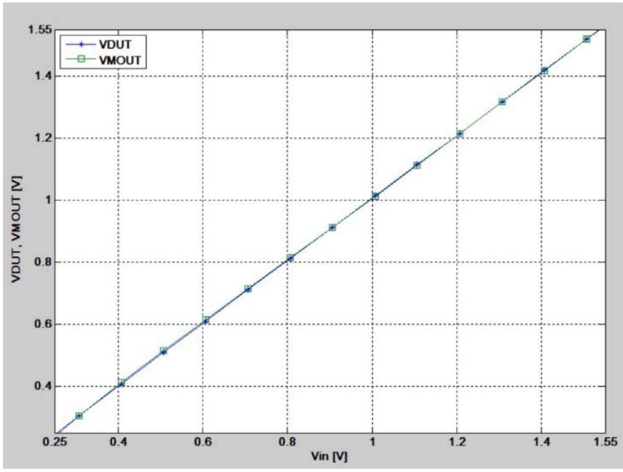
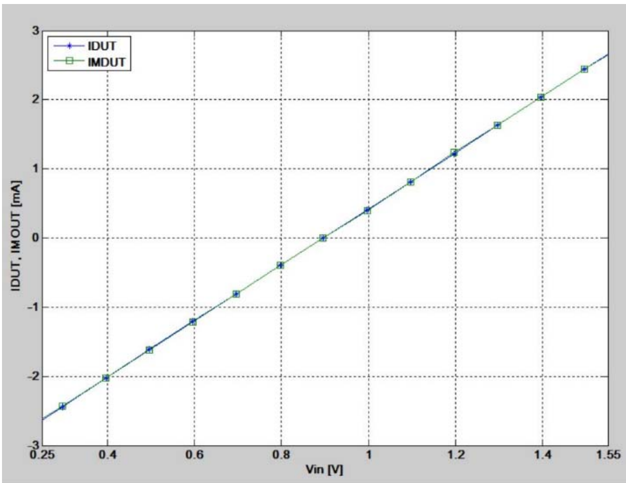


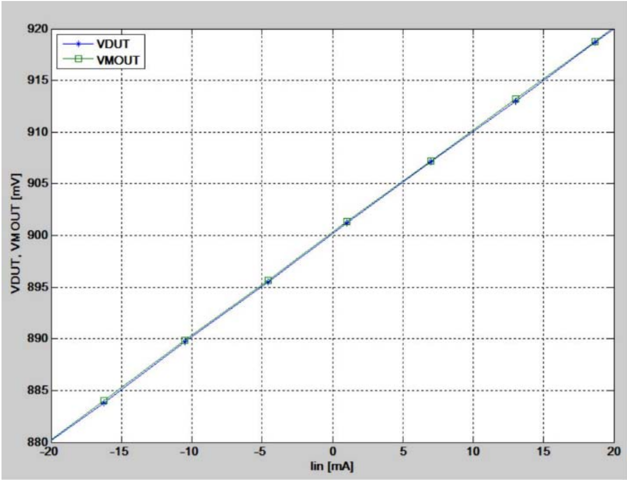
Fig. 7 Test Setup



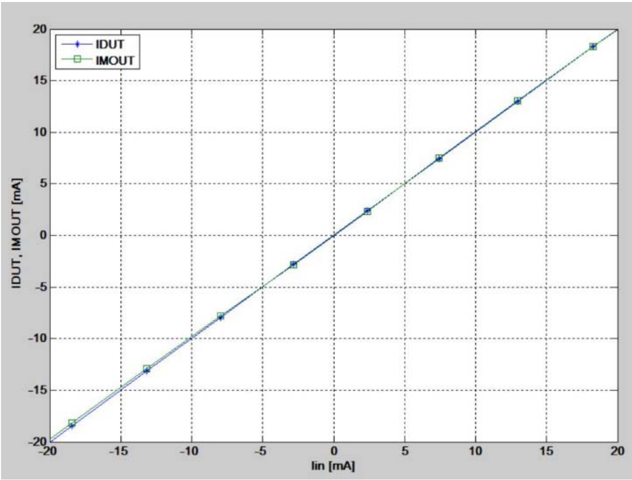
(a)



(b)



(c)



(d)

Fig. 8 (a) FVMV mode (b) FVMI mode (c) FIMV mode (d) FIMI mode

VI. CONCLUSIONS

In this paper, the DC PMU using DDA with full range operation is proposed. The proposed techniques for the new DC PMU are dynamic common-mode voltage technique and new connection structure. As these techniques are adopted, the instrument amplifier using differential difference amplifier overcome the structural limitation, as well as the output saturation of the instrument amplifier. These proposed techniques do not require additional circuits and power consumption. In the experiment results, the operating ranges are 0.25V~1.55V and -20mA~20mA for forcing voltage mode and forcing current mode, respectively. And, the maximum errors are 1.28%, 0.8%, 0.1% and 1.43% for FVMV, FVMI, FIMV and FIMI, respectively.

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