HV Power Converter topology Wireless Power Receiving in Portable Electric devices

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***Abstract* - This article presents a PWM current mode DC-DC buck converter for wireless power receiver in MCR (Magnetic Coupling Resonance) WPT System. Simulations are based on 0.18µm BCD process in Towerjazz technology, 1-poly 3metal. The current mode controlled based DC-DC buck converter operates with 2MHz operating frequency. Power switch was designed with LDMOS of BCD process in order to withstand the high voltage and the high current. We also design a control block composed of the current sensor, comparator, OTA, PWM signal generator and gate driver. The proposed buck converter has an input voltage range 6-10V with maximum output current of 1A while providing 5V output.**

I. INTRODUCTION

Recently, there has been an increasing interest in wireless power transfer due to the development of mobile devices, smart application devices, biomedical devices and electronic vehicles. The wireless power transmission (WPT) technologies can be divided into two methods, inductive coupling and magnetic resonance coupling.

WPT which is based on inductive coupling demonstrates high efficiency, however, they are limited to several tens of mm in power transfer range [2]. Meanwhile, the magnetic resonance coupling method using magnetic evanescent wave coupling was a potential breakthrough, for mid-range energy transfer [1], [3], [4].

Fig. 1 is a general block diagram of magnetic resonance WPT scheme. The integrated power receiver contains a rectifier, DC-DC converter, LDO regulator and battery charge control circuit for mobile applications. The important feature of WPT is high efficiency at large transmission distance. The variation in the impedance of the power receiving circuit, changes the efficiency of power transmission system randomly. The impedance transformations are mainly due to voltage changes and the change in distance between the transmitter and receiver. Therefore, DC-DC converter is able to improve efficiency by regulating load voltage. In paper [5], experiment shows that efficiency of power transmission is increased by DC-DC converter. In addition, in WPT system, the process of converting the voltage which is transferred to a particular application is very important.

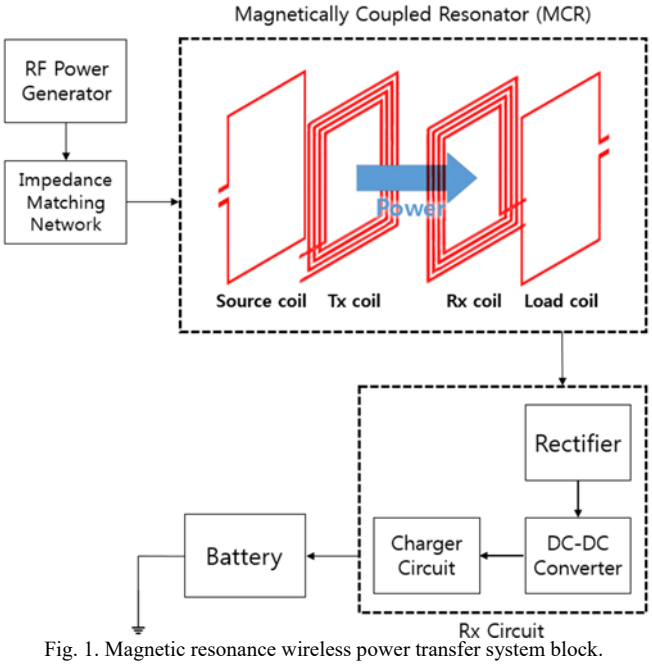

Fig. 1. Magnetic resonance wireless power transfer system block.

In Wireless powered systems, power management circuits play important role to increase the reliability and durability of the system. For wireless charging in portable electronic devices, it is highly recommended to design PMICs (power management ICs) to ensure the safe and reliable battery charging process. This increases the lifetime of the battery and decreases the cost of replacement of the battery ensuring a reliable design of the product. So we propose a design of a novel, ultra-compact, and highly efficient lithium-ion (Li-ion) battery charging circuit that addresses the unique challenges of battery management for small rechargeable cells (800-3500mAh). The entire circuit operates in the analog domain and is particularly well suited for operation in portable electronic devices, where energy and space are at a premium. Ultra-low power-electronic systems utilizing small rechargeable cells present a unique challenge for digitally controlled charger circuitry. In these circuit architectures, the energy overhead consumed by controller logic is fixed, while charging current varies with battery capacity. Thus, at low charging currents, a significant

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fraction of total power may be consumed by the control circuitry. These designs may utilize large-area analog-to-digital converters (ADCs) or costly precision-trimmed sense resistors in the voltage comparator for accurate end-of-charge detection.

The circuit presented here addresses both of these issues. As an alternative to digital control logic, we utilize the tanh basis function of an operational transconductance amplifier (OTA) operating in the subthreshold region to output a current profile that smoothly and automatically transitions between constant-current (CC) and constant-voltage (CV) charging regions. As a result, this circuit is an order of magnitude smaller than previous designs, while achieving higher average power efficiency.

The charging control circuit design is based on saturation region operated OTA control, which helps to attain high power efficiency during the time of recharging process. The proposed design unlike the other design is less complex and less vulnerable to temperature artifacts due to the compensation scheme designed for temperature variations based on the control of gate to source voltage dependency to temperature. The charging profile of typical lithium ion battery is followed during the process of recharging.

The DC-DC converter for the design unlike prior designs provides better stability at high operating frequency conditions. The control scheme is based on pulse width modulation topology involving peak current mode technique that helps to provide faster transient response than the other on-chip voltage mode control converters.

II. PWM CURRENT MODE DC-DC BUCK CONVERTER

A. DC-DC converter with inductor

DC-DC converter with inductor step-up or step-down the input voltage based on application [6], [7], [8], [9]. In general, method for designing current mode controller of DC-DC converter with inductor can be divided into two. The first method is pulse frequency modulation (PFM). PFM controller has simple structure since it is constituted of a comparator and shows high efficiency at low load currents. However, it is very difficult to filter the switching noise due to variation in switching frequency characteristic. The second method is pulse width modulation (PWM) that has constant switching frequency. This method is used in sensitive systems to reduce noise. Therefore, in general, a system that uses a large load current is using PWM control method [10].

B. Current mode DC-DC buck converter

A Model is linearized in order to analyze the stability of the feedback loop. General voltage mode DC-DC buck converter is difficult to secure the gain and phase margin because this converter has two poles [11], [12].

The voltage mode DC-DC buck converter uses proportional integral derivative (PID) compensator which can compensates the gain and phase margin at the same time [12]. The current mode DC-DC buck converter has two poles such as the voltage mode DC-DC buck converter [13]. However, Second pole frequency of current mode DC-DC converter is far away from the first pole frequency. Thus second pole does not affect the stability of the entire converter [13], [14], then it has appropriate phase margin without phase lead network. Therefore, current mode DC-DC converter compensates only gain using proportional integration (PI) compensator.

The oscillation due to Disturbance is a drawback of the current mode that is well known. The current mode DC-DC converter control signal with a inductor current is sensitive to disturbance [13]. To prevent this oscillation due to disturbance, adding artificial ramp to the current sensing signal is essential

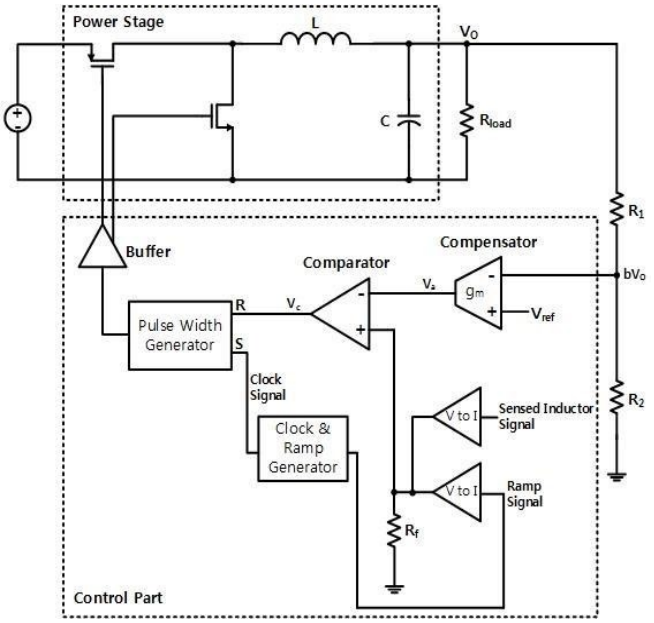

Fig. 2. PWM Current Mode DC-DC Buck Converter block diagram.

Fig. 2 represents a simplified block diagram of current mode DC-DC buck converter. The main function of the converter is to convert the voltage to a lower output voltage than the input voltage. This converter consists of power supply part and feedback control part. V_{DD} is the input voltage and V_{out} is the output voltage. R_1 and R_2 detect the output voltage and determine the value of output voltage of the operational transconductance amplifier (OTA). In Fig. 2, the clock generates a short pulse wave having the determined pre-cycle, the output of the SR latch is determined by this pulse. A reset timing of the latch is controlled by a comparison of $i_c(S)R_f$ through the OTA output and $i_s(S)R_f$ through the inductor sensing current circuit. Flowing current in Q_1 is equal to inductor current. This means that the signal of the current sensing circuit $i_s(S)R_f$ is same as inductor current. When Q_1 is set on, output voltage increases. If V_{ref} is not equal to the output voltage that is measured via (R_1, R_2), the control signal is changed by the OTA, so that it becomes to adjust the output voltage due to a reset timing of the latch is changed. In other words, the operation of the transistors (Q_1, Q_2) is controlled by the PWM signals generated by the latch and it brings to generate the desired output voltage through transistor On/Off operation [11], [12].

C. OTA and compensator circuit

For the design of compensator initially, the unit-gain frequency has to be defined. If unit-gain frequency has decided, it is possible to determine the gain and amount of phase compensation. In general, unity-gain frequency is less than 1/10 of the converter switching frequency. If more than 1/10 of the converter switching frequency, a gain of compensator is to be too large, then switching noise amplified by the compensation will affect the internal converter [13],[14]. After determining the unit-gain frequency, we decide pole and zero frequency and gain of unit-gain frequency. In this case, median of zero and pole frequency will be determined to match the unit-gain frequency to prevent the decrease in phase margin.

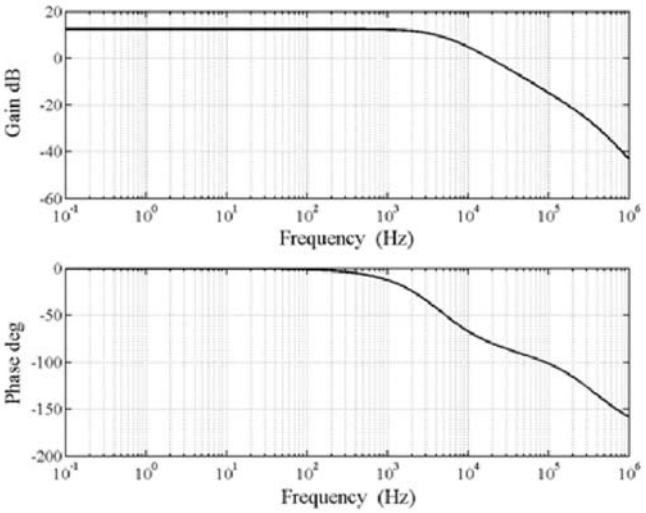

Fig. 3. Frequency characteristics of buck converter without compensation.

Fig. 3 represent the frequency characteristics of uncompensated current mode DC-DC converter. It can be approximated to the first order model of a single pole. The current mode DC-DC converter without compensation has a sufficient phase margin. But DC gain is very low less than 20dB, so it should be compensated by the proportional integration (PI) compensator.

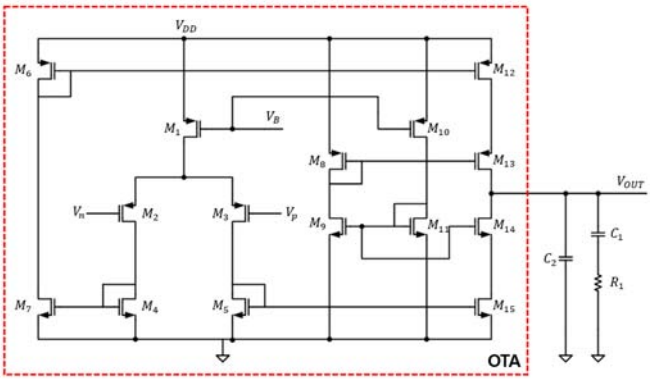

Fig. 4. OTA circuit and PI compensator using OTA.

Fig. 4 shows OTA circuit diagram and proposed PI compensator. In proposed PI compensator, pole and zero frequency are given by equation (1) and (2).

$$f_z = \frac{1}{2\pi R_1 C_1} \quad (1)$$

$$f_p = \frac{C_1+C_2}{2\pi R_1 C_1 C_2} \approx \frac{1}{2\pi R_1 C_2} \quad where\ C_2 \ll C_2 \quad (2)$$

The gain of compensator in unit gain frequency is given by equation (3)

$$A_v = g_m R_1 \quad (3)$$

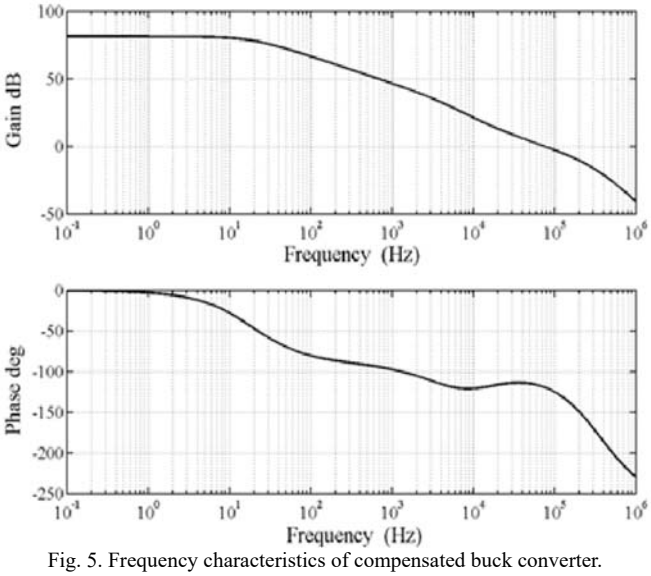

Fig. 5. Frequency characteristics of compensated buck converter.

Fig. 5 represents frequency characteristics of compensated current mode DC-DC buck converter. The gain and phase characteristics were compensated sufficient DC gain and phase margin through the PI compensators.

D. Inductor Current Sensing

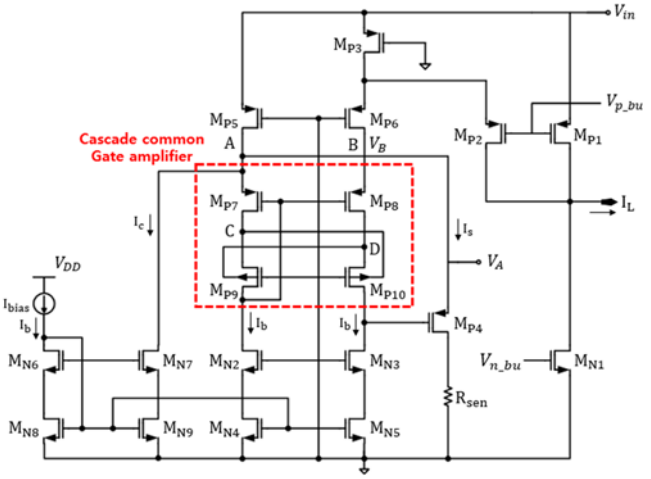

Fig. 6. Current sensing circuit.

Fig. 6 shows the proposed current sensing circuit. A pair of cascade common gate amplifiers achieve high loop gain. The bulks of M_{P9} and M_{P10} are connected to node C and D. Thus it can provide two additional inputs for the cascade common gate amplifier to improve loop gain and transient response. The cascade current mirror composed of M_{N2}-M_{N5} increases the output impedance of the common gate amplifier and reduces the channel length modulation effect. A small input offset voltage between node A and B

according to the negative feedback loop of M_{P4} causes the sensing current IS to decrease. As a result, V_B is increased due to increase in gate voltage of M_{P4} in at saturation region. Therefore, high loop gain and small offset voltage provides high sensing accuracy since the negative feedback forces V_B to change in the same direction as V_A.

E. Clock and ramp signal generator

The schematic of clock and ramp signal generator is shown in the fig. 7. This circuit generates the clock and ramp signal for PWM signal control and stability of the current sensing. The schematic circuit of comparator is shown in Fig. 8. When the capacitor C1 is charged by the current source, the voltage of ramp node increases according to the following equation (4).

$$\text{Ramp} = \frac{I_{REF}}{C_1} \cdot t \tag{4}$$

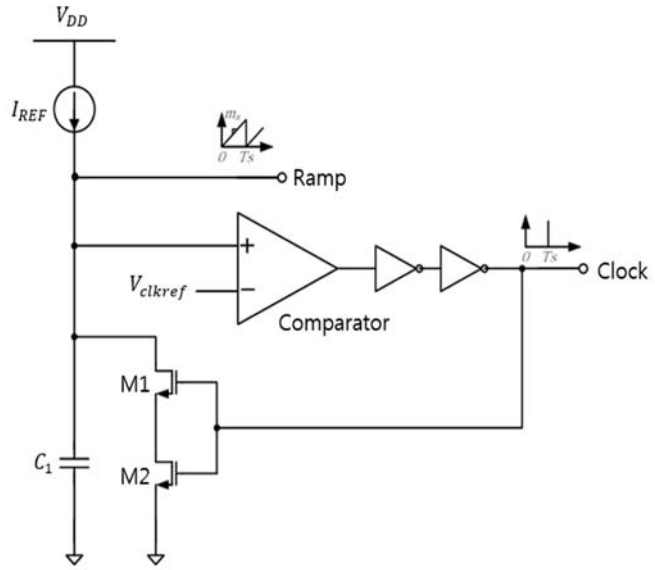

Fig. 7. Clock and Ramp signal generator.

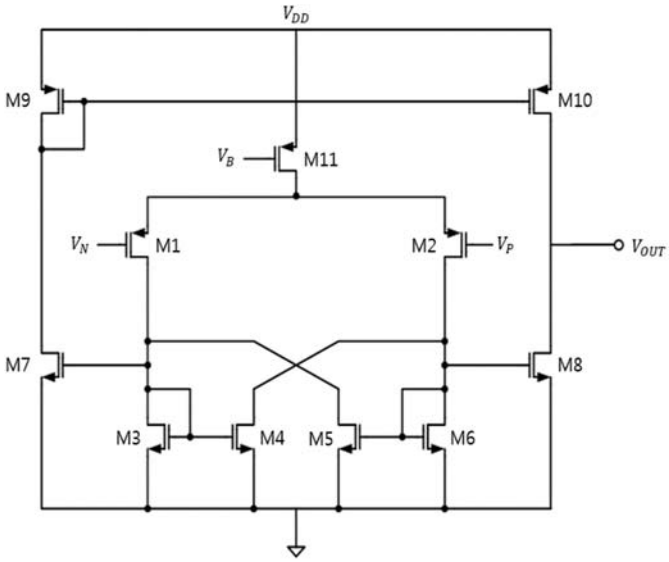

Fig. 8. Hysteresis comparator.

When the ramp voltage increase until VCLKREF, M1 and M2 is turn on, then C1 is discharged. As a result, lamp node voltage is to be reduced. When C1 is discharged, so much current flows in to the capacitor momently. It is able to lead to destruction of the transistor. Therefore, M1 and M2 transistor was placed in series to prevent destruction of transistor. While repeating the above process, signal generator produces the desired signal.

F. Charging control circuit

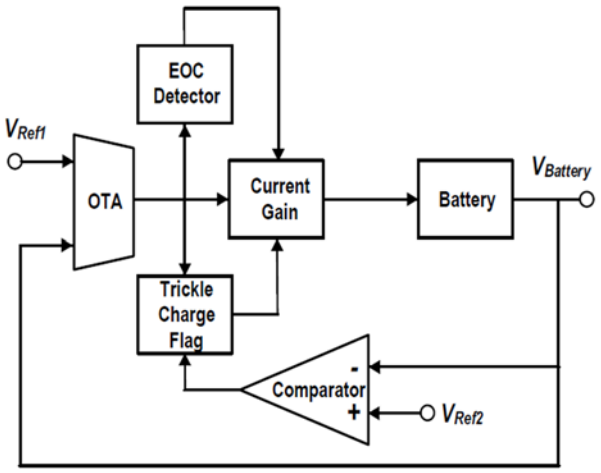

Fig. 9. Charging circuit block diagram.

Fig. 9 shows block diagram of charging circuit. For safe charging, we have developed a control circuit that is in trickle charging, constant current (CC), constant voltage (CV) and end of charging (EOC) during charging.

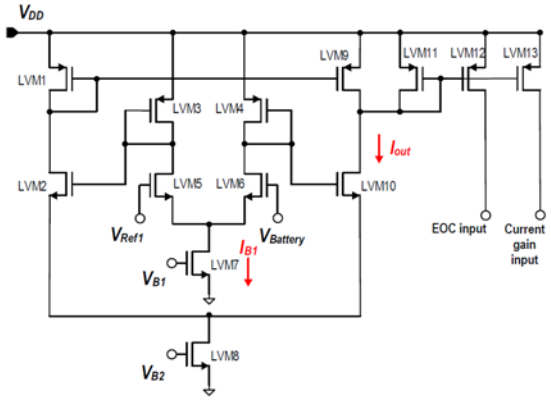

Fig. 10. OTA.

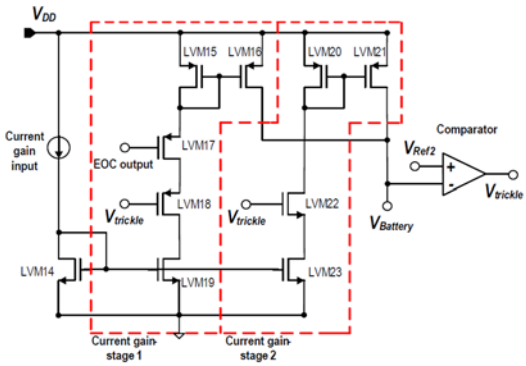

Fig. 11. Current gain stage and trickle charge detector.

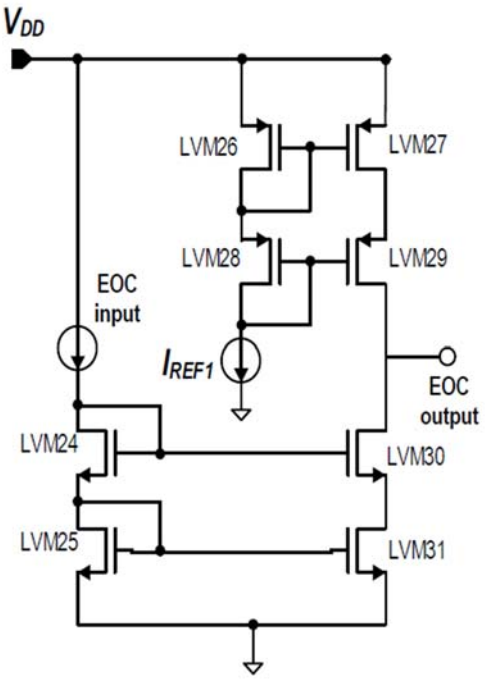

Fig. 12. EOC detector.

III. RESULTS AND DISCUSSION

The packaged chip is further tested and verified using special socket designed for the purpose. Discrete components with minimum tolerance are used in additional for the test and verification. The initial procedure of the testing involves the test and verification of individual circuits on the chip for the desired performance. The entire system verification is done after individual circuit test and verification. In general the following procedures are followed for the test and verification process. First, A four coil helical antennae structure for wireless power transmission using resonance magnetic coupling. Second, The testing socket with the chip for testing the circuits. Third, Oscilloscope for capturing and verifying the test result. Fourth, A RF signal/function generator for testing analyzing the individual circuits for various frequencies. Fifth, A Dual supply DC power source for individual test and verification of the circuit. Sixth, A lithium-ion battery for the purpose of recharging.

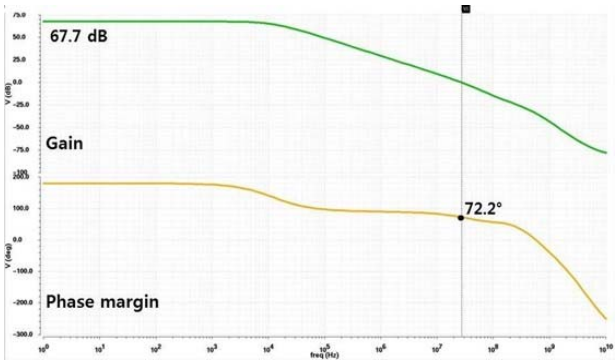

Fig. 13. OTA bode plot.

Fig. 13 shows the AC analysis of OTA used in current mode DC-DC converter. The OTA results compared the output voltage and the reference voltage. OTA gain and phase margin is measured 67.7dB and 72.2° respectively.

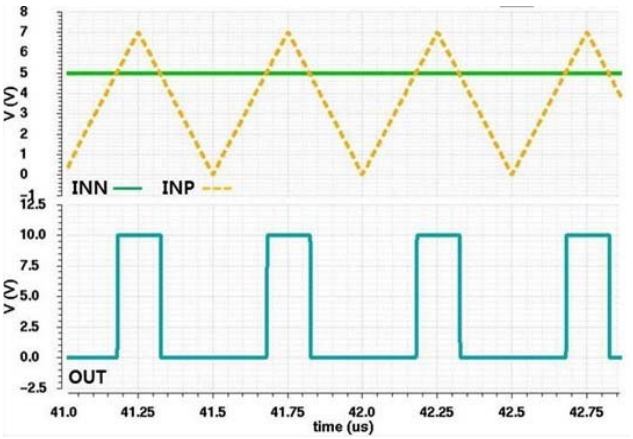

Fig. 14. Wave form of comparator.

Fig. 14 represents a waveform of comparator. The comparator is used to generate a reset signal through the RS latch of the PWM generator by comparing the output voltage and detected signal in the inductor. Besides, it controls the charged voltage in capacitor from ramp signal generator. The output pulse is generated by comparison of both the input voltages. When INP is larger than the INN, the output pulse is high. Therefore, it plays the role of switching.

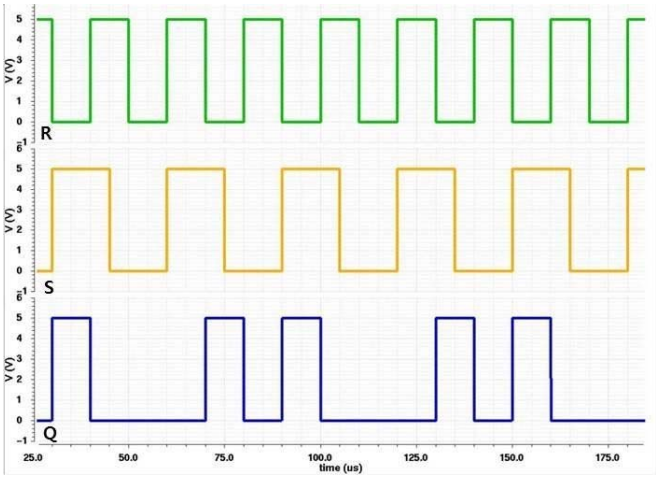

Fig. 15. The simulation waveform of RS-latch.

TABLE 1.
RS latch truth table.

Input		Output	
S	R	Q	$\bar{Q}$
0	0	Hold	
0	1	0	1
1	0	1	0
1	1	0	0

Fig. 15 represents a simulation result of RS-latch for generating PWM signal. TABLE 2 shows truth table of RS latch. We confirmed the operation in accordance with the truth table.

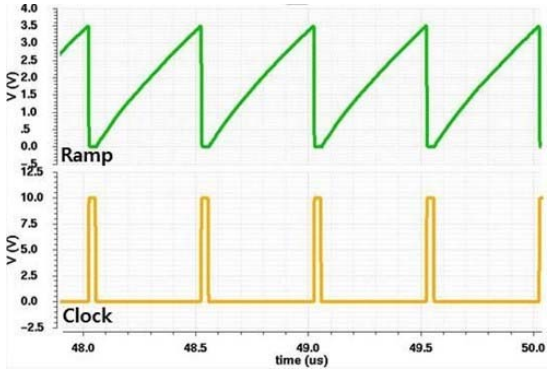

Fig. 16. The output voltage of clock and ramp signal generator.

Fig. 16 shows the clock signal in order to generate ramp and PWM signal. The ramp voltage increases according to the current flowing through capacitor and capacitance. When the ramp signal becomes higher than reference voltage, the clock pulse changes to high and the lamp voltage is decreased rapidly. The clock frequency which is generated by above process equals to the switching frequency in DC-DC converter.

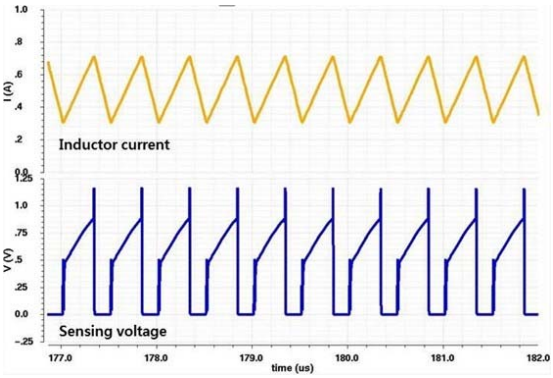

Fig. 17. Inductor current and current sensing voltage.

Fig. 17 shows the wave form of inductor current and current sensing voltage. The slope of sensing voltage waveform which is related input voltage is adjusted the pulse width.

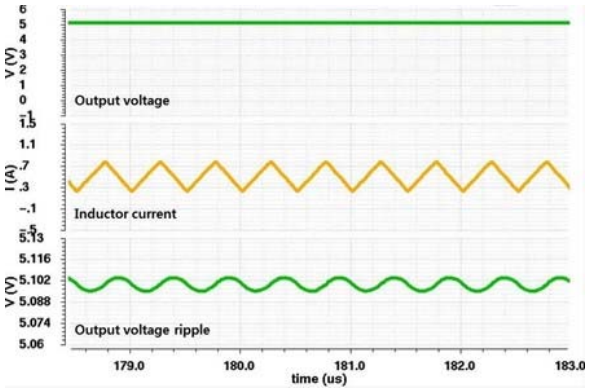

Fig. 18. Fabricated entire current mode DC-DC buck converter wave form.

Fig. 18 shows the output voltage, inductor current and output ripple voltage wave form of fabricated entire current mode DC-DC buck converter. The converter measured 5V output voltage, 10mV ripple voltage and 1A output current at 6-10V input voltage.

TABLE 2.
Performance comparison with prior DC-DC converter.

Publication	[15]	[16]	[17]	[18]	This work
Process	0.35μm CMOS	0.5μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm BCD
Input voltage (V)	3.3	5.5	2.7 ~3.6	2.7 ~4.2	6 ~10
Output voltage (V)	1.65	3.3	2	1	5
Output ripple voltage (mV)	< 10	16	N/A	N/A	10
Switching frequency (MHz)	1	4	1	3	2
Maximum output current (A)	0.5	0.6	0.5	0.5	1

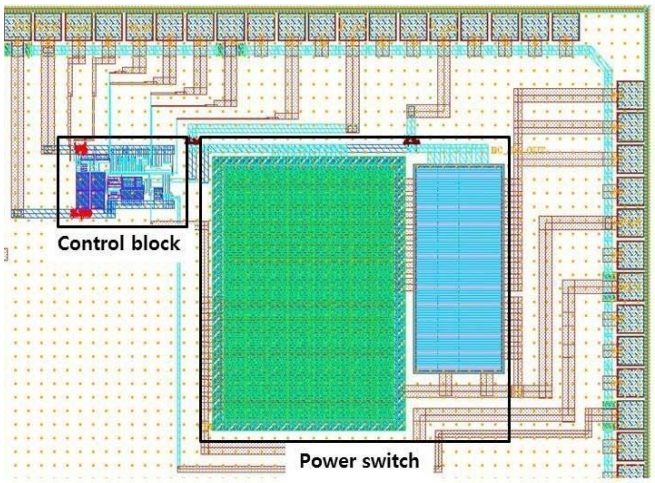

Fig. 19. Layout of current mode DC-DC buck converter chip.

Fig. 19 shows the layout of proposed DC-DC buck converter. It is implemented using 0.18μm BCD process in order to operate high voltage. The power switch is designed LDMOS and separated from control part by guarding process using Pwell.

IV. CONCLUSIONS

In this paper, we proposed current mode DC-DC buck converter for magnetic resonance wireless power transfer. It was implemented by using TowerJazz 0.18μm BCD process, 1-poly 3metal. The current mode controlled based DC-DC buck converter operates with 2MHz operating frequency. Power switch was designed with LDMOS of BCD process in order to withstand the high voltage and the high current. We also design a control block composed of the current sensor, comparator, OTA, PWM signal generator and gate driver. The proposed buck converter has an input voltage range 6-10V with maximum output current of 1A while providing 5V output.

The design of the proposed circuit was typically for wireless battery recharging in portable devices such as in mobile phones, laptops, tablets, Bluetooth headsets etc. The design also qualifies for the application in biomedical implants owing to the miniature size of the chip and high power efficiency. Applications such as in solar sensors and piezoelectric sensors are for low power modules.

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