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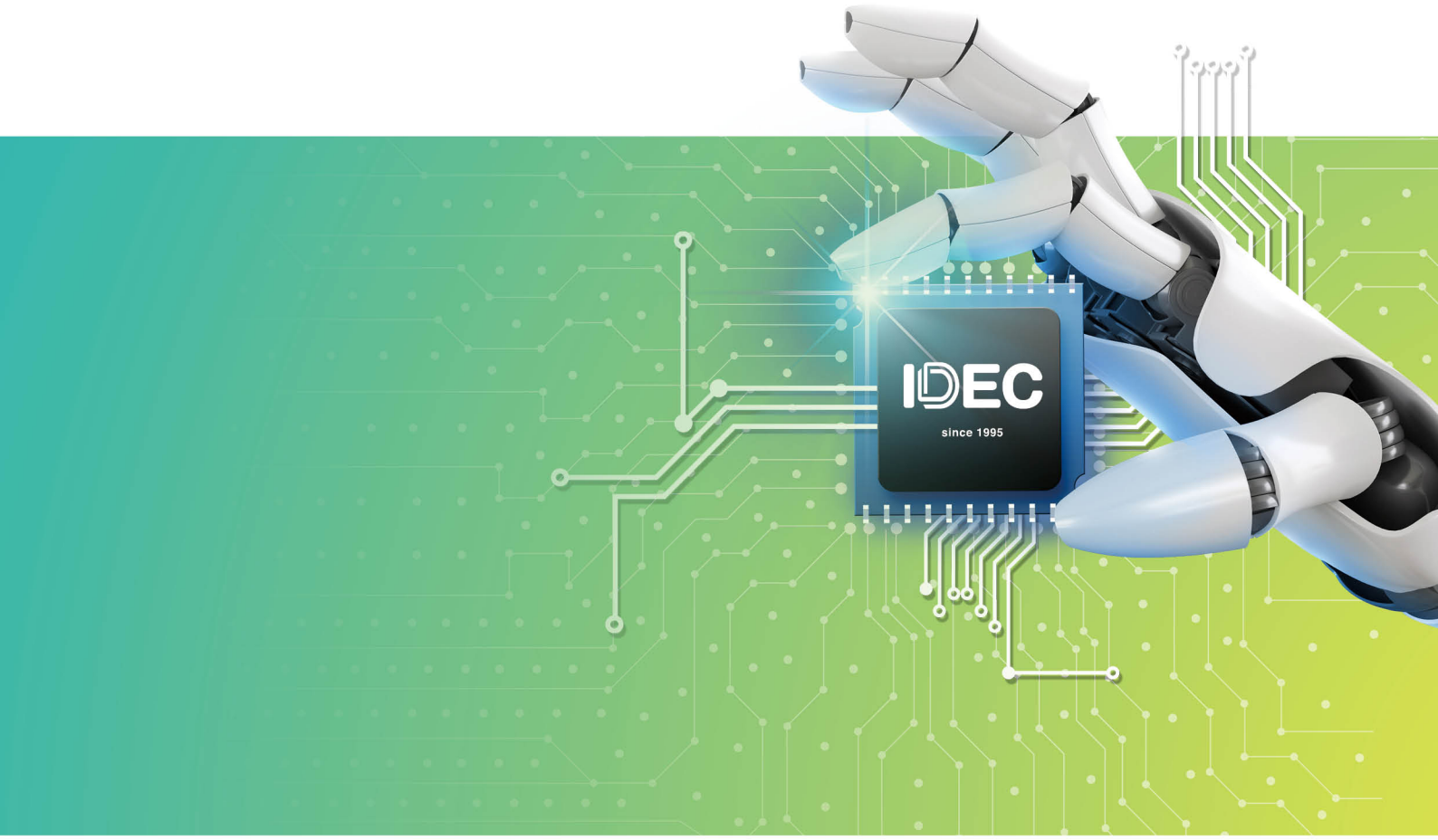

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Addressable Microstimulator Circuit for Neural Prosthesis

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***Abstract* - Current state-of-the-art Brain-Machine Interfaces (BMIs) with multi-channel neural interfacing microsystem has been developed as the scale of CMOS process continuously miniatured. Further performance enhancement in BMIs relies on the ability to develop implantable integrated circuit system that would reduce the noise level and the power consumption to operate scalable thousands of channels. In this work, we describe a prototype of distributed wireless microimplants, which provide a high-density network of addressable neural stimulator system with an optical powering method. The proposed circuit built in a standard 0.18μm CMOS process, which include the rectifier, the binary phase-shift keying (BPSK) demodulator, the clock recovery, 9-bits metal fuses and the digital block to discriminate address for each chip. The circuit occupies 211×204 μm^2 of silicon area totally, which would be a reasonable size for micro implant. A photovoltaic cell is used to provide efficient power as BPSK modulated signal with the supply voltage 3 V. The designed circuit consumes ~77μW at a data rate of 20 Mbps at 20 MHz carrier frequency.**

***Keywords*—Brain-machine interface, implantable sensor, wireless microstimulator**

I. INTRODUCTION

Brain-machine interfaces (BMIs) is a technology that provides bidirectional communication between the external machine and the nervous system. With the neural information pathway through BMIs, it can provide solutions for neurological disabilities, which can be possible to monitor the neural activity and stimulate nervous system with input the specific signal to mitigate functional impairment through the use of multichannel electrode devices, either microelectrode arrays (MEAs) or Electrocorticography (ECoG). For the significant advantages, developing micro-implant systems in BMI are crucial for not only the neuroscience research but also the neural prosthetic systems enabling the treatment of neurological disease, the restoration of sensory and motor disabilities.

Among the several different approaches to neural implant system, wired microsensor system has been developed since its successful human clinical trials. It has facilitated the acquisition of neural data with high temporal and spatial resolution. However, the wired neural system requires cables that connect between the external device and brain for powering and data transmission penetrating skin and skull, which cause can cause neurological damage and the increasing risks of infection. As a result, the next-generation BMIs critically need to provide wireless powering and telemetry system across a range of brain tissue. Furthermore, individual implant volume is required to minimize less than sub-mm that can be inserted to the brain with minimum damage to tissue and located without any interruption biological function of the brain. Recently, small distributed sensors that remotely power controlled have been proposed as a way to measure the neural activity with a high spatial and temporal sampling (Fig. 1).

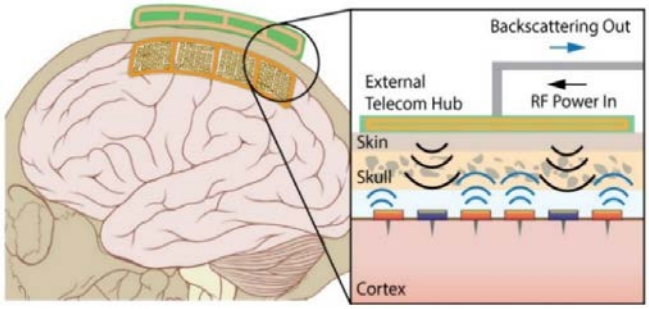

Fig. 1. The concept of a wireless neural implant('Neurograin') network.

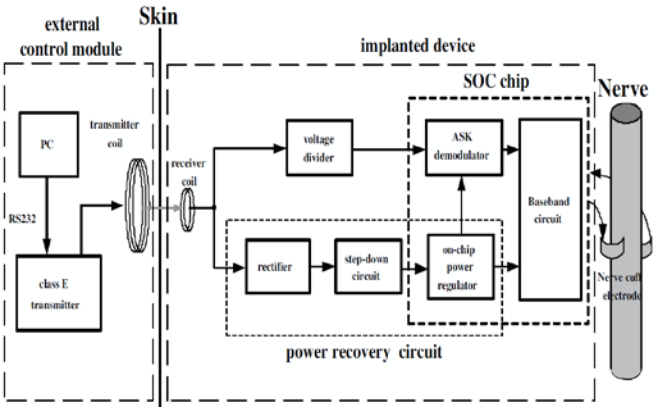

Fig. 2. Functional block diagram of wireless neural stimulating system [5]

Ultralow power consumption in biomedical implants is pursued so that some researches would be used for pre-clinical and clinical applications with RF wireless power transfer system [1, 2, 3, 4]. In present, the promising energy transfer method is inductive coupling using two pairs of coils depicted in Fig. 2 [5]. The external system consists of amplifier and transmitter coil. ASK modulation protocol is utilized to transfer power and data signal to the internal chip.

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An on-chip low dropout (LDO) voltage regulator circuit works as power recovery from the induced RF signal, which drives a stable supply voltage 3.3V. However, the ASK modulation has the major drawback of relatively the low data transmission rate and the decreasing in amount of transferred power to implants. In this paper, we suggest low power, sub-millimeter, and individually addressable neural stimulation system. With the Manchester encoding technique, the system has downlink data communication with a high data rate and efficient power delivery.

II. FUNCTIONAL BLOCK OF SYSTEM

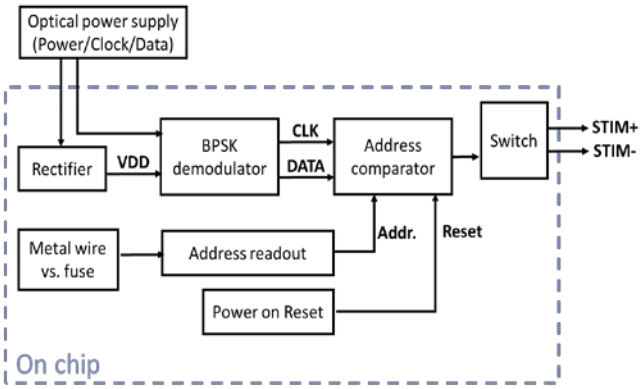

Fig. 3. Functional block diagram of neural implant system

A. Optical Power supply

For the optical power source, we have designed the photovoltaic cell that is based on a tandem structure pn-junction gallium-arsenide/aluminum-gallium-arsenide (GaAs/AlGaAs) hetero-structures [6, 7]. This optical power supply provides not only the power to operate the whole system on the chip but also the data and clock including specific sequence such as the 4-bits header, 9-bits address, and timing command. The photovoltaic cell is bonded with pads on chip, which can provide 3V input power for the internal circuit.

B. Clock recovery

The proposed clock recovery circuit extracts the clock signal from BPSK modulated input signal using a XOR gate. It is not necessary to have the implanted any modules to generate the clock within the chip, e.g., an on-board crystal oscillator, which can reduce the enormous total power consumption and chip area in layout. In addition, the clock signals are synchronized with the input BPSK modulated signal all the timing. The output of two-input XOR gate is fed to the digital block.

C. BPSK demodulator

BPSK demodulator is proposed without using any passive component in this work. Traditional BPSK demodulators in biological implanted devices need a large capacitor, which occupies a huge area on the chip. We use the diode-connected transistor in standard CMOS process that acts as a source-drain-shorted capacitor instead of a direct capacitor component. Based on the BPSK demodulator, it is an efficient way to be in synch with generated internal signals on chip such as clock, demodulated data, and the initial input signal.

D. Address Comparator

To make a form of distributed wireless sensor network, each chip is designed to have a unique ID, which is a 9-bits fuse using the top metal layer (aluminum) available in the CMOS process. A pad opening layer is used to eliminate any passivation layers on fuse area. The fuses exposed the top metal facilitate laser ablation process with the use of the green light laser (532 nm) for cutting the metal trace to set a bit. The address comparator compares the read-out address bits written by fuse on the chip and the incoming command signal through the BPSK demodulator in order to find the device that has matched addresses.

III. RESULTS AND DISCUSSION

A. Benchtop testing and validation

A bench top set up was created to test the performance of the stimulation source on the chip. The chip was wire-bonded to a PCB and a known resistor (50 kOhm) was connected across the terminal to figure out the output current (Fig. 4). For each block characterization, we connected SMA connectors with for each node. Since the chip is operated by 20MHz clock-frequency and its data rate is chosen at 20Mbps, we used a mixed signal oscilloscope with high sampling rate (Tektronix, MSO5204) and a 1 GHz probe (Tektronix, TPP1000) with low capacitance (3.9 pF/10 MOhm) to measure the chip performance accurately.

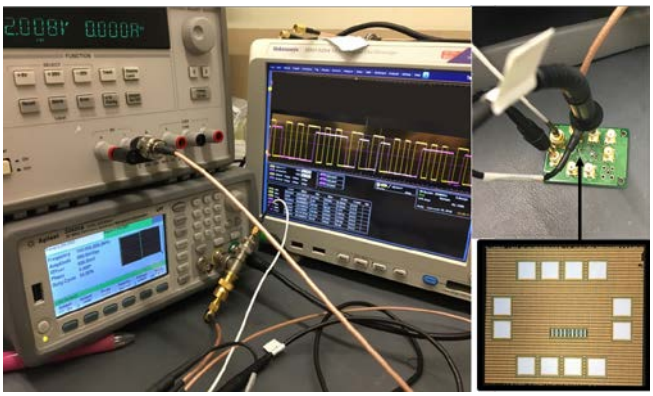

Fig. 4. Benchtop setup; The chip was wire-bonded on the PCB board and connected to a load resistance 50kohm.

B. Analog circuit

Fig.5 shows the block diagram of the analog circuitry in the chip, which is based on the data detection circuit. A pad (a part of the on the chip called 'Vin') is coupled to the external function generator, which simulates wireless implant system that operates by the photovoltaic cell. The input of BPSK modulated signal is fed to the rectifier, which then produces DC voltage to all on-chip circuits. The BPSK demodulator consists of a pulse-width measurement unit,

two identical Schmitt triggers and a NOR-based SR latch. In order to retrieve a clock signal, the demodulated data throughout the SR latch and the input BPSK signal are fed to a two-inputs XOR gate. The received input signal is slightly delayed via the demodulated data by using a buffer that consists of two cascaded CMOS inverters.

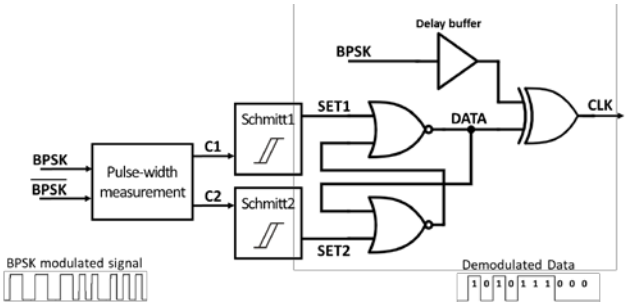

Fig. 5. Functional block diagram of analog circuitry

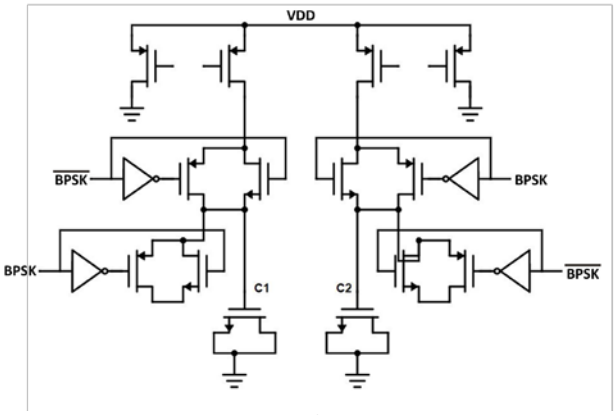

Fig. 6. Circuit schematic of Pulse-width measurement

Since we adapted the BPSK detector instead of the coherent demodulator that generally needs high power consumption COSTAS loop [8, 9], the analog circuit can be reduced the totally layout area of 44×47 μm^2 in Table 1 and the operating power level at ~77μW (Table 2).

As regards the rectifier circuit, maximizing the pulsed BPSK signal-to-dc power conversion efficiency has two challenges: (a) the received BPSK signal from the GaAs photovoltaic cell we have developed is not sinusoid signal but rectangular pulses, since the GaAs photovoltaic cell for the wireless power source is controlled by turning on and off the external light source. (b) As the high efficiency GaAs cell generates 3V output voltage, the rectifier requires a respond of voltage fluctuation from 0 to 3V. Therefore, the rectifier circuit is designed with the envelope detector structure that consists of two capacitors and a single diode. As a result, the rectifier produces 1.959V DC voltage and supplies it to all on-chip circuits.

For pulse-width measurement in the proposed demodulator, two capacitors are first charged with the same current and then the voltages across the capacitors are compared using a comparator. The process of charging and discharging of these capacitors are synchronized with the input BPSK signal. By applying the BPSK signals to be switched to each side of the pulse width measurement unit, the rectangular BPSK pulsed with longer time duration are interpreted as sawtooth waveforms in Fig. 6. In this design, as two capacitors used the diode-connected transistors, the demodulator is made of only transistors. Therefore, it not only provides a fast speed of charging and discharging but also reduces occupying total area on the layout. In the pulse width measurement, the integral form of BPSK signal is generated and then these signals are fed to the inputs of two Schmitt triggers. By choosing appropriate transistor aspect ratios, the upper trigger point of the designed Schmitt trigger is set to be 1.55V. If the signal from PWM circuit is higher than the trigger point, the Schmitt trigger makes signal goes to ′high′ state. Therefore, the output of the Schmitt triggers is a series of rectangular pulses, discriminating between the short and long BPSK carrier cycles. These pulses are fed into a NOR-based SR latch, which is used for a data decoder.

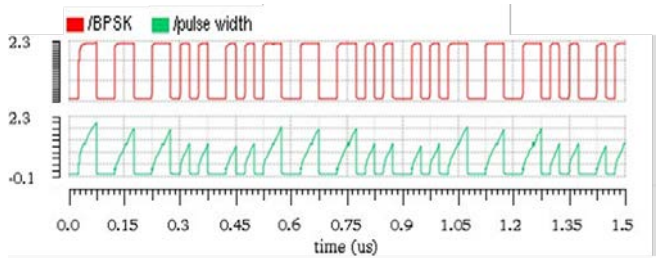

Fig. 6. Post-stimulated the voltage response across the capacitor in the pulse width measurement.

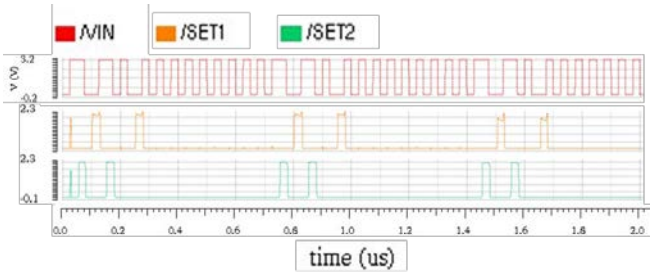

Fig. 7. Post-stimulated the rectangular pulsed voltage response of two Schmitt triggers (SET1, SET2) and BPSK input signal (VIN).

C. Digital circuit

The digital controller is a crucial component of the system related to address selectivity, which includes the serial input interface, the 9-bits address readout and a comparator. Serial data is delivered a 13-bits identification and the end-timing information 16-bits within a data packet structure described in Fig.6. When only the header detector detects the header sequence (′1011′), address comparator is active. The two-input serial data comparator compares the demodulated data and metal addresses. In order to assemble an addressable network, each chip is designed to have a unique device ID (Fig. 10). We have implemented a 9-bit fuse line using the top metal layer available in the CMOS process. Fuse-bits are set through laser ablation during post-processing and then read out in sequence from right to left. When two addresses both the demodulated data and read-out fuse bits are matched, the chip generates the current to stimulate the brain tissue. We designed that the chip operates with the load

impedance 50 kOhm that was calculated with low impedance electrode and it can be generated by ~36 μA at 1.8 V voltage. To control stimulation time, the chip is designed with a 4-bits counter. When all of bit in the 4-bits counter becomes ′1′, the generated stimulation current is stopped. We designed the 4-bits sequence header detector and the address comparator based on the Moore finite state machine (FSM). To control network with tens of addressable devices, it is noted that the digital output depends on only the current state of the FSM.

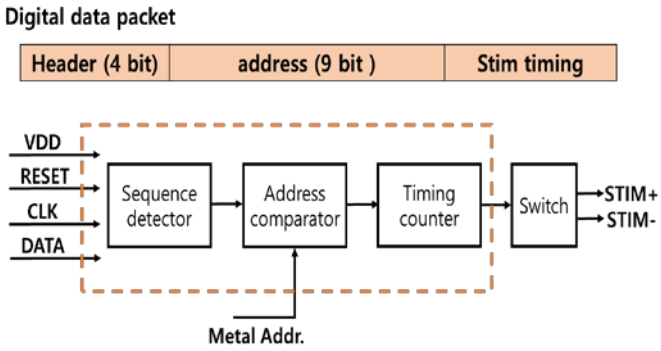

Fig. 8. A single data packet instructing stimulation current and the block diagram of the digital circuitry.

To test three important parts in the digital block for the initial prototype, we have designed three flags at the end of each part, which monitor them in sequence for each three output nodes: the header detector, the address comparator and the timing counter. Firstly, the header detector keeps detecting a specific binary sequence ′1011′ from the input of demodulated data and the its output is set to a high-level voltage only when the header is detected. Then, while the output of the header detector keeps setting the high voltage, the address comparator starts to compare the 9-bits demodulated address following the header bits and the read-out physically curved address. If two addresses are matched, the comparator output will be set to a high-level voltage, otherwise, it is set to a low-level voltage. The flags of the header detector and the address comparator are labelled ′detector_out′ and ′a′, respectively.

To validate discriminating address in the chiplet, the digital block that has a default address (10b’1) is tested in benchtop setup given two kinds of 20 MHz modulated BPSK input signal. One encoding sequence is all of the binary number ‘0’ and the other one is all of ‘1’. In Fig. 9(a), as two addresses are unmatched, the flag ‘a’ goes a low-level voltage during operating the address comparator and the stimulation current is not generated. On the other hand, in a case of matched addresses, ‘a’ keeps a high-level voltage after the header sequence detects and the switch to generate stimulation current turns on described in Fig. 9(b). We measured that the chip was able to source up to 33 μA, which is consistent with simulated values at nominal 1.66V across the 50 kOhm resistor (Fig. 9).

Ongoing work in our hand is the post-CMOS processing to make the electrode that has low impedance to deliver the stimulation current into brain tissue efficiently. We have used poly (3, 4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT: PSS), an organic material with demonstrated history of use for neural simulation applications as the planar structure stimulation electrode material [13]. The photolithographically fabricated 70 μm-sized PEDOT: PSS electrode brought impedance down to 4.33 kOhm at 1kHz.

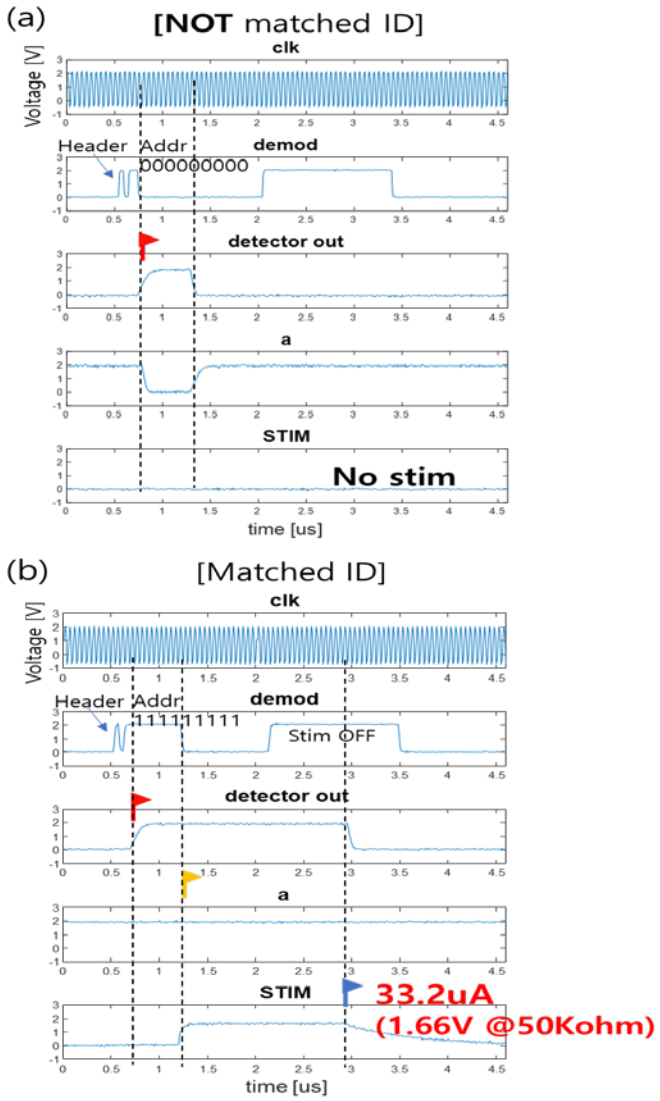

Fig. 9. Measured the digital block three outputs: the header detector ‘detector_out’, address comparator ‘a’, and stimulation current ‘STIM’; (a) when the addresses are not matched and (b) addresses are matched.

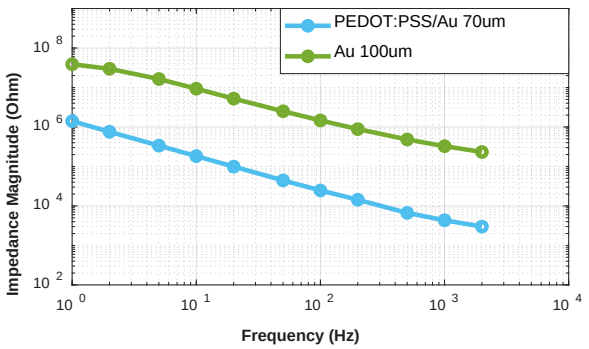

Fig. 10. Impedance spectra of Au and PEDOT: PSS/Au electrode

The total load resistance of the chip is twice the resistance of one electrode because stimulation current goes round-trip between two pads. One pad served as the working electrode and the other one served as the reference electrode. Based on this impedance result, we will target lower load resistance with PEDOT: PSS electrodes (< 10 kOhm) to get higher stimulation current via 1.8V supply voltage, which will be able to generate 150 μA approximately.

TABLE Ⅰ. The layout area for each block

Module	Area
BPSK demodulator	44×47 μm^2
Power on reset	14×65 μm^2
9-bits fuse	40×128 μm^2
Digital block	87×110 μm^2
Total layout.	211×204 μm^2

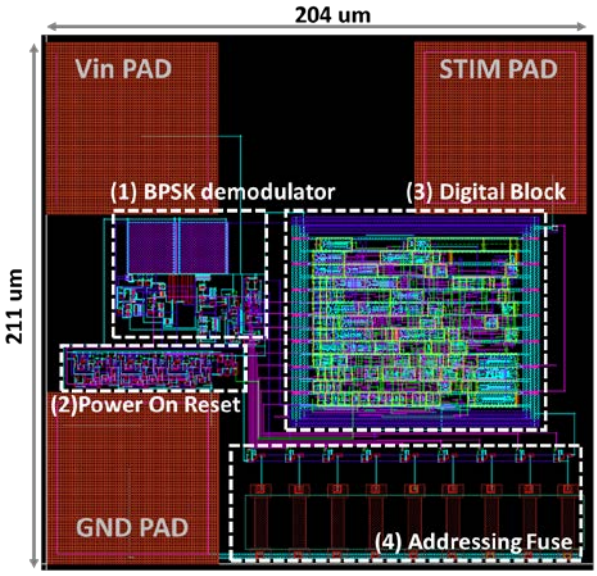

Fig. 11. Layout of the mixed mode chip in 0.18 μm CMOS process

TABLE II. Comparison of the BPSK demodulator

Ref.	Carrier Freq.(MHz)	Data Rate (Mbps)	DRCF Ratio	Power consumption(μW)
[8]	13.56	0.02	0.15%	3000 @ 3.3V
[10]	10	10	100%	77.9 @ 1.8V
[11]	10	10	100%	119 @ 1.8V
[12]	2	1	50%	82 @ 1.8V
This	20	20	-	77 @ 2V

The complete layout of the designed circuit is shown in Fig. 10, occupying the entire area of 204 x 211 μm^2, which is the ultra-small remotely powered stimulator. The area summary of the important blocks in the designed circuit is reported in Table I. Table II compares specifications of the demodulator and clock recovery circuit proposed in this work with some of the recently reported BPSK demodulators at the similar carrier frequency range.

IV. CONCLUSIONS

In this work, we have designed and demonstrated a prototype distributed neural implants for BMI applications. The entire chip was designed with 0.18μm Magnachip/SK Hynics general process using Cadence and tested by using chip-on-board process. Validation of the BPSK demodulator and addressable digital circuit have been demonstrated through the benchtop test. These are the first steps toward the micro-sized addressable neural implant system with the optical powering described in Fig. 3. In the future work, we will process the microfabrication of optical power source using the GaAs photovoltaic cell and its integration into the silicon chip that can be operated fully wirelessly.

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A DC-DC Converter with Voltage-Mode PWM Control

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Abstract **- In this paper, a voltage-mode PWM controlled buck converter is addressed. It consists of a pair of fully-integrated switches, an LC filter, a type 3 compensation loop, an internal ramp & clock generator, and a dead-time generator. A portion of output is taken with a resistive divider and subtracted from an external reference voltage to generate an error voltage. Then the error voltage is compared with a ramp signal, creating a PWM signal for controlling high-side and low-side switches. This buck converter is fabricated in 0.18-μm CMOS process and area of control block is 0.28 mm^2. Input voltage is 3.3 V and target output voltage is 1.8 V. Peak measured power conversion efficiency is 94.38% at 150 mA constant load condition. In a load transient testing from 100 mA to 300 mA, overshoot settling time measures 17.44 us. Overshoot magnitude is 68 mV and undershoot settling time and magnitude is 8.56 us and 60.8 mV, respectively.**

Keywords**—Buck converter, Dead-time, Power conversion efficiency, Voltage-mode PWM control**

I. INTRODUCTION

In many electronic devices, DC-DC conversion is required to supply power with desired voltage level. Since the output voltage of DC-DC converters is supplied as a VDD to subsequent circuits, ripple of the output voltage should be minimized. Linear regulators are well known for their superiority in ripple suppression. However, linear regulators are generally not suitable for applications that need efficient power converters. Efficiency of linear regulators depends on the difference between the input and output voltage level. Assuming a constant input voltage, if required output voltage gets lower, then power that is lost by the linear regulator increases proportionally. The reason for this efficiency degradation is that the voltage drop across a pass transistor of the linear regulator is the output voltage subtracted from the input voltage. Therefore, in order to maximize the efficiency of linear regulators, the output voltage should be close enough to the input voltage [1]. In other words, output voltage range of linear regulators lacks flexibility.

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Another problem arises when high current flows through pass transistors. Not having any switching elements, linear regulators have to let the current flow all the time which results in excessive thermal stress [2]. To disperse the heat effectively heat sinks could be adopted, which will make the system bulkier [3]. So it is not a decent solution for applications that require compact circuits.

One good example of such applications is portable devices. These run with a rechargeable battery that only supplies limited amount of energy. Among many aspects, especially when it comes to maximizing battery life of portable devices there has been an increasing demand for efficient DC-DC converters. Switched-mode power supply (SMPS) is inherently efficient compared to linear regulators [4], because its pass transistors toggle between on and off state to minimize the wasted energy. Also the switching action reduces heat dissipation, which allows DC-DC converters to operate without any heat sink, or at least smaller heat sink.

In this work, a voltage-mode pulse width modulation (PWM) controlled buck converter is implemented. In Section II, structure of the buck converter control circuits and details of important sub-blocks are explained. Simulation and measurement results are discussed in Section III. And lastly the conclusion is given in Section IV.

II. DESIGN METHODOLOGY

A. Block Diagram

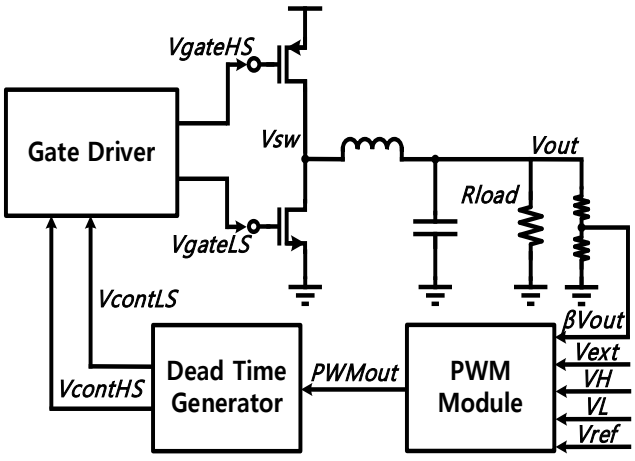

Fig. 1. Top block diagram of voltage-mode PWM controlled buck converter

Fig. 1 shows the overall structure of the proposed work. It consists of two CMOS switches, an off-chip inductor, an off-chip capacitor, a load circuit, a PWM module, a dead-time generator, and a set of gate drivers. At cold start, high-side pMOS switch is initially turned on and inductor current builds up during on-state. After on-state, off-state begins and high-side pMOS switch is turned off while low-side nMOS switch is turned on for the continuous flow of inductor current. With a pair of identical resistors that are integrated in the chip, a portion of the output voltage βV_{out}, which is half in this work, is delivered to the PWM module. By subtracting βV_{out} from an external DC voltage V_{ext}, amplified error voltage is produced. Then that error voltage is compared with an internally-generated ramp voltage to generate a digital control signal *PWMout*. The structure of PWM module is illustrated in Fig. 2.

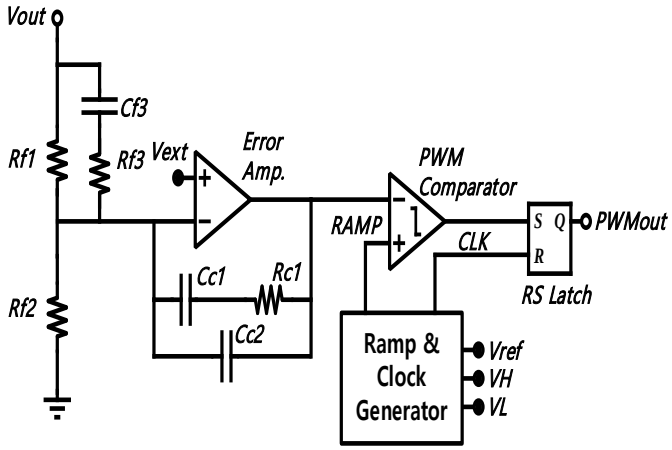

Fig. 2 Structure of PWM module

B. Type 3 Compensation Loop

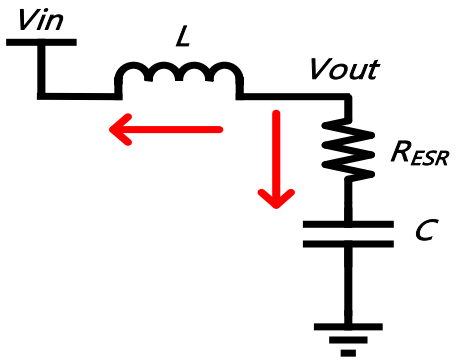

Fig.3 Simple modeling of the LC filter of a buck converter for analyzing double pole and ESR zero

From the simplified structure of a buck converter, a Kirchhoff's Current Law (KCL) equation

$$\frac{V_{out}-V_{in}}{sL}+\frac{V_{out}}{R_{ESR}+\frac{1}{sC}}=0 \quad (1)$$

is obtained. Therefore the frequency of double pole and equivalent series resistance (ESR) zero is

$$f_{LC}=\frac{1}{2\pi\sqrt{LC}} \quad (2)$$

$$f_{ESR}=\frac{1}{2\pi R_{ESR}C} \quad (3)$$

, respectively. To reduce output voltage ripple, ESR should be minimized and that usually set the frequency of ESR zero much higher than that of the double pole [5]. Phase will reach -180° before ESR zero boosts the phase. Thus there is a need for a compensation loop that counteracts the double pole for power stage stability.

A type 3 compensation loop is adopted for the PWM module to cancel the phase drop caused by the LC filter. In Fig. 2 additional passive components *Rf3*, *Cf3*, *Cc1*, and *Rc1* are added to the basic feedback path to introduce two zeros and two poles for compensation. Values of the components are chosen by the following procedure [5]:

1. Choose switching frequency f_{sw} and crossover frequency f_{cross}. Rule of thumb is $0.1f_{sw} \le f_{cross} \le 0.2f_{sw}$.

$$f_{sw}=870\ kHz \rightarrow\ f_{cross}=87\ kHz \quad (4)$$

2. Calculate double pole frequency f_{LC} and ESR zero frequency f_{ESR}.

$$f_{LC}=\frac{1}{2\pi\sqrt{10uH*6.8uF}}=19.3\ kHz \quad (5)$$

$$f_{ESR}=\frac{1}{2\pi*45m\Omega*6.8uF} \quad (6)$$

3. Decide frequency of required poles and zeros.

$$f_{z2}=f_{LC}=19.3\ kHz \quad (7)$$

$$f_{z1}=0.75*f_{z2}=14.5\ kHz \quad (8)$$

$$f_{p2}=f_{ESR}=487.6\ kHz \quad (9)$$

$$f_{p3}=\frac{f_{sw}}{2}=439\ kHz \quad (10)$$

4. Calculate passive components. Start by giving a reasonable value to C_{f3}.

$$C_{f3}=10\ pF \quad (11)$$

By selecting $L=10\ uH$ & $C=6.8\ uF$,

$$R_{f3}=\frac{1}{2\pi*C_{f3}*f_{p2}}=30.6\ k\Omega \quad (12)$$

$$R_{f1}=\frac{1}{2\pi*C_{f3}*F_{z2}}-R_{f3}=794\ k\Omega \quad (13)$$

$$R_{c1} = \frac{2\pi * f_{cross} * L * C * V_{osc}}{V_{in} * C_{f3}} = 2.271 \ M\Omega \quad (14)$$

$$V_{osc}: \ ramp \ voltage \ magnitude$$

$$C_{c1} = \frac{1}{2\pi * R_{c1} * f_{z1}} = 4.84 \ pF \quad (15)$$

$$C_{c2} = \frac{1}{2\pi * R_{c1} * f_{p3}} = 159.7 \ fF \quad (16)$$

$$R_{f1} = R_{f2} = 1 \ M\Omega \ for \ precise \ matching$$

Grounds for selecting the frequency of each pole and zero is summarized in Table. I.

TABLE I. Grounds for the frequency of poles and zeros

Frequency	Grounds
f_{z1}	Compensating DC pole
f_{z2}	Compensating a pole of the LC filter
f_{p2}	Cancelling the ESR zero
f_{p3}	Attenuating frequency components higher than the half of the switching frequency
f_{cross}	Suppressing output voltage ripple

C. Ramp & Clock Generator

On-chip ramp & clock generator is utilized in this work. The generator receives three external DC voltages that define the frequency of generated ramp and clock signals.

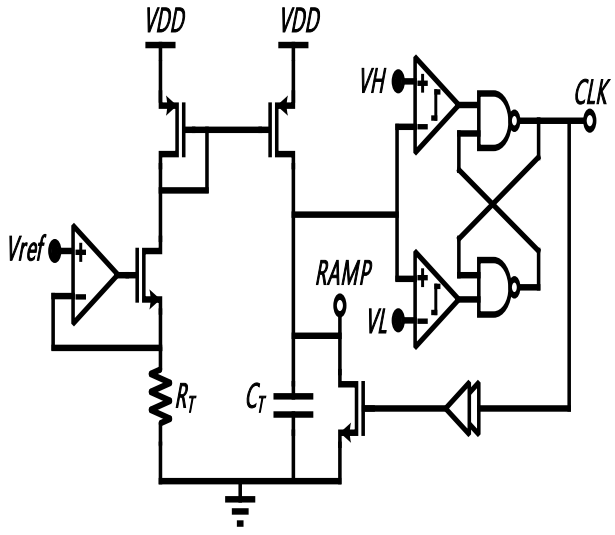

Fig. 4 Structure of ramp & clock generator

In Fig. 4 the schematic of the ramp & clock generator is given [6]. After start up, V_{ref} is assigned across R_T and current defined by the resistor is mirrored to another branch. That current charges C_T and rising ramp signal is generated. When ramp signal exceeds voltage *VH*, *CLK* is set to logical high. Then an nMOS transistor turns on and discharges C_T until it goes below *VL*. As soon as discharging phase finishes the nMOS transistor is turned off and subsequent charging phase follows.

The frequency of ramp and clock signals can be approximated as,

$$f_{sw} = \frac{V_{ref}}{(V_H - V_L) * C_T R_T} \quad (17)$$

Parameters are chosen to simplify calculations.

TABLE II. Parameters for ramp and clock signals

Parameter	Value
V_{ref}	1 V
V_H	2.5 V
V_L	0.5 V
C_T	5 pF
R_T	100 kΩ
f_{sw}	870 kHz

Strength of nMOS and pMOS transistors decides the speed of charging and discharging C_T. The strength is designed to set the time ratio of ascending and descending as 91.2:8.8. This is a dominant factor of the duty-cycle range of the buck converter. Since this work targets output voltage lower or equal to 3 V with the input of 3.3 V, maximum duty-cycle of the converter is limited to 91.2% whereas lower bound of it is 8.8%. To push the range further, wider transistors are needed.

D. Dead-Time Generator

In a buck converter, pMOS and nMOS switches toggle in complementary manner. Ideally the switches change their state instantly, but they spend some time to change in practical cases. If the on-state of nMOS and pMOS transistors coincide then shoot-through current flows directly from VDD to VSS. The rush of current can be observed as a sharp spike and that degrades the overall efficiency of the buck converter. Therefore, there should be a way to force a switch to be toggled only after turning off the previously on-state switch.

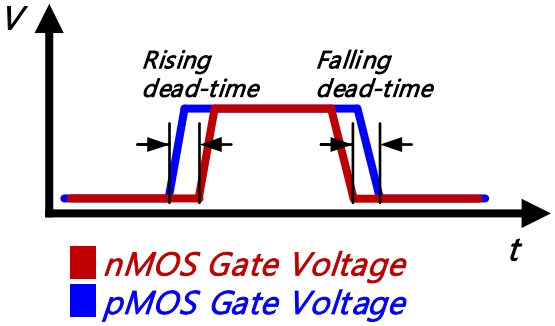

Fig. 5 Definition of dead-time

The amount of time interval between the state transition of a high-side switch and a low-side switch is defined as dead-time. It should be noted that if dead-time is too short then partial shoot-through current will flow whereas body diode of the nMOS transistor will be a conduction path for the inductive current that has been flowing if dead-time is too long. Without the transition of the pMOS transistor, output voltage of buck converter will continue to fall.

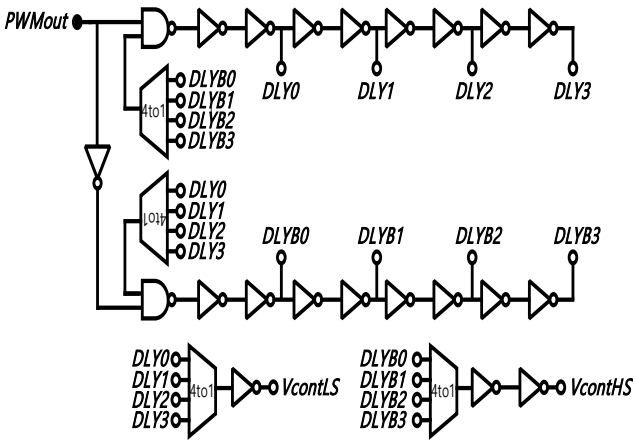

Fig. 6 Structure of dead-time generator

Fig. 6 shows the structure of the dead-time generator. 4-to-1 multiplexers are controlled by a 2-bit external input SEL, realized by two single-put-double-throw switches soldered on a testing printed circuit board (PCB). Dead-time of gate driving signals is the number of inverter stages multiplied by propagation delay. Dead-time can be controlled within the range from 1.7 ns to 4.9 ns by selecting the number of inverter stages with external digital input.

TABLE III. List of available dead-times

SEL<1>	SEL<0>	Rising dead-time [ns]	Falling dead-time [ns]
0	*0*	1.78	1.96
0	*1*	2.88	3.06
1	*0*	3.98	4.16
1	*1*	4.89	5.07

III. RESULTS AND DISCUSSIONS

Chip micrograph is shown in Fig. 7. Dummy metal blocking layer was applied to the PWM module, the ramp and clock generator, the dead-time generator, a bias circuit, and a high-side gate driver.

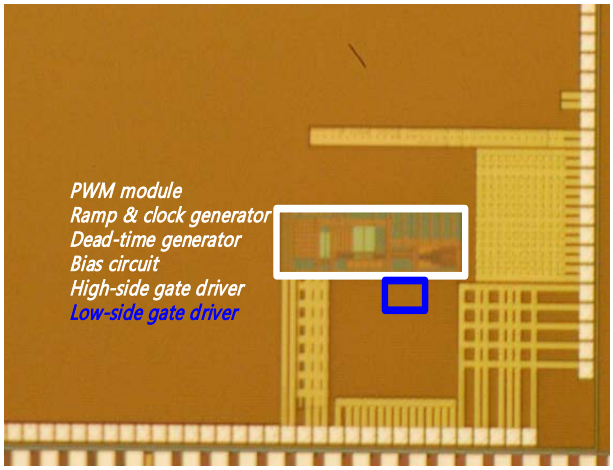

Fig. 7 Chip micrograph

Some off-chip components were used to configure a testing PCB. A list of components is shown in Table IV. An aluminium electrolytic capacitor is used to minimize output voltage ripple by reducing ESR.

TABLE IV. List of off-chip components

Components	Value/ Usage
LT3042	Off-chip low dropout regulator
SMD inductor	10 uH/ LC filter
Aluminium electrolytic capacitor	6.8 uF/ LC filter
IRLZ24N	Off-chip power MOSFET/ Load-controlling transistor

* SMD: Surface-Mount Device

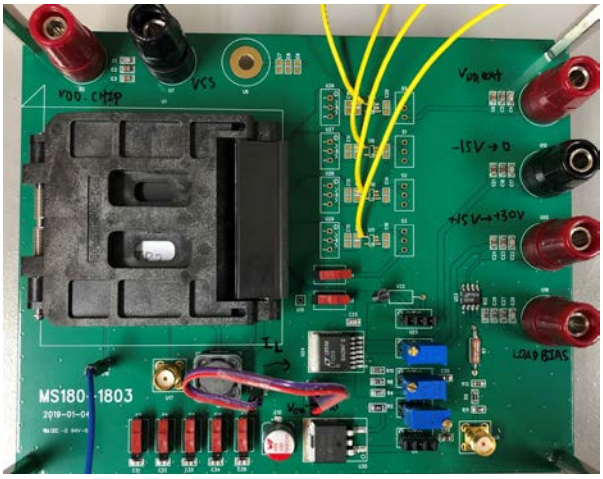

Fig. 8 Configuration of the testing PCB

Two-bit input of the dead-time generator was toggled to check the difference. However, calculated output power based on measured results showed almost no difference which was 542.7 mW in 300 mA constant load. Considering possible measurement error, the minimum and maximum dead-time did not make noticeable difference to efficiency.

Inductor current in no load condition is measured with a current probe and a digital phosphor oscilloscope. DC coupled output voltage and inductor current is illustrated in Fig. 9. The frequency of inductor current is 877.2 kHz, which is in phase with the internally generated ramp and clock signal. Average output voltage is 1.81V.

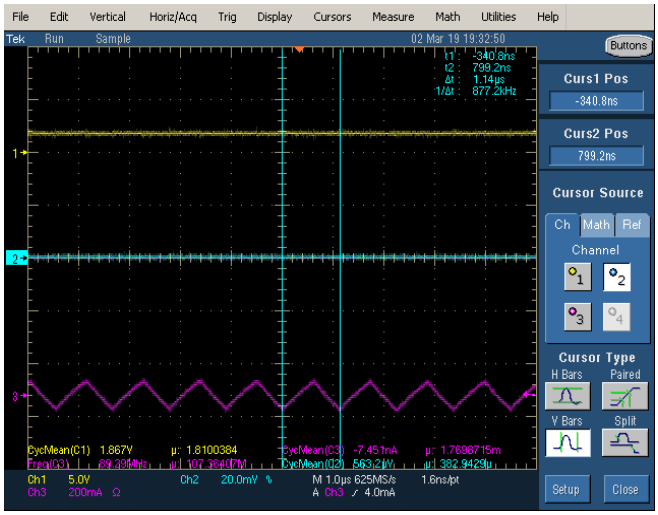

Fig. 9 Measurement result of no load condition

Inductor current in 100 mA constant load condition is measured and the result is plotted in Fig. 9. AC coupled output voltage ripple is measured to stay in a 5.2 mV voltage window.

Fig. 10 Measurement result of 100 mA constant load condition

In Fig. 11, power conversion efficiency (PCE) is calculated and plotted based on measured results. Load current is swept from 0 to 1.57 A. Maximum PCE is 94.38 % when the load current is 150 mA. PCE in high-load current condition fell below 90 % because there are some undesired parasitic resistances in testing PCB configuration. A pair of short jump wires was used to connect the LC filter inductor and capacitor, which made it easy to install a current probe.

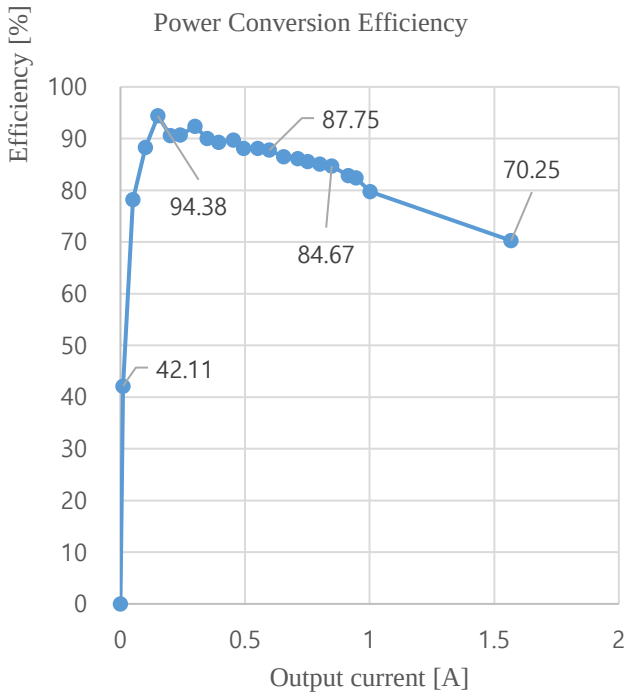

Fig. 11 Plot of PCE versus output current

Load transient test from 100 mA to 300 mA is measured. The result is shown in Fig. 12. Square wave signal is applied to the gate of an off-chip power MOSFET to make a load transition. Frequency of the square wave signal is 2 kHz and rising time and falling time is both 1 ns. Average output voltage is 1.816 V and average output current is 195.11 mA.

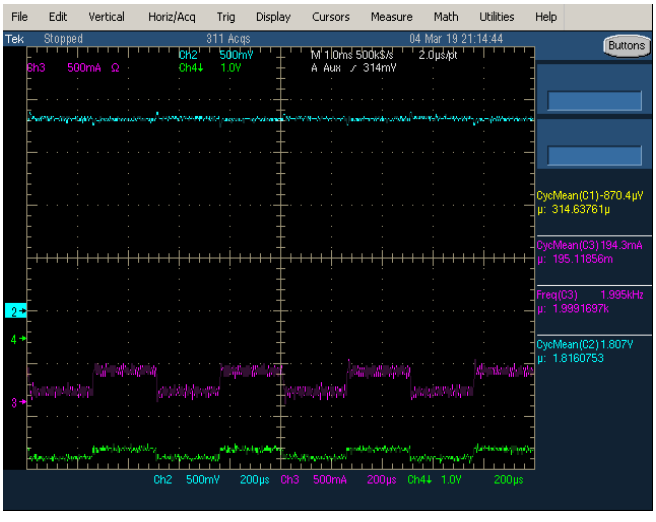

Fig. 12 Measurement result of a load transient condition from 100 mA to 300 mA

AC coupled output voltage is measured in the same load

TABLE V. Comparison table

	[7]	[8]	This work
Technology	TSMC 0.35 um	0.18 um	Magnachip 0.18 um
Control mode	Hysteresis & dynamic frequency	Hysteresis & PFM	PWM
Input voltage	2.7 ~ 4.2 V	2.7 ~ 3.3 V	3.3 V
Output voltage	2 V	1.2 V	1.8 V
Inductor	10 uH	1.2 uH	10 uH
Capacitor	20 uF	22 uF	6.8 uF
Load current range	20 m ~ 600 mA	10 m ~ 500 mA	50 m ~ 1 A
Switching frequency	50 k ~ 1.38 MHz	9.7 k ~ 250 kHz (light load) 1.97 MHz (heavy load)	870 kHz
Load transient	8.26 us (100 mA to 600 mA) 7.44 us (600 mA to 100 mA)	3.7 us (500 mA to 10 mA)	8.56 us (100 mA to 300 mA) 17.44 us (300 mA to 100 mA)
Overshoot/ undershoot	79 mV/ 67 mV	2.5 mV	68 mV/ 60.8 mV

transient condition to measure overshoot and undershoot. Fig. 13 and Fig. 14 display cursors on an overshoot situation and an undershoot situation, respectively. Measured values are listed in Table VI.

Fig. 13 Measurement result of output voltage overshoot

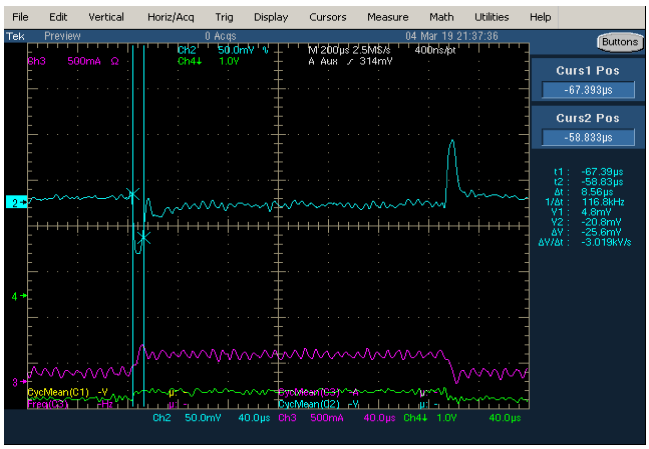

Fig. 14 Measurement result of output voltage undershoot

TABLE VI. List of measured values in load transient condition

Average output voltage = 1.81 V	
Overshoot settling time	17.44 us
Overshoot magnitude	68 mV
Undershoot settling time	8.56 us
Undershoot magnitude	60.8 mV

IV. CONCLUSION

A voltage-mode PWM controlled buck converter is presented in this paper. A type 3 compensation loop effectively deals with a double pole and an ESR zero caused by an LC filter of the buck converter. The procedure of deciding passive components for the poles and zeros introduced by the compensation loop is fully covered. Internal ramp and clock generator eliminated the needs for external ramp and clock input. Operating frequency can be controlled by modifying applied DC voltage to the generator. To resolve shoot-through current problem, a dead-time generator is implemented. This work achieved maximum PCE of 94.38 % and overshoot and undershoot settling time 17.44 us and 8.56 us, respectively.

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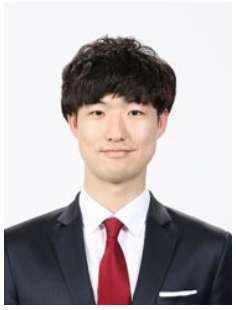

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Dual-Mode Noninverting DC-DC Buck Converter for Wearable AMOLED Display

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Abstract **− This paper proposes a highly integrated dual-mode noninverting DC-DC buck converter for wearable AMOLED display panels. The DC-DC buck converter is designed to increase power efficiency under light load using PWM-SPWM (set-time variable pulse width modulation) dual-mode. The major role of the PWM-SPWM controller is to switch frequency according to the load current by changing only the set signal using the VCO (voltage controlled oscillator) in the conventional PWM control signal. The converter generates variable output voltages by changing reference voltage of error amplifier. The proposed circuit has been designed using a 0.35 μm standard CMOS process and its core area of 1.2 mm x 1.3 mm. The measurement results show that the proposed circuit has power efficiency of 65% ~ 75% with output voltage of 2.0 V ~ 2.7 V for a load current range of 5 mA ~ 50 mA and input voltage 3.3 V ~ 4.2 V.**

Keywords**— AMOLED, buck converter, DC-DC converter, dual-mode, PWM**

I. INTRODUCTION

The market of portable devices such as cellular phones, PDAs, video game consoles, and wearable watches has been rapidly expanding and this trend has led to a large emerging market for switching power ICs [1]. Because of the switching power IC's high efficiency, small size, and low power consumption, it is suitable to be a power supply model for mobile devices [2-7]. Especially since mobile devices left in the standby mode have long usage time, the power efficiency of switching power IC under light load is a crucial factor for selecting the power supply circuit. [6-7]. An AMOLED display panel requires two supply voltages, a positive voltage and a negative voltage [8]. High power efficiency and being able to vary output voltage in the DC-DC converters are the two most important aspects for positive voltage.

In this paper, a noninverting DC-DC buck converter is proposed to increase power efficiency in PWM-SPWM dual-mode. The converter has variable output voltages by changing reference voltage of error amplifier. This paper is organized as follows. Design methodology of a DC-DC buck converter is presented in Section II. Measurement results of the proposed DC-DC converter are described in Section III. Conclusions are finally drawn in Section IV.

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II. DESIGN OF DC-DC BUCK CONVERTER

We design a PWM-SPWM dual-mode DC-DC buck converter with variable positive output voltage for low power wearable AMOLED display panel. The dual-mode DC-DC converter operates in the PWM mode under heavy load, and in the SPWM mode under light load in which the switching frequency of the set-time is changed in proportion to the load current in the PWM mode. Table I shows the major design specifications of the proposed DC-DC buck converter. For an input voltage of 3.3 V to 4.2 V, the DC-DC buck converter has an output voltage of 2 V to 2.7 V. Figure 1 is the block diagram of the proposed DC-DC converter for a positive voltage V_{POS} of wearable AMOLED display panel. In the DC-DC converter for V_{POS}, a PWM-SPWM dual-mode is adopted to achieve high power efficiency. The converter operates in the current mode control (CMC) when the output voltage and the inductor current are fed back and the output voltage is constant. The converter includes an error amplifier that compares the feedback voltage with the reference voltage to amplify the error with the target output voltage, a current

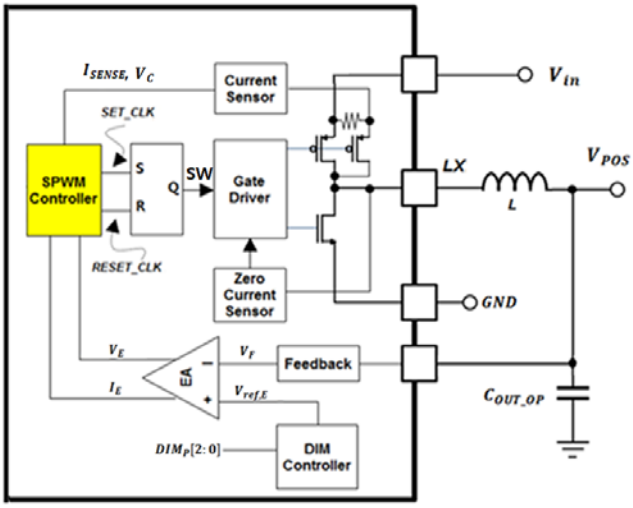


Fig. 1. Block diagram of the proposed DC-DC buck converter

sensor that detects the inductor current, a zero current detector that detects the reverse current of the inductor and a PWM-SPWM controller that adjusts switching frequency or pulse width according to load current, as well as a gate driver that controls on/off of the power switching transistors.

TABLE I
Specifications of the proposed DC-DC buck converter.

Item	Specification
Process	0.35 μm CMOS
Input voltage	3.3 V ~ 4.2 V
Output voltage	2 V ~ 2.7 V
Load current	5 mA ~ 50 mA
Frequency	0.15 MHz ~ 1.4 MHz
Output voltage ripple	< 5 mV
External inductor	4.7 μH

A. PWM-SPWM controller

The major role of the PWM-SPWM controller is to switch frequency depending on the load current by changing only the set signal through the VCO in the conventional PWM control signal. This controller is a switching control circuit to reduce the power loss under light load by generating a switching frequency proportional to the load under light load. Fig. 2 illustrates the proposed PWM-SPWM controller. The VCO generates a set signal V_{VCO_ref} whose frequency is varied by an error voltage V_E that changes with the load current. Also, a set signal V_{comp_set} generates a fixed switching frequency. A mode selector composed of two flip flops chooses a signal with a low frequency, and a set signal V_{setclk} is generated. The current comparator compares the inductor current I_{SENSE} with the sum of the ramp waveform I_{RAMP} and the error voltage V_E to generate the reset clock $V_{resetclk}$. Set clock V_{setclk} and reset clock $V_{resetclk}$ are applied to the SR latch to generate the control signal for the power switching transistor.

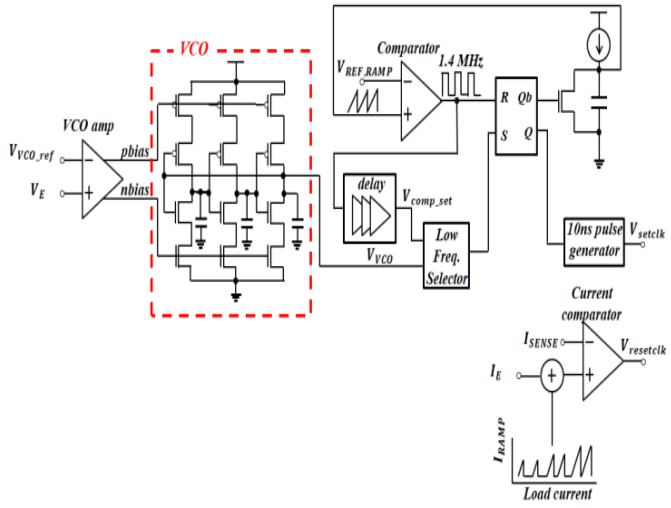


Fig. 2. Proposed SPWM controller.

The proposed PWM-SPWM controller requires only a simple low frequency selector to operate dual-mode. So, it can be implemented in a small area, and since it has a set signal periodically, its ripple voltage is smaller than PSM.

Fig. 3 shows the SPWM waveform of the buck converter. Under a light load of less than dual- mode switching load current I_{MC} (max current), the set clock V_{setclk} senses the output voltage V_E of the error amp, and the reset clock $V_{resetclk}$ senses the inductor current through the current sensor so that the switching frequency is modulated in proportion to the load current. Under a heavy load larger than load current I_{MC}, the set clock V_{setclk} is generated with a constant maximum frequency irrespective of load current, so that the switch signal SW operates in the PWM mode with constant frequency.

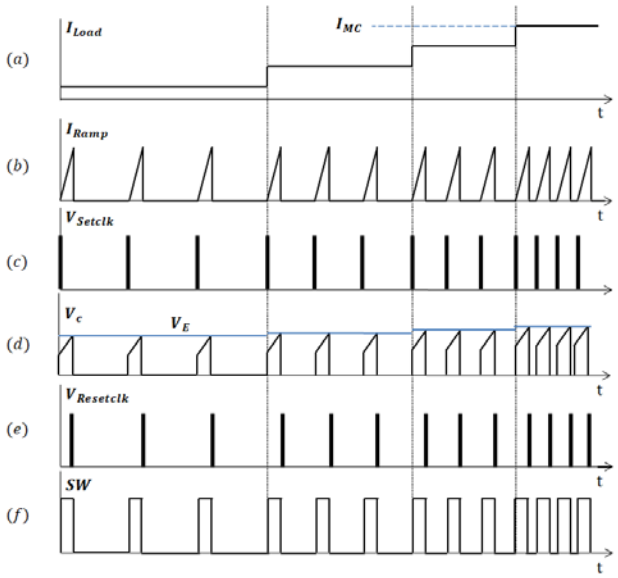


Fig. 3. Waveform of SPWM method (a) Load current I_{MC} , (b) Ramp current I_{Ramp}, (c) Set clock signal V_{setclk}, (d) Current sensing voltage V_C and error amplifier voltage V_E, (e) Reset clock signal $V_{resetclk}$, (f) Switching pulse SW.

B. Variable output voltage

Fig. 4 shows a variable output voltage circuit for V_{POS}. The V_{POS} is determined by the ratio of the feedback resistor and reference voltage VREF_P as shown in equation (1).

$$V_{POS} \times \frac{R_B}{R_A+R_B} = \text{VREF\_} \quad (1)$$

The output voltage is adjustable by changing the reference voltage VREF_P of the error amplifier with resistors and a multiplexer according to external control signals DIM_P[2:0]. According to external control signals, 8 reference voltages are generated as shown in TABLE II to determine output voltage.

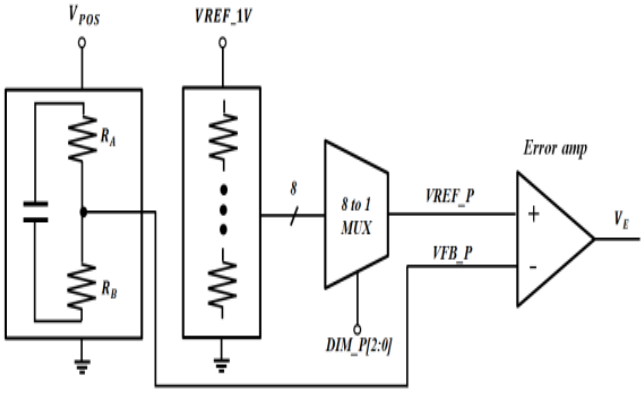


Fig. 4. Variable output voltage circuit for V_{POS}.

TABLE II. Variable output voltages by external control signals DIM_P[2:0].

DIM_P[2:0]	V_{POS} [V]
000	2.0
001	2.1
010	2.2
011	2.3
100	2.4
101	2.5
110	2.6
111	2.7

III. MEASUREMENT RESULTS

DC-DC buck converter which proposed in Section II has been designed through a 0.35 μm CMOS standard process. Fig 5 shows the chip photograph of the proposed converter whose chip area is 1.2 mm × 1.3 mm.

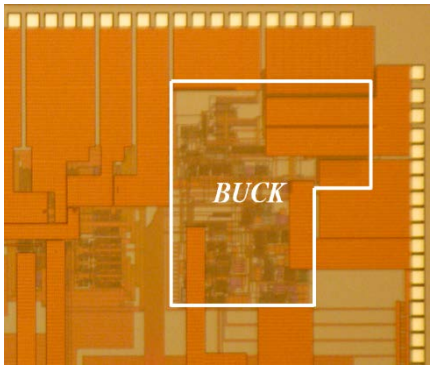
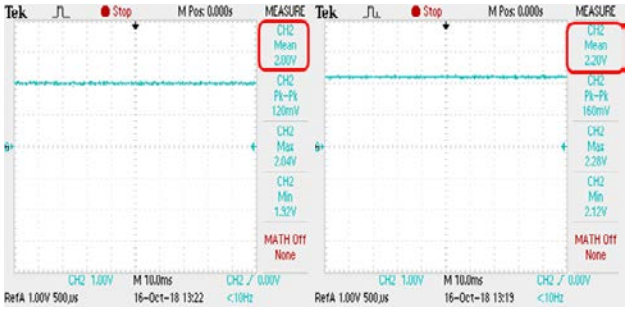
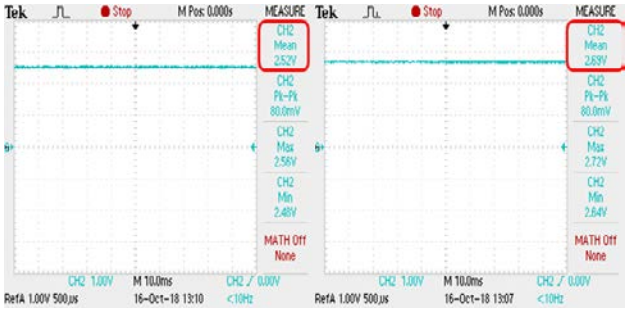


Fig. 5. The photograph of the proposed DC-DC buck

Fig. 6 demonstrates the output voltage of buck converter by external control signals DIM_P[2:0]. It can be seen that the output voltage varies from 2.0 V to 2.7 V according to the external control signal as shown in TABLE II.

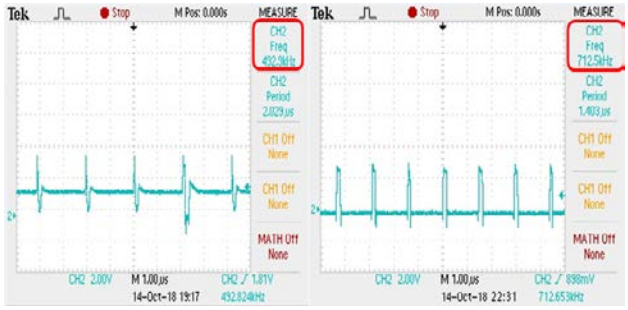


(a) 2.0V (b) 2.2V



(c) 2.5V (d) 2.7V

Fig. 6. Output voltage of buck converter by external control signal DIM[2:0]. (a) DIM[2:0] = 000, (b) DIM[2:0] = 010, (c) DIM[2:0] = 101, (d) DIM[2:0] = 110.



(a) 492 kHz @ 10 mA (b) 712 kHz @ 20mA

(c) 1.027 kHz @ 40 mA (d) 1.043 kHz @ 50mA

Fig. 7. The PWM-SPWM switching frequency according to load current.

Fig. 7 shows the PWM-SPWM switching frequency of external inductor LX according to load current. The switching frequency varied from 492 kHz to 1.04 MHz for load currents of 10 mA ~ 50 mA.

Fig. 8 shows power efficiency according to load current. (b) is a simulation result using only the previous PWM mode and (a) shows a simulation result on dual-mode. The result (a) has 8% more efficient than (b). (c) shows a measured result using dual-mode with power efficiency of 65.5% ~ 77.3% under loads of 5 mA ~ 50 mA. However, the power efficiency of (c) is 16% lower than that of (a) because of several factors of power dissipations. First one is latch-up phenomenon. It causes leakage current of parasitic BJT using a standard CMOS process. Leakage current increases the input current. The other is caused by a shoot-through current flowing through the CMOS power transistor being turned on simultaneously.

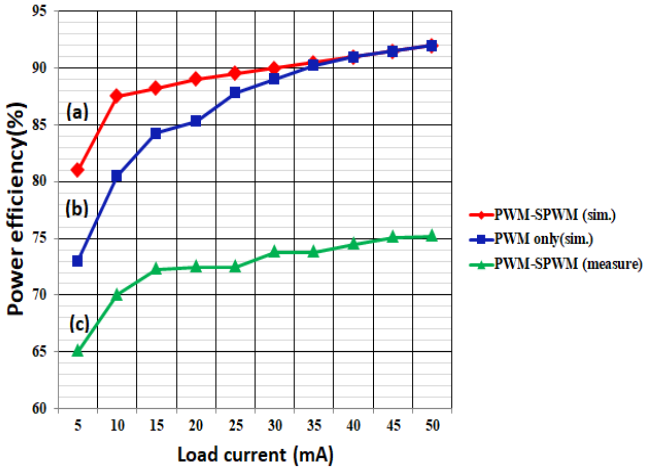


Fig. 8. Measurement results of power efficiency according to load current.

V. CONCLUSION

A dual-mode noninverting DC-DC buck converter for wearable AMOLED display has been designed. The converter uses a dual-mode with PWM-SPWM controller using the VCO, and has variable output voltages by changing reference voltage of error amplifier.

The converter has been implemented in a chip with 1.2 mm x 1.3 mm using a 0.35 μm standard CMOS process. Measurement results show that output voltage has 2.0 V ~ 2.7 V for input voltage of 3.3 V ~ 4.2 V. And the converter has a power efficiency of 65% ~ 75% under a load current of 5 mA ~ 50 mA. In simulation results, the dual-mode DC-DC converter is 8% higher in power efficiency than the previous converter using only the PWM mode.

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In-Band Full-Duplex Transceiver Using Phase Locked Loop for Impedance Change Tracking

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Abstract **- This paper describes the design of an integrated in-band full-duplex transceiver using phase locked loop. Generally, the transmission signal leakage to the receiver is detected in a transceiver with a single antenna. In order to minimize the signal leakage, a method of isolation between the leakage signals from the transmitter and the receiver is adopted. We suggest a method of impedance change tracking based on phase locked loop system, which can maintain high isolation between the transmitter and the receiver. Phase locked loop is therefore employed to sense the transmitter leakage and tune the impedance of the balance network. The TX port reflection coefficient of -29.65 dB at 1.95 GHz, the antenna port reflection coefficient of -28.09 dB, the RX port reflection coefficient of -26.41 dB, TX insertion loss of -11.58 dB, -45.2 dB the results of TX-RX isolation were obtained through measurements. The proposed circuit is fabricated in the area of 4mm x 4mm.**

Keywords **— Duplex Transceiver, Phase Locked Loop (PLL)**

I. INTRODUCTION

The development of wireless communication systems and the diversity of wireless communication technologies are increasing exponentially. However, Radio frequency resources are becoming increasingly depleted worldwide. A full duplexer has been commonly used in frequency division duplex (FDD) system to isolate the transmitter and the receiver while sharing the same antenna. However, because of the bandwidth limitation, integrating transmitter and receiver bands are considered as an important assignment. The integrated duplexer can reduce the bandwidth requirement and also maintain high isolation between the transmitter and the receiver. RF duplexer using a hybrid transformer and tunable CMOS integrated duplexer based on impedance tracking have been demonstrated [1, 2].

In this paper, an impedance tracking system based on phase locked loop (PLL) which can measure the transmitter leakage and tune the impedance of the balance network is suggested as shown Fig.1.

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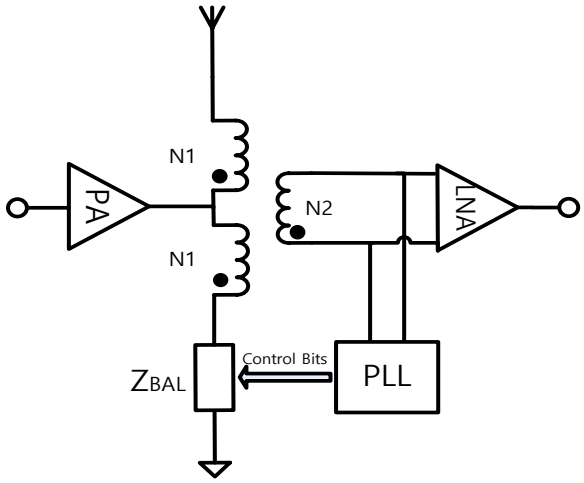

Fig. 1.The integrated full duplexer transmitter based on phase locked loop.

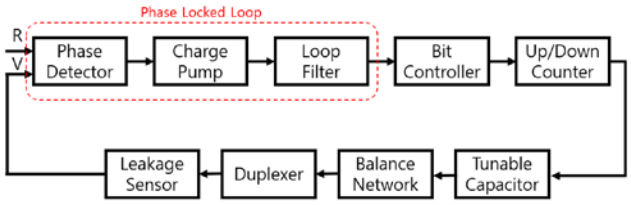

Fig. 2. Block diagram of the integrated full duplexer transmitter based on phase locked loop.

II. EXPERIMENTS

A block diagram of the integrated full duplexer based on phase locked loop is shown in Fig. 2. The self-interference signal received from the antenna is detected by a leakage sensor and a Phase/Frequency Detector(PFD). The PLL, which consists of PFD, Charge Pump, and Loop Filter transmits the sensed signal to the Balance Network, which generates the impedance equal to the impedance of the antenna and tracks the impedance of the antennas. Due to interactions between the user and the antenna, as the capacitance seen at the antenna varies, transmitter leakage increases. The transmitter leakage is shown in Fig. 3 and Fig. 4. Using the phase of transmitter leakage, the varactor determines whether to increase or decrease the capacitance in the balance network.

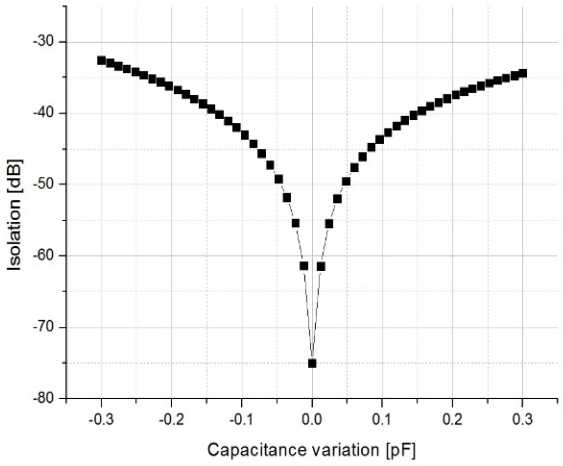

Fig. 3.Isolation between TX and RX by antenna capacitance variation.

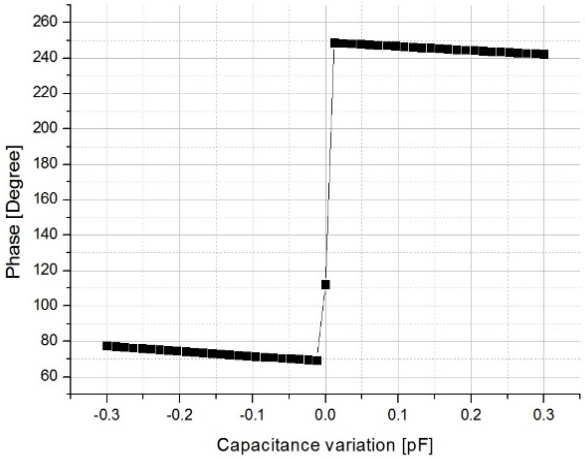

Fig. 4. Phase of the transmitter leakage by antenna capacitance variation.

A. Phase Detector

The phase detector consists of two D-flip flops (D-FF), one NAND gate, and several inverters refining the signals as shown in Fig. 5. D-FF detects the rising edge which can represent the phase of signal as described in Fig. 6. When both D-FFs are set, the value will be reset. The difference between the rising edges of transmitter leakage signal and the reference signal is transported to the charge pump.

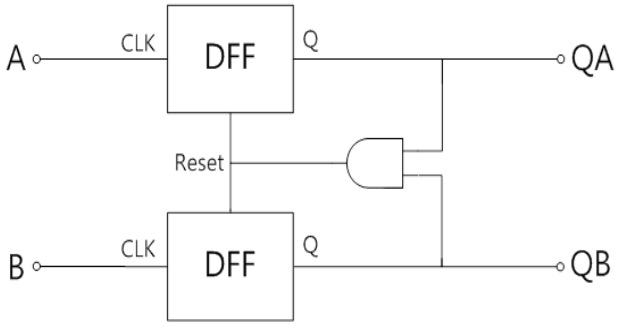

Fig. 5. Block diagram of the phase detector.

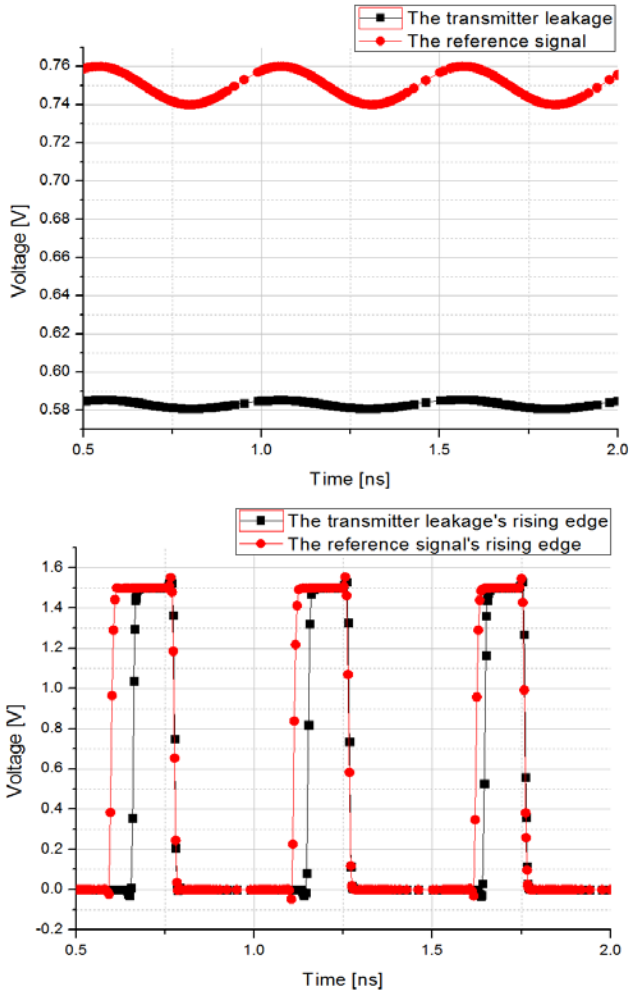

Fig. 6. Input and output voltages of the phase detector.

B. Charge Pump and Loop Filter

A charge pump detects the difference between the rising edges of transmitter leakage signal and the reference signal and adjusts the control voltage by charging or discharging the capacitor of loop filter as shown in Fig.7. A loop filter plays the role of a low pass filter (LPF) and a charge collector.

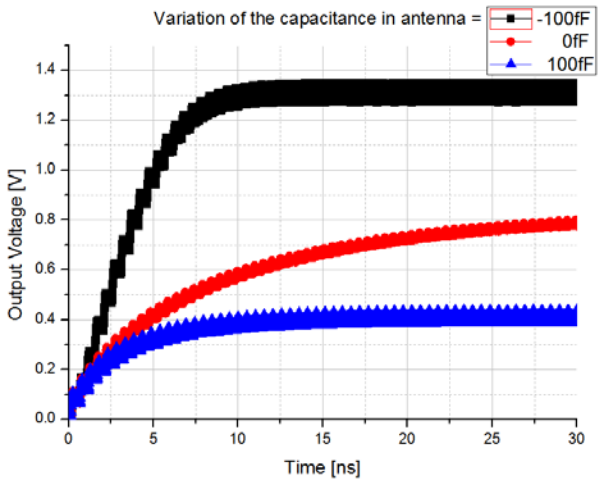

Fig. 7. Output voltage of charge pump and loop filter.

C. Bit Controller

Bit controller consists of six inverters, one NAND gate and one NOR gate as shown in Fig. 8. Two inverters in front divide the input voltage into three parts as shown in Fig. 9. And the NAND gate, the NOR gate and rest of the inverters determines whether to increase, decrease or maintain the control bits.

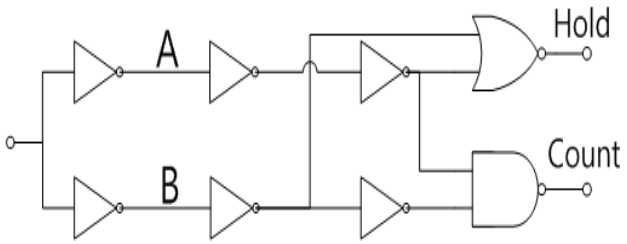

Fig. 8. Block diagram of Bit Controller.

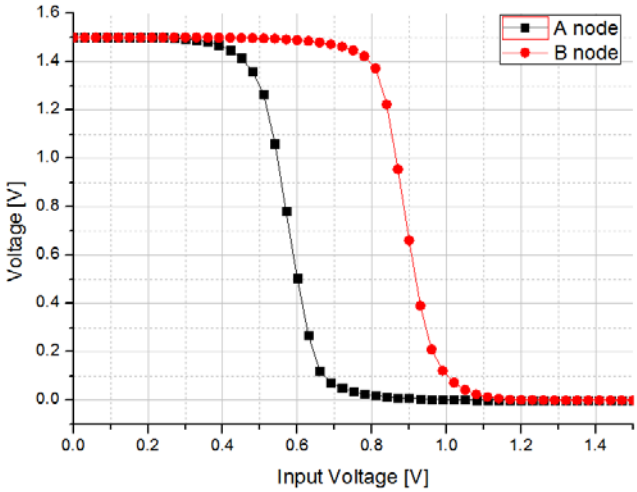

Fig. 9. Three parts of the input voltage at A and B node.

D. Up/down Counter

Up/down counter consists of three JK flip-flops, four NOR gates, four AND gates and two inverters as shown in Fig. 10. According to COUNT bit, control bits increase or decrease, and HOLD bit maintains the control bits.

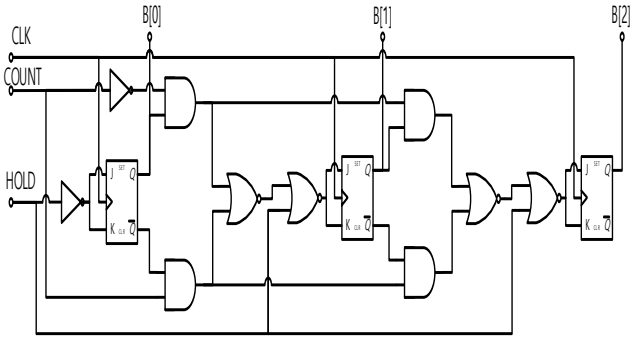

Fig. 10. Block diagram of Up/down counter

E. Tunable Capacitor

Tunable capacitor is placed in the balance network and the unit of tunable capacitor is 100fF as shown in Fig. 11.

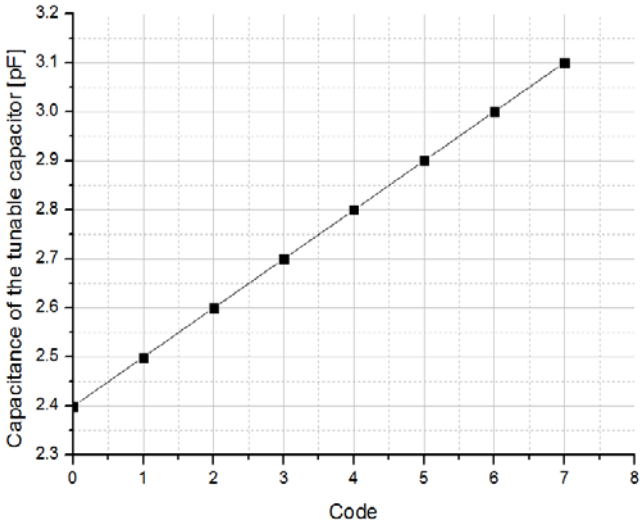

Fig. 11. Tunable capacitor with 100fF/step.

By the variation of the capacitance in antenna, the isolation get poor. But PLL system tracks the impedance variation of the antenna, therefore maintain high isolation between the transmitter and the receiver as shown in Fig. 12 and achieves average isolation of 65.5 dB and power consumption of 321.5 uW.

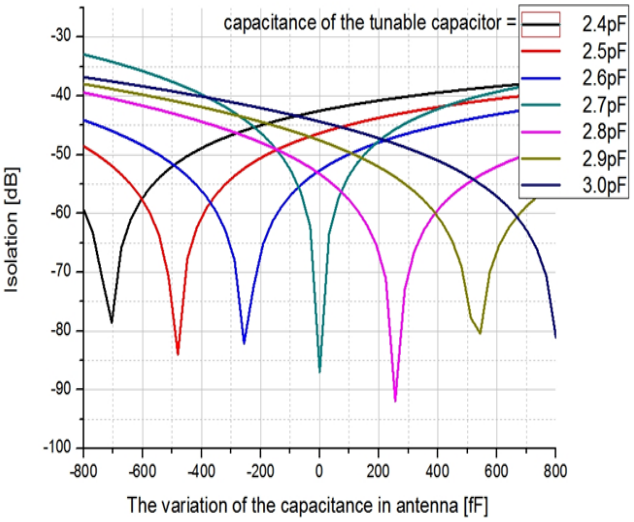

Fig. 12. Isolation by the variation of the capacitance in antenna.

The proposed in-band full duplexer has been fabricated in 65nm RFCMOS process as shown in Fig. 13. The designed chip is wire-bonded and connected on PCB to the test equipment for providing the input signal and measuring the leaked signal. The PIFA model consisting of passive elements and leakage cancellation transformer are located outside the chip and soldered on PCB as shown in Fig. 14. The designed full duplexer has been tested by varying the capacitance value of PIFA model which is chosen to be 2.7 pF initially.

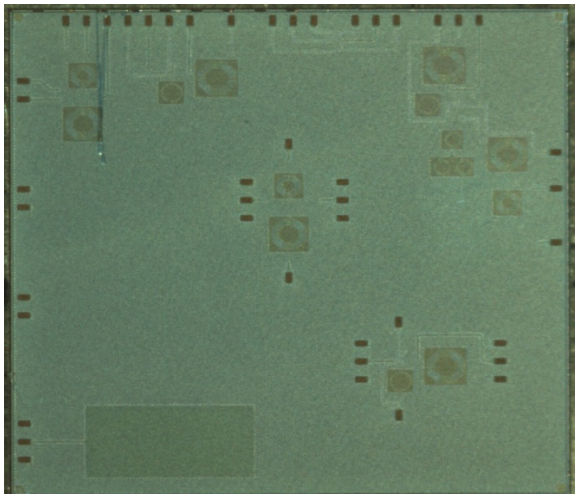

Fig. 13. The microphotograph of fabricated full duplexer.

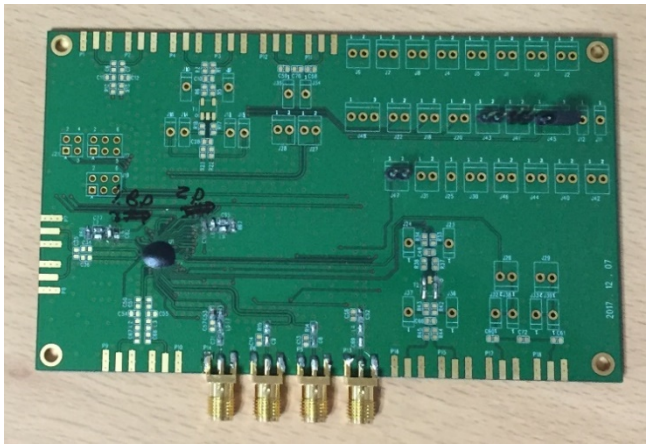

Fig. 14. The photograph of fabricated PCB.

Measured performances for insertion and return losses at the transmitter and receiver ports are illustrated along with return loss at the antenna port and isolation as shown in Fig. 15. The bandwidth of isolation with respect to over 40 dB shows 14 MHz at the center of 1.95 GHz.

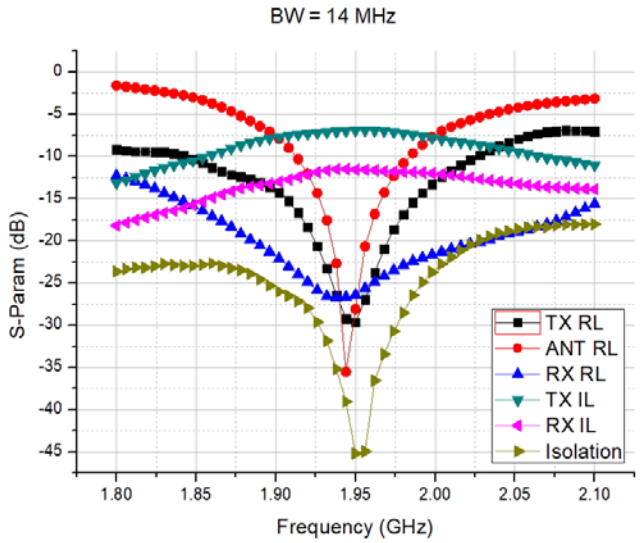

Fig. 15. Measured results for insertion loss, return loss and isolation.

III. CONCLUSION

An integrated full duplexer transceiver based on phase locked loop detects and tracks the impedance variation of the antenna and maintains and even improves isolation between the transmitter and the receiver. The TX port reflection coefficient of -29.65 dB at 1.95 GHz, the antenna port reflection coefficient of -28.09 dB, the RX port reflection coefficient of -26.41 dB, TX insertion loss of -11.58 dB, -45.2 dB the results of TX-RX isolation were obtained through measurements.

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