Calibration of Offset Voltage of Op-Amp for Bandgap Voltage Reference Using Chopping Technique and Switched-Capacitor Filter

Ji-Yong Um[a]
Department of Electronic Engineering, Hannam University
E-mail : jyum@hnu.kr

Abstract **- A calibration scheme is proposed for a bandgap voltage reference. The proposed scheme calibrates an offset voltage of operational amplifier (op-amp) of a bandgap reference which is the critical source of an output-voltage deviation of the bandgap reference. The proposed calibration is based on a chopping technique which makes an output voltage of op-amp modulate. An IIR filter is used to average out the modulated output voltage of chopped amplifier. The output voltage of IIR filter is fed into gate node of a PMOS current source which is located in the final output branch. As a result, the output reference voltage becomes insensitive to the offset voltage of op-amp. The proposed circuit was verified through Monte-Carlo simulations by using thick-oxide transistors in a 0.13-μm CMOS process. In the simulation results, the proposed calibration suppresses the deviation of output reference voltage up to 1.94 mV for the temperature range between -40ºC and 125ºC. Also, the deviation of output reference voltage is reduced by 24.5 times through proposed calibration.**

I. INTRODUCTION

A precise temperature-insensitive reference circuit is an essential building block for a variety of mixed-signal circuits and their applications. There are numerous schemes to enhance precision of reference voltage or current. Most of schemes for accurate reference voltage or current are based on trimming [1-3]. Trimming can reduce chip-to-chip variation of reference voltage or current significantly, however, it requires additional process step and time to correct chip-to-chip variations of reference voltage or current. Hence, in low-cost applications, a reference circuit without additional process step to enhance precision of reference is more preferable even though it has moderate accuracy in the reference voltage or current level.

There are several error sources in a bandgap reference circuit. Error sources that degrade the precision of a bandgap reference mainly include process variation and nonlinear temperature dependency of base-emitter voltage of diode-connected BJT, voltage difference between two diode-connected BJTs, and op-amp offset voltage [1]. Among aforementioned error sources, one of the critical error sources that degrades the precision of the bandgap reference is the offset voltage (V_{OS}) of an amplifier located in a closed loop of the reference circuit. The input-referred V_{OS} of op-amp, whose standard deviation is typically less than 10 mV, is amplified with the resistor ratio, so it is one of the critical error sources in most of the reference circuits (Fig. 1).

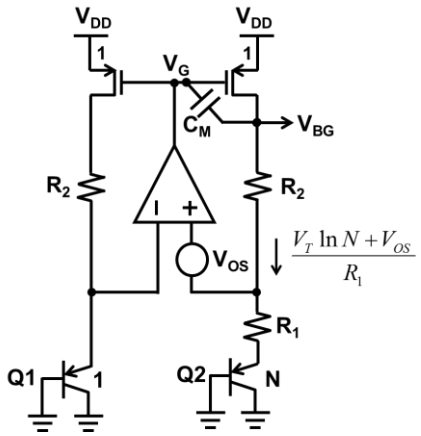


Fig. 1. Effect of offset voltage of op-amp on reference voltage.

Offset voltage of op-amp mainly depends on area of input differential pair transistors and a coefficient of variation in a utilized CMOS process [4]. One of possible solution to achieve low offset voltage is to increase chip area of op-amp, which is approximately proportional to square of required precision. Hence, in some cases, it is infeasible to achieve high precision reference voltage without additional calibration or trimming.

There are numerous counter measures for high precision performance of reference circuit in an area efficient way [5-7]. In [5], the auto-zero technique is utilized to suppress offset voltage of op-amp. However, the output voltage is discontinuous due to two-phase operation and noise performance is degraded as a result of noise folding. A

a. Corresponding author; jyum@hnu.kr

continuous reference output with reduced variation can be acquired by using chopping technique [6-7]. However, high frequency ripple due to utilization of chopper should be suppressed. Reducing this ripple to less than mV typically requires very narrow bandwidth in a filter which is located after a chopper. The narrow bandwidth means large chip area, so an area-efficient implementation method is required if chopper is utilized

In this paper, a chopping technique is applied to a CMOS bandgap voltage reference. In addition, a switched-capacitor filter, that is an IIR filter, is utilized to implement an area-efficient narrow-bandwidth low-pass filter [8]. With the use of chopping technique along with an IIR filter, a deviation of output reference voltage less than 1.94 mV for the temperature range between -40ºC and 125ºC is achieved with a small-area op-amp. The proposed calibration scheme operates in background. Hence, the proposed reference circuit with calibration scheme is considered as appropriate for low-cost application which does not require an additional process step such as trimming. Also, as an extension of [8], analysis on utilized IIR filter and simulation results are complemented.

This paper is organized as follows. Section II presents concept of calibration along with a comparison against chopping technique with a notch filter scheme in [1]. Section III describes circuit implementations and an analysis of utilized IIR filter. Simulation results and conclusions will be presented in Section IV and V, respectively.

II. CONCEPT OF CALIBRATION

A typical bandgap reference circuit is shown in Fig. 1 [4]. The output voltage of bandgap reference circuit considering input-referred offset voltage V_{OS} of op-amp is as follows.

$$V_{BG} = V_{EB2} + \left(1 + \frac{R_2}{R_1}\right)\left(V_T \ln N + V_{OS}\right) \quad (1)$$

As shown in (1), the input-referred offset voltage is amplified with a resistor ratio, and typical standard deviation of offset voltage is several mV. Hence, for applications which require moderate or high precision, offset-suppression scheme or large-sized circuit implementation is essentially necessary.

A. Chopping Technique with a Notch Filter

A work in [1] proposed a chopping technique with a notch filter to cancel out offset voltage V_{OS} of the amplifier (Fig. 2). In order to remove ripple caused by up-modulation, a notch filter is inserted between chopped amplifier and PMOS current source. The notch filter in Fig. 2(b) is implemented with two sample-and-hold circuits working in Ping-Pong mode. The sampling frequency of notch filter is chosen to be half of the chopping frequency, so that every sampling operation in the notch filter takes place at the same slope of the modulated output voltage of the amplifier as shown in Fig. 2(c).

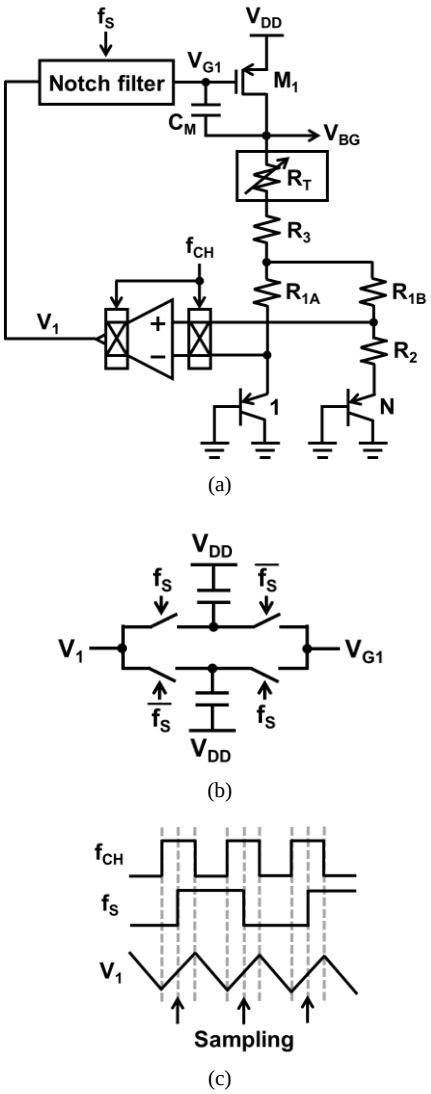


Fig. 2. (a) Bandgap reference with chopper and notch filter [1] (b) Notch filter (c) Timing diagram of notch filter

The sampled voltage is read-out and delivered to the gate node of PMOS current source M_1, as shown in Fig. 2. As a result of sample-and-hold operation of the notch filter, the band-stop frequency response at the chopping frequency is ensured. However, the reduction of chopping ripple can be sensitive to the sampling timing of the sample-and-hold circuit in the notch filter. Since the sample-and-hold circuit typically utilizes non-overlapping sampling clocks, it is not easy to make the duty cycle of the sampling clock f_S, which is shown in Fig. 2, 50%. Also, nonlinearities of capacitors in notch filter result in a DC level shift at the output of the notch filter.

In this work, in order to make the reference circuit with chopped amplifier insensitive to sampling timing of non-overlapping sampling clocks, the frequency of chopper in an amplifier is relaxed to make the modulated output voltage of op-amp settle within allocated period [8]. Then, the settled op-amp output voltage is sampled by the following IIR filter. The IIR filter continuously averages the sampled op-amp output voltage, so that the offset-averaging

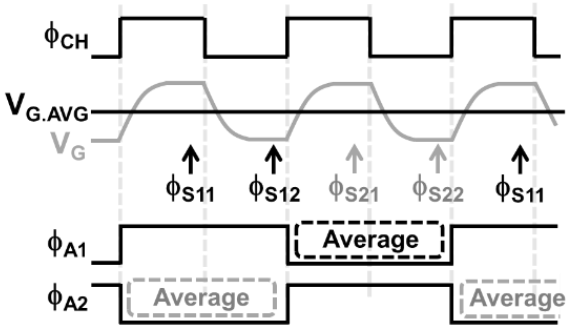


Fig. 3. Concept of proposed calibration.

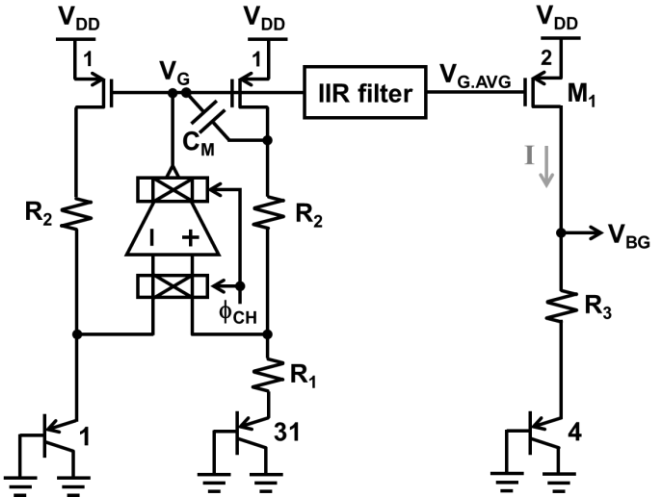


Fig. 4. Circuit implementation of bandgap voltage reference with prop osed calibration scheme.

operation becomes less-sensitive to the sampling timing of the sampling clocks of the IIR filter (Fig. 3).

B. Proposed Calibration

The proposed calibration concept can be implemented with a circuit diagram of Fig. 4. Two choppers are inserted at both of input and output of op-amp in a conventional bandgap voltage reference. As a result of chopping operation, a polarity of the input-referred offset voltage of op-amp in Fig. 4 is swapped at each phase of chopper. The swapped offset voltage V_{OS} is amplified and generated at the output of chopped amplifier. Then, the output voltage of op-amp, which is the gate-bias voltage of PMOS current sources, dithers with the chopping frequency. The modulated output voltage of op-amp can be settled, because the chopping frequency is relaxed enough. Since the average value of modulated output voltage of chopped amplifier is offset-free gate-bias voltage for PMOS current source, an IIR filter is inserted between the chopped op-amp output and the gate of PMOS current source M_1, which belongs to the final output branch. The IIR filter performs sampling operations for both phases of chopper. After completing sampling operations at both phases of chopper, the sampled voltages are averaged. The average voltage, which is the

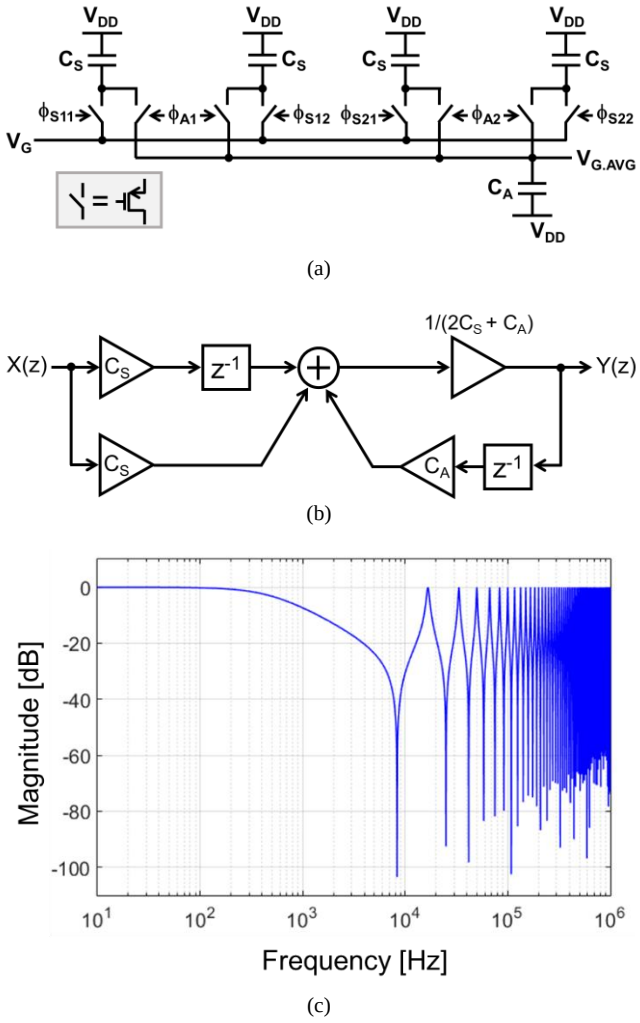


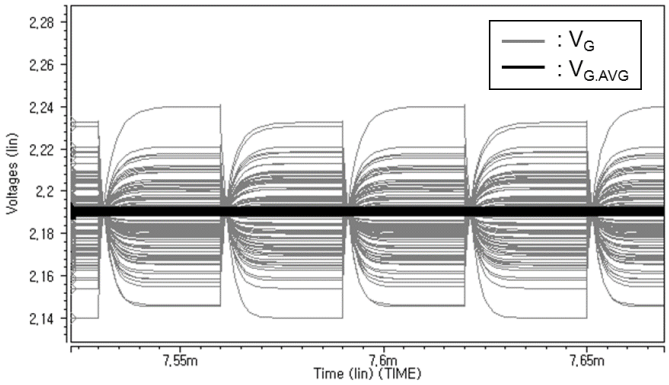
Fig. 5. IIR filter. (a) Circuit diagram (b) Linear z-domain model (c) Frequency response

gate-bias voltage of the PMOS current source M_1 is almost insensitive to offset voltage of op-amp.

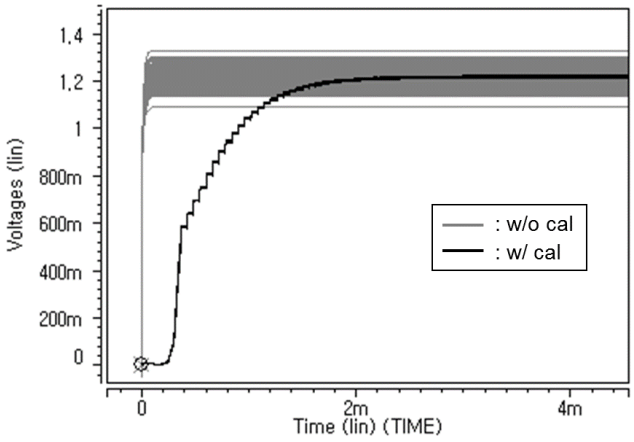
A circuit diagram of the utilized IIR filter is shown in Fig. 5(a). The IIR filter consists of two sample-and-average circuits, which operate in Ping-Pong mode, and a capacitor C_A as a memory element. During the sampling phase, each sampling capacitor C_S samples the output voltage of the chopped op-amp by using corresponding sampling clocks of ϕ_{S11} and ϕ_{S12} (ϕ_{S21} and ϕ_{S22}). During the average phase, PMOS switches, which are controlled by ϕ_{A1} (ϕ_{A2}) is connected and the charge sharing occurs. As a result, the voltage at the memory capacitor C_A is updated. When input node V_G and output node $V_{G.AVG}$ of IIR filter are denoted as $x[n]$ and $y[n]$ in discrete-time domain respectively, the relationship between $x[n]$ and $y[n]$ is expressed as

$$y[n] = \frac{1}{2C_S + C_A}\left(C_S x[n] + C_S x[n-1] + C_A y[n-1] \right) \qquad (2)$$

Also, it eventually saturates after enough time, which depends on the capacitance ratio between the sampling



(a)



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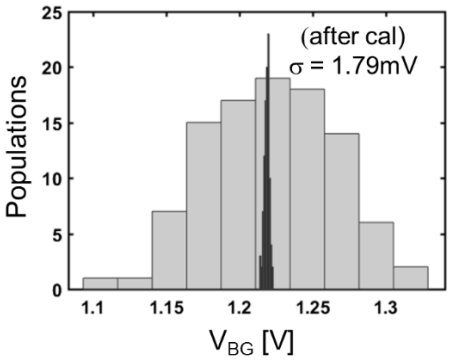


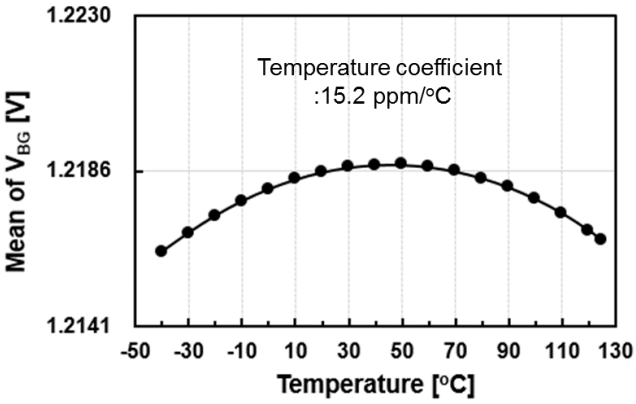
(c)

Fig. 6. Monte-Carlo simulation results with 100 iterations. (a) Wavefo rm of input and output of IIR filter (b) Waveform of reference outpu t V_{BG} depending on calibration (c) Histogram of reference output V_{BG} at temperature of 25ºC

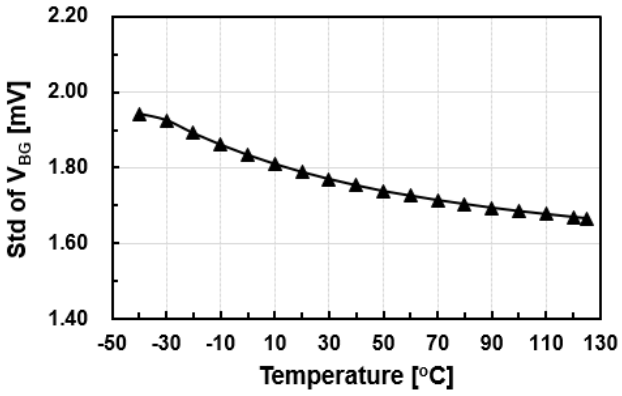
capacitor C_S and the memory capacitor C_A. The utilized capacitances of C_S and C_A are 0.2 pF and 2 pF, respectively. The IIR filter has low-pass filter characteristic with cut-off frequency of 481 Hz and notch frequencies at the odd harmonics of 8.33 kHz (Fig. 5(c)).

III. SIMULATION RESULTS

The proposed bandgap voltage reference circuit with



(a)



(b)

Fig. 7. Temperature characteristics of reference output $V_{BG.}$ (a) Mean values (b) Standard deviations

calibration scheme is simulated using thick-oxide transistors and other circuit elements in a 0.13-μm CMOS process. The PMOS current source M_1 supplies current of 2 μA at the temperature of 20ºC.

In order to verify the effectiveness of the proposed calibration, Monte-Carlo simulations are performed with variations of the threshold voltage V_{TH}. A deviation of threshold voltage of MOS transistor can be characterized as follows.

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{3}$$

A_{VTH} in (3) is a proportionality factor and it determines a degree of mismatch of threshold voltage of CMOS process. The utilized values of A_{VTH} for NMOS and PMOS in this simulation are 7.9 mV·μm and 4.2 mV·μm, respectively.

The voltage waveforms at both input and output of the IIR filter acquired from Monte-Carlo simulation are shown in Fig. 6(a). A peak-to-peak value of the modulated output voltage of op-amp and the output voltage of the IIR filter are 94.0 mV and 3.72 mV, respectively. As a result of the averaging operation of the IIR filter, the output voltage of the IIR filter is located at the cross point of the dithering

TABLE I
PERFORMANCE COMPARISON OF CORRECTED (CALIBRATED OR TRIMMED) VOLTAGE REFERENCES

		JSSC'11 [1]	ESSCIRC'11 [9]	JSSC'12 [10]	**This work**
Technology (CMOS)		0.16 μm	0.13 μm	0.13 μm	**0.13 μm**
Supply voltage		1.8 V	0.75-1.7 V	0.5-3.0V	**2.8 V**
Bandgap voltage		1.088 V	256 mV	174.9-178.7mV	**1.219 V**
Inaccuracy	w/o correction	±0.75 % (3σ)	±1.5 % (5σ)	±2.16 % *(3σ)	**±12.4 % (3σ)**
	w/ correction	±0.15 % (3σ)	±0.5 % (5σ)	±0.55 % **(3σ)	**±0.48 % (3σ)**
	Temp. range	-40 to 125 ºC	-20 to 85ºC	-20 to 80ºC	**-40 to 125 ºC**
Temperature drift		5-12 ppm/ºC (61 samples)	40 ppm/ºC (N.A.)	5-47 ppm/ºC (25 samples)**	**13-22 ppm/ºC (100 samples)*** **
Active area		0.12 mm^2	0.07 mm^2	0.0093 mm^2	**N.A.**
Power consumption		99 μW	173 nW	29.5 pW	**53 μW**
Correction	Calibration	Background	None	None	**Background**
	One-point trim.	O	O	O**	**X**

*49 samples from two separate fabrication runs ** trimmed result from other fabrication run *** Monte-Carlo simulation

output voltage of op-amp. The simulated waveform of output voltage V_{BG} of bandgap voltage reference is shown in Fig. 6(b). After calibration, the standard deviation of the output voltage V_{BG} becomes 1.79 mV at the temperature of 20ºC. This shows that the proposed calibration suppresses the standard deviation of output reference voltage V_{BG} by 24.5 times. Since the simulated standard deviation of the input-referred offset voltage of op-amp is 6.10 mV, the estimated standard deviation of the output voltage V_{BG} due to offset voltage of op-amp is 43.8 mV according to the following equation

$$\Delta V_{BG} = \frac{2V_T}{I \cdot R_1} V_{OS} + \frac{2R_3}{R_1} V_{OS} \quad (4)$$

The first term in (4) is derived from the emitter-base junction voltage of PNP transistor at the output current branch, and the second term in (4) stems from the voltage drop across resistor R_3.

Other contributions in the standard deviation of the output voltage V_{BG} mainly come from current mismatch between PMOS current sources, because the current mismatch between PMOS current sources is not modulated by chopper. The current mismatch is determined by the following equation.

$$\sigma^2\left(\frac{\Delta I}{I}\right) \cong \frac{4A_{VTH}}{W \cdot L \cdot (V_{GS} - V_{TH})^2} \quad (5)$$

where A_{VTH} is proportionality factor. In order to minimize the current mismatch between PMOS current sources, large-area PMOS current sources are simply utilized. The aspect ratio (W/L) of PMOS current source M_1 is 20.8/32. Meanwhile, transistors in op-amp have relatively small area, and have the same length of 0.7 μm.

The simulated mean and standard deviation values of the output voltage V_{BG} for the temperature range between -40ºC and 125ºC is shown in Fig. 4. The mean-value plot of output voltage V_{BG} shows a bell-shape curve, which is a typical temperature characteristic of the conventional bandgap voltage reference. The standard deviation values of V_{BG} is less than 1.94 mV for all temperature ranges and decreases as temperature increases. As mentioned in the previous discussion, the residual deviation of V_{BG} is mainly caused by current mismatch of PMOS current source. The current of the PMOS current sources in Fig. 4 have proportional-to-absolute-temperature (PTAT) characteristic, so the overdrive voltage of PMOS transistors increases as the temperature increases. According to (5), the current mismatch amount of transistor decreases when the overdrive voltage of transistor increases. Hence, the deviation of V_{BG} in this work exhibits negative temperature coefficient as shown in Fig. 7(b).

Performance of proposed reference circuit is compared with results of other publications [1, 9, 10]. A one-point trimming is widely used in a voltage reference circuit if high precision performance is necessary. Works reported in [1, 9, 10] also utilize a one-point trimming at one specific temperature. By means of trimming, works in [1, 9, 10] achieve σ/μ less than ±0.55% with a probability of 99.7%. Unlike other works of [1, 9, 10], this work does not rely on trimming for improvement of accuracy. By using background calibration based on choppers with an IIR filter, this work achieves an output-voltage deviation σ/μ of ±0.48% with a probability of 99.7%. Since this work achieves moderate precision performance without a trimming process, it is appropriate for low cost applications.

IV. CONCLUSION

A calibration of bandgap voltage reference is presented. The proposed calibration utilizes the chopping technique to modulate the input-referred offset voltage of

op-amp, which is the main source of reference voltage deviation. By applying choppers at both input and output of op-amp within the closed loop of the bandgap voltage reference, the bias voltage of PMOS current source is modulated. The chopping frequency is relaxed, so that the modulated bias voltage can be settled sufficiently. The average value of the modulated bias voltage is acquired by using IIR filter. The IIR filter performs sampling operations at both chopper phases. Since the IIR filter samples the sufficiently settled output voltage of op-amp, the averaging operation of IIR filter is less-sensitive to the rising or falling instances of the sampling clocks. The output voltage of IIR filter, which is insensitive to offset voltage of op-amp, is fed into the gate of the PMOS current source of the final output branch. The IIR filter consists of two sample-and-average circuits, which operate in Ping-Pong mode, and the memory capacitor for continuous averaging operation. The proposed calibration of reference circuit is verified through Monte-Carlo simulations. The simulation results show that the proposed calibration suppresses the standard deviation of output reference voltage up to 1.94 mV for the temperature range between -40ºC and 125ºC. Since the proposed calibration does not require an additional process step such as trimming for reduction of reference-voltage deviation, it is suitable for low-cost applications which accept a moderate deviation in the reference level.

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Ji-Yong Um received the B.S., M.S. and Ph.D. degrees in Electronic and Electrical Engineering from Pohang University of Science and Technology (POSTECH), Kyungbuk, Korea, in 2006, 2008 and 2013, respectively.

From 2014-2015, he was a Senior Engineer at CMOS Image Sensor (CIS) Division of SK Hynix. In 2016, he joined the faculty of the Department of Electronic Engineering at Hannam University, where he is currently an Assistant Professor. His research interests include analog/digital beamformer circuits for ultrasound medical imaging, data converters, and high-precision techniques using calibration.

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