The ROIC design for distance image measurement

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***Abstract* - In this work, 4-to-1 combined pixel array for front-end readout integrated circuit of laser radar is developed in SK Hynix 0.18 μm CMOS technology. As a mixed circuit type, 4-to-1 combined unit pixel consists of 4-to-1 transimpedance combining amplifier, comparator and time-to-voltage converter with control logic blocks. Here, 8 × 8 combined pixel array is implemented and tested for 3-demensional (3-D) range detection. The power for the array is supplied from 1.8 V supply and the bandwidth is under 1 GHz.**

I. INTRODUCTION

Laser detection and ranging (LADAR) sensors have been commonly used to acquire the real time three-dimensional (3-D) images using time-of-flight (TOF) of a short laser pulse. LADAR technology has the potential to get the 3-D images of the fast moving target, it has been deployed in many application, such as, reconnaissance, autonomous vehicles and robots, remote sensing, terrain visualization, non-contact motion recognition, surface mapping for buildings and scenes where high 3-D resolution is of prime importance [1]-[6]. For the high precision 3-D image acquisition, pulsed time-of-flight (TOF) LADAR is widely used to measure distances compare to other measurement methods such as the continuous-wave optical phase method [7], [8].

There are different operation methods of pulsed LADAR systems with varying scanning mechanisms, number of lasers, and geometric configurations. Especially, 3-D flash LADAR can provides a unique advantage of a flash image which means that it can detect the 3-D image of a very fast object. 3-D flash LADAR obtains an entire frame of 3-D data with a single short laser pulse and a focal plane array (FPA) of the photodetectors and front-end readout integrated circuits (ROICs), similar to 2-D FPAs that are common in digital cameras today. Fig. 1 illustrates the 3-D FPA.

Every photodetector and its corresponding front-end readout circuits within a pixel need to be operated independently. The size of one pixel should be reduced around <100 μm for a higher 3-D resolution and the used pulse width is normally <10 ns. However, to enhance the pixel sensitivity, the effective pixel size should be increased. In this case, the parasitic capacitance by larger photodetector arealimits the bandwidth of the ROIC.

In this work, to improve the sensitivity without bandwidth limitation of the front-end ROIC, the 4-to-1 combined pixel is used to consist of FPA providing a small area to fit within the 100 μm × 100 μm. The 8 × 8 combined pixel array is implemented in SK Hynix 0.18 μm CMOS technology.

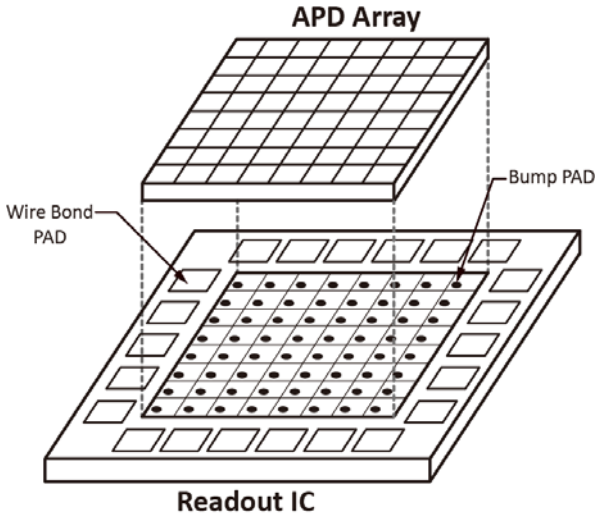

Fig. 1. 3D FPA Design.

II. EXPERIMENTS

A. 4-to-1 combined pixel architecture

A 4-to-1 combined pixel has four small photosensitive cells. This pixel combines every photocurrent from each cell into a single signal. From this technique, the effective active area is maintained but the parasitic capacitance of photodiode is lower to release the bandwidth limitation.

The 4-to-1 combined pixel for front-end ROIC of laser radar consist of three parts, such as 4-to-1 transimpedance combining amplifier (TCA), comparator, and time-to-voltage converter (T2V) with control logic block, as shown in Fig. 2.

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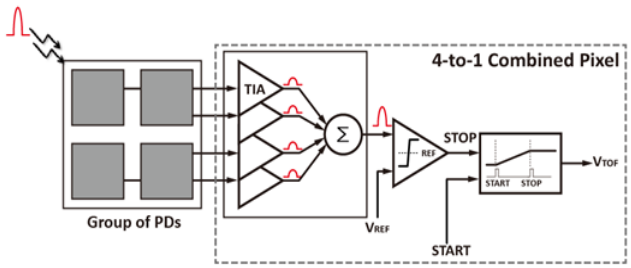

Fig. 2. 4-to-1 combined pixel architecture.

The developed 4-to-1 TCA is used to amplify and combine current signals, converted from incoming optical signals by the photosensitive cells, to one voltage signals for further processing. A comparator compares the signal with threshold voltage. In LADAR front-end circuit, it is used to produces a timed logic pulse that indicates the arrival of the return signal. The T2V converts the time between START and STOP into voltage, proportionally. It is able to measure time intervals over a linear range.

B. 4-to-1 combined pixel array architecture

Architecture of 8×8 pixel array with 4-to-1 combined pixels is illustrated in Fig. 3.

In this work, the readout circuitry, which consists of an 8-channel decoder for row selection, 8-to-1 multiplexer for column selection, and output buffer for output impedance matching to 50 Ω, is additionally designed to readout the stored range information in every pixel.

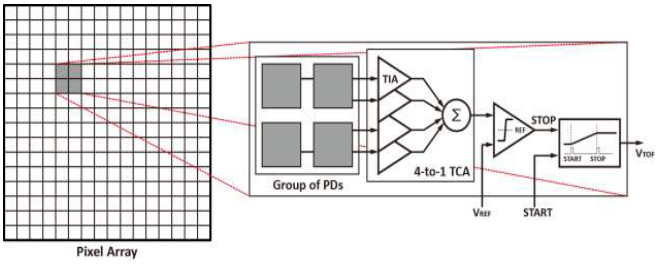

Fig. 3. Architecture of 8×8 pixel array with 4-to-1 combined pixels.

C. 4-to-1 combined pixel array specifications

In this work, 8 × 8 combined pixel array is implemented and tested 3-D range detection. The specifications of pixel array are summarized in Table I. The considered parameters for designing the 4-to-1 combined pixel are transimpedance gain and bandwidth of TCA, hysteresis of comparator, and maximum detectable range of T2V.

By implementing and testing this array, the specification of the combined pixel is optimized, and then the combined pixel is possible to enlarge to 2-D combined pixel array for FPA with more pixels.

D. Cad tools

The proposed chip is designed and verified as fully customized mixed circuit with Calibre and Assura. EM simulation tools, such as ADS or Sonnet, are used with necessity. PCB test fixture to measure the pixel performance is designed with ADS.

TABLE I.
Design specification of the proposed combined pixel array

Parameter	Target
Array	8 × 8
Gain [dBΩ]	75
Bandwidth [MHz]	500
Hysteresis [mV]	20
Max. Range [m]	5

E. Design size

The proposed chip size including I/O pads is 3.8 mm × 3.8 mm, and the combined pixel array occupies an active area of 800 μm × 800 μm, as shown in Fig. 4.

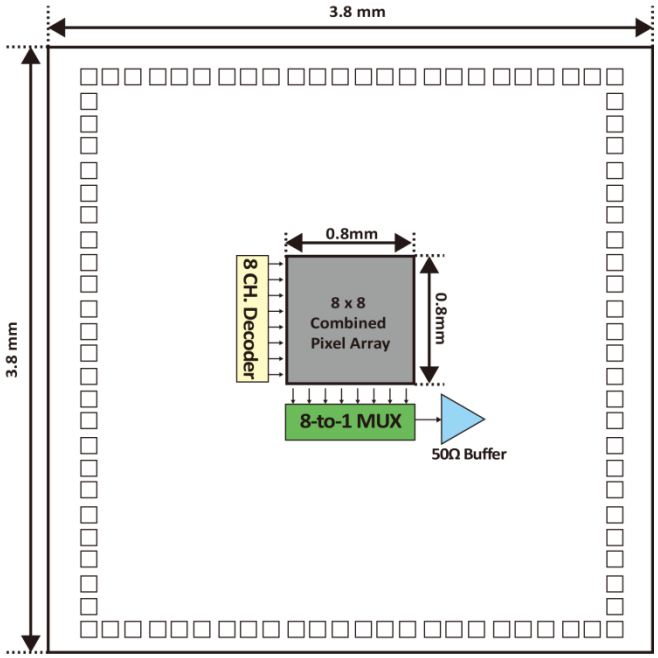

Fig. 4. Chip size.

F. Chip test plan

To test the fabricated chip, this will be mounted on the FR-4 PCB test fixture. Input signals are induced by pulse pattern generate, electrically. All biases were applied through bond wires, and short pulse response measurement was performed with CMJ connector. The output voltage according to the TOF and input amplitude is being measured by using the oscilloscope. Fig. 5 shows the measurement setup for the fabricated chip. The signals which involved in the designed array operation are going to be generated from an external control board with a FPGA.

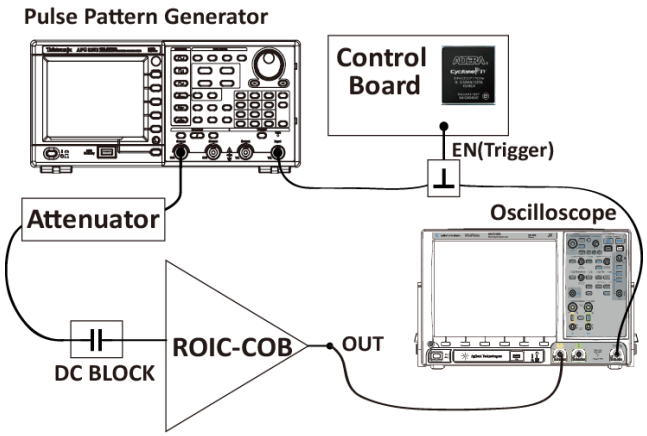

Fig. 5. Setup for fabricated chip test.

III. Results and Discussion

The schematic and the simulated results for the designed circuits consisted in the 4-to-1 combined pixel are presented.

A. 4-to-1 TCA

The 4-to-1 TCA amplifies and combines the photocurrent from the four partitioned photodetector cells to one voltage signal. Four independent regulated-cascode (RGC) trans-impedance amplifiers (TIA) [9] as a low impedance input stage to amplify the received optical current from each photodetector cell, a signal combiner to sum all the outputs of each TIA. The schematic for the 4-to-1 TCA is shown in Fig. 6.

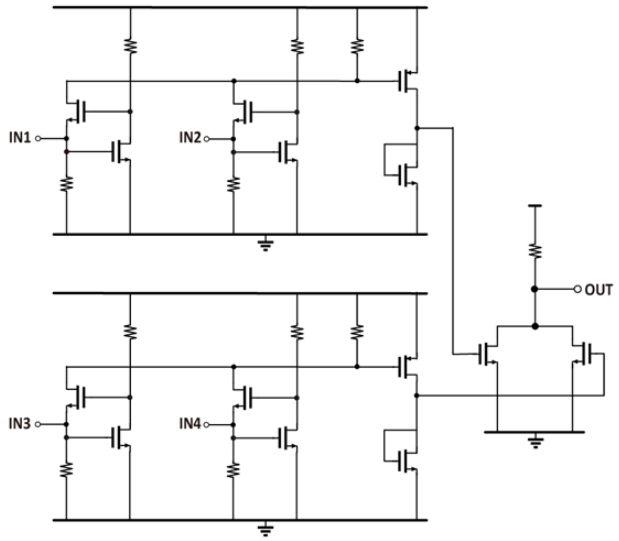

Fig. 6. 4-to-1 TCA schematic.

Fig. 7 and Fig. 8 show the ac and transient simulation results, respectively. The transimpedance gain of TCA is about 84 dBΩ and the bandwidth is about 733 MHz. The input pulse used in simulation has rising and falling time of 1.8 ns and the pulse width is 3.8 ns. The linear range is up to 35 uA of input pulse amplitude, approximately.

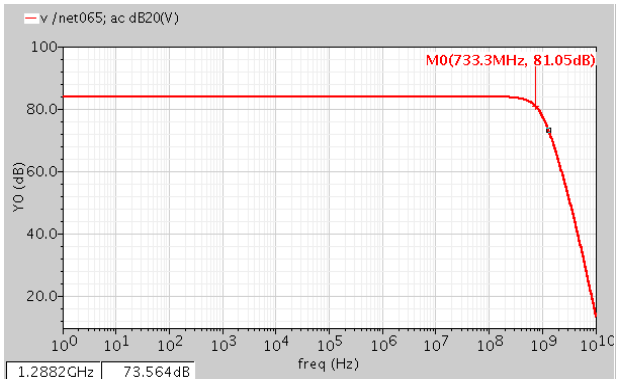

Fig. 7. AC simulation result for the 4-to-1 TCA

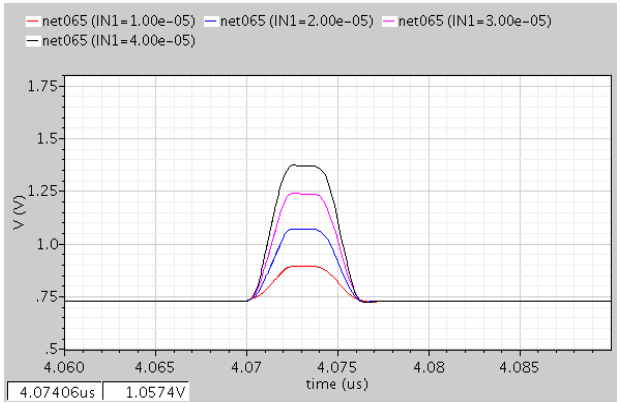

Fig. 8. Transient simulation result for the 4-to-1 TCA

B. Comparator

A comparator compares the signal with threshold voltage. In LADAR front-end circuit, it is used to produces a timed logic pulse that indicates the arrival of the return signal. The comparator schematic is depicted in Fig. 9.

Fig. 10 shows the simulated hysteresis results for the designed comparator. The hysteresis voltage is about 20 mV. Fig. 11 shows the simulated transient response according to the input pulse amplitude. With the designed TCA as a preamplifier, the designed comparator is detectable from 3 uA of input amplitude. In linear operation range, the work error is about 2.4 ns, which is corresponding 36 cm.

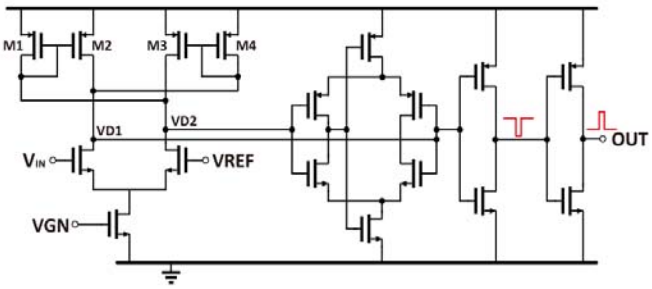

Fig. 9. Comparator schematic.

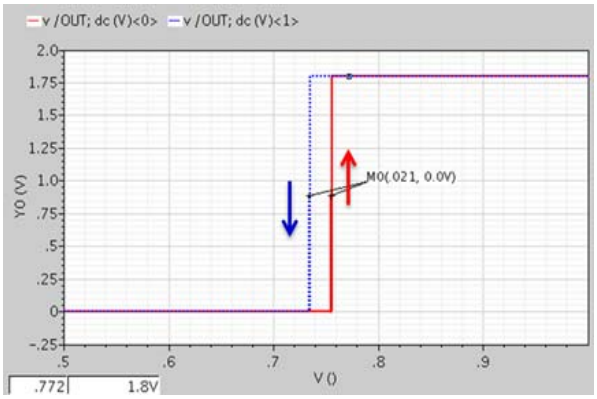

Fig. 10. Hysteresis simulation result for the comparator

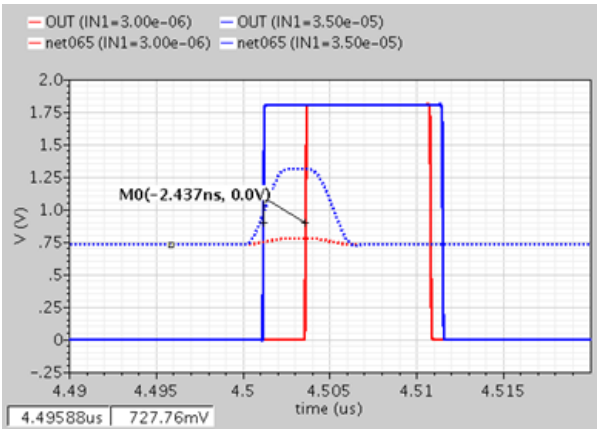

Fig. 11. Transient simulation result for the comparator according to the amplitude of the input voltage pulse.

C. Time-to-voltage converter (T2V)

The T2V converts the time between START and STOP into voltage, proportionally. It is able to measure time intervals over a linear range of 15 ns to 70 ns. The range is adjustable to longer intervals with a corresponding loss in accuracy [10]. The schematic for the T2V is shown in Fig. 12.

The simulated output voltage according to the TOF for the designed T2V is shown in Fig. 13. The TOF is from 15 ns to 70 ns.

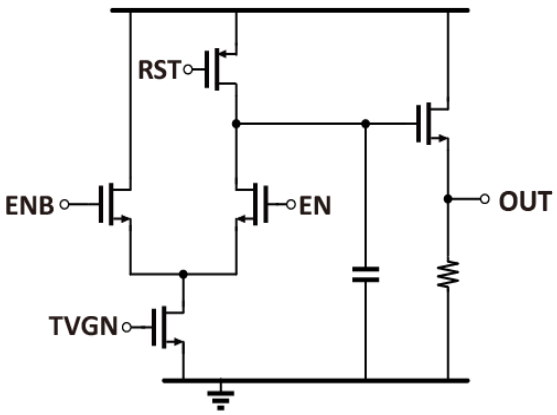

Fig. 12. T2V schematic.

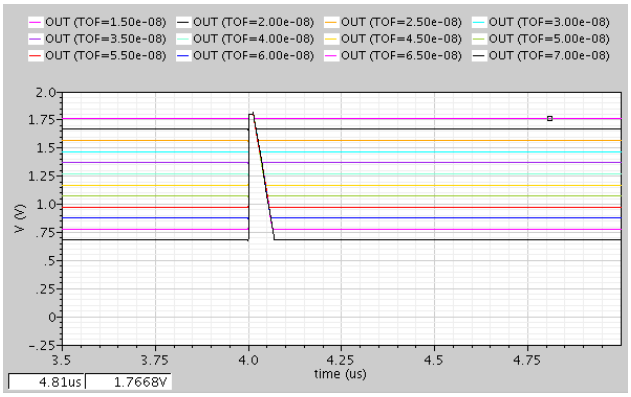

Fig. 13. Simulation result for T2V according to TOF

D. Readout from 8 × 8 array

The simulated result from each pixel is shown in Fig. 14. Each pixel in a column has input pulse with different TOF. The TOF is from 15 ns to 85 ns.

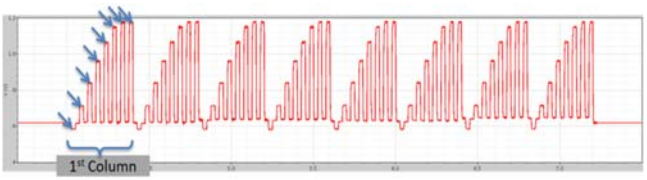

Fig. 14. Simulation result for T2V according to TOF from 8 × 8 array

E. Measurement Result

Figure 15 is a microphotograph of the designed combined pixel array. The signal was applied as a bond wire.

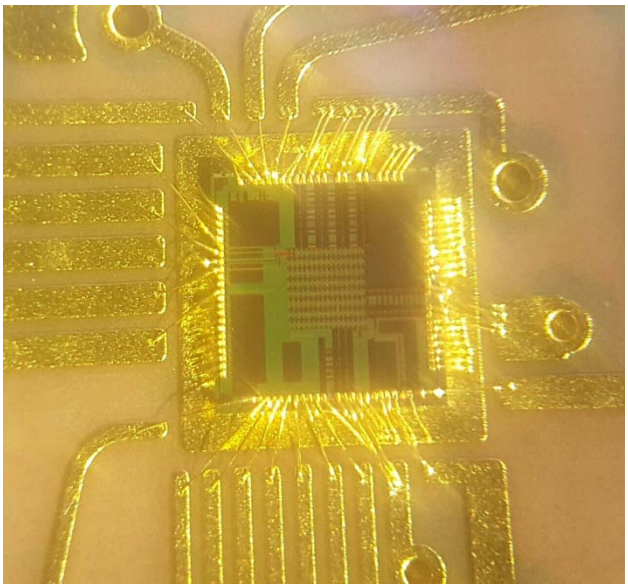

Fig. 15. Microphotograph of a designed 8 x 8 combined pixel array

Figure 16 shows the actual chip measurement setup. Various digital block signals were applied by FPGA board and DC voltage was applied by power supply. The output signal of the combined pixel array was measured with an oscilloscope.

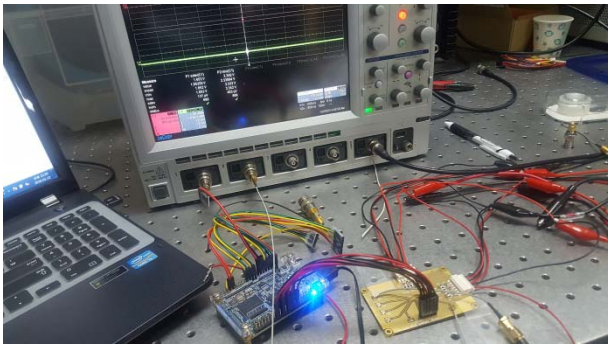

Fig. 16. Setup for fabricated chip test.

The measurement setup desired in Table 2 was set to be almost the same as the simulation condition.

TABLE II.
Design specification of the proposed combined pixel array

Parameter	Simulation	Measurement
VDDA [V]	1.8	1.792
VDDD [V]	1.8	1.8
VDDB [V]	1.8	1.8
VREF [V]	1.09	1.1
CVGN [mV]	740	809
TVGN [mV]	540	540

Figure 17 shows measured results of the designed pixel array. Enable signal (Yellow) goes low and read starts. Originally, we had to read all 64 pixels, but the pixel array designed has pixels that are not measured because of poor pixel variation. Therefore, pixel variation needs to be improved.

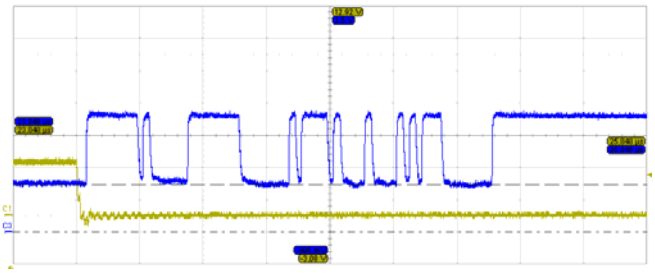

Fig. 17. Measurement result for 8 × 8 pixel array

Figure 18 is a graph of the voltage level linearity with respect to the TOF of the pixel array. It can be seen that the graph is fairly linear from 0 ns to 250 ns.

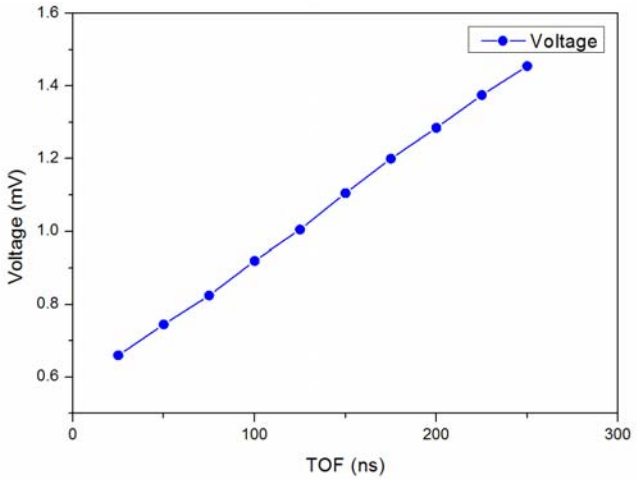

Fig. 18. Measurement result for T2V according to TOF from 8 × 8 array

IV. CONCLUSIONS

In this work, the 4-to-1 combined pixel array was proposed to enhance the sensitivity and bandwidth for optical sensor. However, it is necessary to improve the pixel variation. The 4-to-1 combined pixel array is possible to apply for the direct-ToF-based high-sensitive 3-D range image sensor for non-contact motion recognition, autonomous vehicle, and 3-D scanner and printer.

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