

A low noise Hall Effect Sensor Readout Circuit

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Abstract – In this paper, the structure, operation principles, and characteristics of the hall sensor using semiconductors are discussed through the hall sensor design. The CMOS hall sensor is composed of a CMOS hall plate and Readout Integrated Circuit (ROIC) which processes the signal of the hall plate. For this sensor, a detailed ROIC design is required due to the small output signal of the hall plate. The ROIC consists of the part related to current spinning with chopping and Instrumentation Amplifier (IA). In this circuit, the offset and 1/f noise of the magnetic signal are separated by the current spinning frequency of 100 kHz and the noise of amplifier is removed by chopping. The IA has high input impedance, low offset and large Common Mode Rejection Ratio (CMRR). Also, the de-chopping is placed inside the IA which can be designed with op amp that has low slew rate and narrow bandwidth. The designed ROIC has the difference 43dB gain between noise gain and signal gain. The signal gain is 64dB. The proposed hall sensor operates as a switch at 0~20mT magnetic field in 10 kHz with 1mA bias current. It has been integrated in a standard 0.18um CMOS technology.

Keywords—Hall effect sensor, Magnetic sensor, ROIC

I. INTRODUCTION

The interest in magnetic sensors has significantly increased in recent years because of its attractive and applicable advantages in various ways. The magnetic sensor that converts magnetic field into electrical signal is widely used in various fields. Magnetic sensors are frequently applied not only for automotive industry and compass applications but also in a large variety of biomedical systems. The Hall Effect is a typical phenomenon that is occurred in magnetic sensors. Hall Effect magnetic sensor is the base of highly developed and important industrial activities. It is commonly used as a key element in contactless sensors for linear position, angular position, velocity, rotation, electrical current, and so on [1]. The basic principle of the Hall Effect is shown in Fig. 1.

When the magnetic field is placed perpendicular to the conductor where a current is passed, the voltage is generated,

perpendicular to both the current and the magnetic field. This effect is known as Hall effect, and the generated voltage is called Hall voltage. Therefore, the hall voltage of a hall plate may be regarded as a signal carrying information. If we know the material properties, device geometry and biasing conditions, the hall voltage can give us information about the magnetic induction B [2]. The Hall plate that senses magnetic field is produced by bipolar or CMOS process [3]. The CMOS Hall plate is small size and low cost but it has low sensitivity and offset on process variation. Therefore, effective hall plate and low noise readout circuit are required [4]. The cross shape of hall plate effectively reduces offset of hall plate, and the combination of chopping and current spinning technique can reduce offset and 1/f noise [5]. Generally, hall effect sensors are composed of the hall plate to generate hall voltage and ROIC [6]. The integrated hall sensor block diagram is shown in the Fig. 2.

In this paper, a hall sensor is designed to have readout circuit applying current spinning and chopping technique. In the section A and B of chapter II, the cross shape hall plate structure with high sensitivity is described and the hall plate equivalent circuit for signal processing circuit design is modeled. In section C, the signal processing circuit is designed with the proposed hall plate and the principles of the combination of chopping and current spinning technique for low noise, as well as IA designs are illustrated. Since the operation error occurs in the ROIC due to the bandwidth limitation of the IA, the designed model has a de-chopping

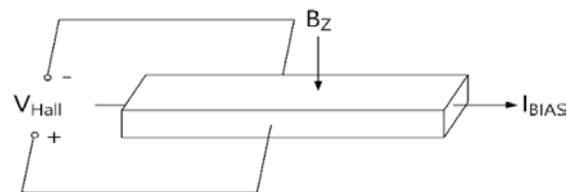


Fig. 1. The basic principle of the Hall Effect

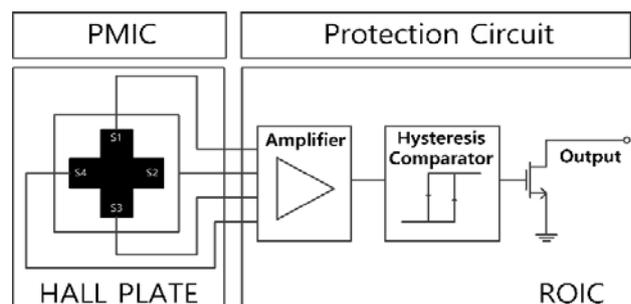


Fig. 2. The integrated Hall sensor block diagram

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structure in the middle of the measurement amplifier to solve this error. The simulation of the designed Hall sensor is presented in Section D. Related results and discussion of the manufactured Hall sensor test are shown in Chapter III. Finally, the conclusion is drawn in chapter IV.

II. MAIN SUBJECT

A. Hall plates

Hall sensor has two different modes and it is called ‘Current mode’ when current is outputted and ‘Voltage mode’ when voltage is outputted. In voltage mode, current or voltage can be received by the bias input. These are referred to as ‘Current-related voltage mode’ and ‘Voltage-related voltage mode’, respectively. One of the most important characteristic is magnetic sensitivity and the equations to calculate absolute sensitivity S_A for each mode are shown as eq. (1-a) and eq. (1-b).

$$\text{Voltage-related } S_A = \frac{V_{Hall}}{B} \text{ [V/T]} \quad (1-a)$$

$$\text{Current-related } S_A = \frac{I_{Hall}}{B} \text{ [A/T]} \quad (1-b)$$

V_{Hall} and I_{Hall} mean Hall voltage and Hall current respectively. Relative magnetic sensitivity depending on the operating mode of the sensor is shown in TABLE I [7].

TABLE I
Sensitivity of Hall magnetic sensors in voltage-mode and current-mode condition

Mode	Sensitivity	Unit
Current-Biased Voltage-Mode	$S_A = \frac{S_{Hall}}{I_{bias} \times B}$	[V/AT]
Voltage-Biased Voltage-Mode	$S_A = \frac{S_{Hall}}{V_{bias} \times B}$	[V/VT=T]
Current-Mode	$S_A = \frac{I_{Hall}}{I_{bias} \times B}$	[A/AT=T]

Hall plates are classified into three types according to the shape of the sample. First type is when its length L is infinite, second type is when it is a rectangle, and the third is the cross shape device. Three types of hall plates are shown in Fig. 3.

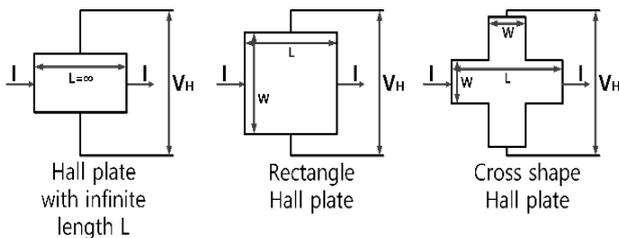


Fig. 3. Types of hall plates

In the case of a Hall plate with infinite length L, the Hall voltage is eq. (2).

$$V_{Hall} = \frac{1}{qnt} I_{Bias} B \quad (2)$$

Where q denotes the magnitude of the electron charge, n is the carrier concentration in the plate and t is the plate thickness. However, the Hall voltage of rectangle Hall plate and cross shape Hall plate is eq. (3).

$$V_{Hall} = \frac{G}{qnt} I_{Bias} B \quad (3)$$

G denotes the geometrical correction factor of Hall voltage. For an ideal Hall sensor with a very long rectangular shape, G=1. In case of the cross shape Hall plate, G can be formulated as eq. (4) and the value of G is less than 1(G<1) meaning that Hall voltage is smaller than the ideal case.

$$G = 1 - 5.0267 \frac{\theta_H}{\tan(\theta_H)} e^{-\frac{\pi W + 2L}{2W}} \quad (4)$$

The cross shaped Hall plate is a geometry with low offset noise and high sensitivity [8]. CMOS Hall plate is composed of N-well active region, P+ layer and N+ contacts. P+ layer covers the surface of active area to decrease the flicker noise and N+ contacts use to reduce contact resistances. The cross shaped Hall plate cross section is shown in Fig. 4.

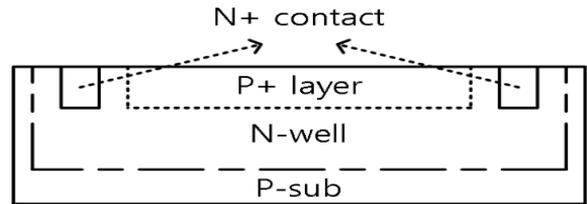


Fig. 4. The cross shaped Hall plate cross section

The cross shaped Hall plate has been modeled in using the Verilog-A language as shown in Fig. 5. in order to easily simulate [7].

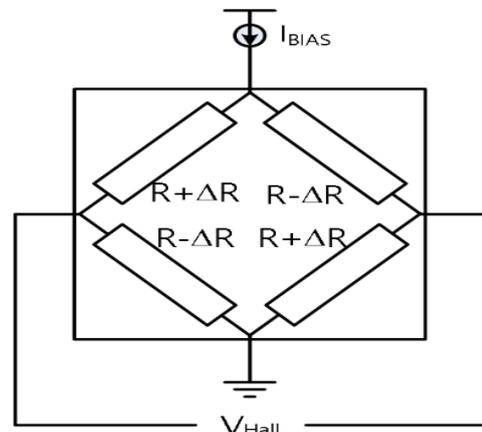


Fig. 5. Bridge circuit model of Hall plate using Verilog-A

B. Hall plate optimal size tracking

G in eq. (4) is proportional to length and inversely proportional to width. The longer the length, the more Hall plate is identical to the ideal shape of very long rectangle. So, this equation (G) converge to 1 and it is shown as a graph in Fig. 6.

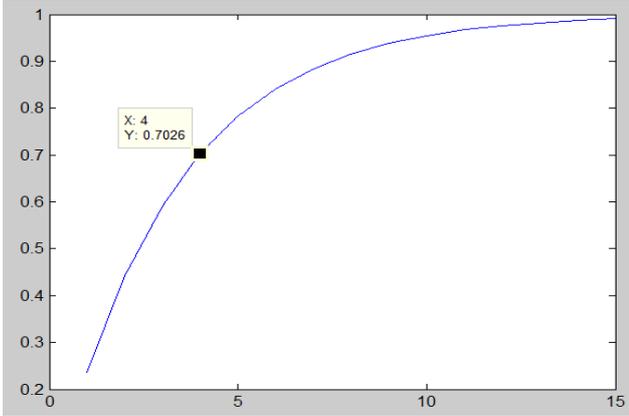


Fig. 6. Geometry correction factor according to length

The relation between the voltage related voltage mode and the current related voltage mode is formulated in eq. (5) [9].

$$S_V = \frac{S_I}{R_S N_S} \cong \frac{G}{2 \frac{L}{W} + \frac{2}{3}} \mu_H \quad (5)$$

This equation is shown as a graph in Fig. 7.

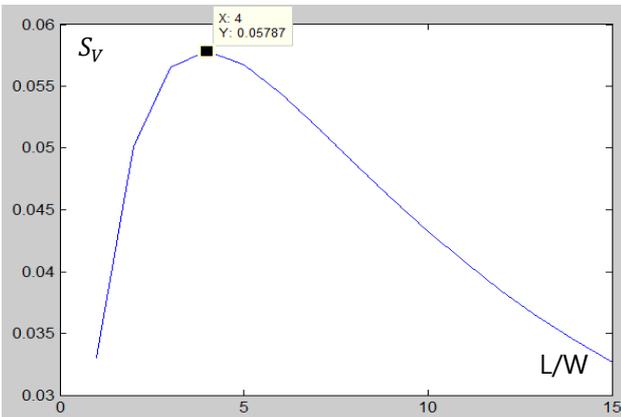


Fig. 7. Voltage related efficiency per width over length ratio of the sensor's arms.

As shown in Fig. 7., when the ratio of L/W is 0.4, the value of the sensitivity reaches its maximum. Therefore, the cross shape Hall plate width and length are designed as 10um and 4um respectively. Sheet resistance is shown in eq. (6). This value is given in the process and is 940 ohms.

$$R_S = \frac{1}{q \mu N t} \quad (6)$$

C. Readout circuit

According to materials, the electron mobility varies, and silicon's electron mobility is relatively low. It leads to low sensitivity of Hall plate and low output signal of Hall plate. In addition, due to the asymmetry of the process variables, offset and 1/f noise occur in the output signal. Therefore, noise must be suppressed. The combination of chopping and current spinning technique allows to dramatically reduce noises of Hall plate. The detailed noise reduction principle using chopping and current spinning technique is visualized in Fig. 8.

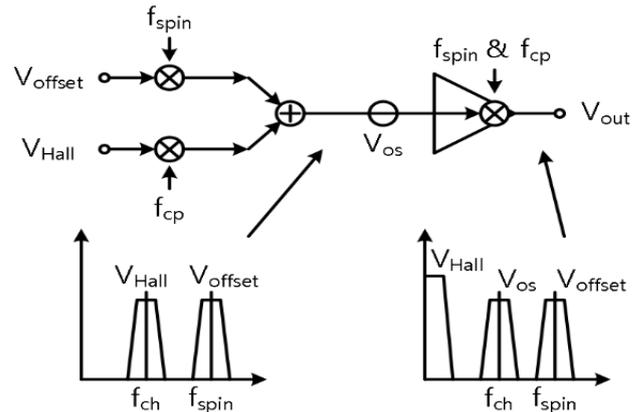


Fig. 8. The noise reduction principle using chopping and current spinning technique

The magnetic signal and the noise of Hall plate are divided by current switching frequency. The magnetic signal is moved to the chopping frequency and the noise is moved to the DC frequency band. The magnetic signal and the noise are divided through that the magnetic signal is moved to the DC frequency band by the de-chopping.

The Hall plate is a resistive sensor which has high output impedance. The resistive sensor also requires fully differential amplifiers due to its different output. More specifically, low noise amplifier is needed because the output signal of the Hall plate is very low and has unnecessary noise. Using the fully differential amplifier as close loop is not suitable to amplify the plate signal because the input impedance is low. Therefore, instrumentation amplifier is chosen to amplify signal of Hall plate because it has high input impedance, low offset and large CMRR. However, since IA does not have wide bandwidth, putting de-chopping after normal IA is problematic due to the amplified swing range of the input signal. The amplified swing range of the input signal appears as chopping ripple. The principle of chopping ripple is shown in Fig. 9 [10].

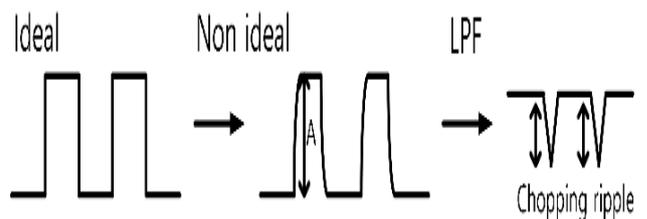


Fig. 9. The principle of chopping ripple

The amplified signal signifies that the amount of change dV of the signal becomes large. When amplifying dV is increased by the gain of instrumentation amplifier. So, the more current needs by eq. (7).

$$C \frac{dV}{dt} = I \quad (7)$$

Thus, chopping of the amplified signal has large chopping ripple. High slew rate and wide bandwidth are required to reduce the chopping ripple. The designed Hall sensor has de-chopping inside the IA. It decreases the necessary slew rate and bandwidth to reduce the chopping ripple than conventional IA. The structure of De-chopping is illustrated in Fig. 10.

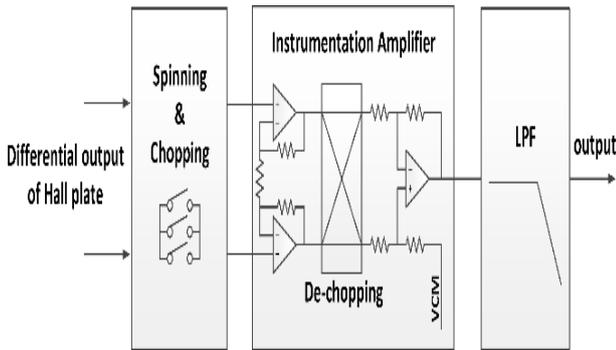


Fig. 10. De-chopping inside the instrumentation amplifier

In this circuit, the offset and $1/f$ noise of the magnetic signal are separated by the current spinning frequency of 100kHz and the noise of amplifier is removed by chopping of 200kHz.

D. Simulation

Fig. 11. illustrates the top block diagram of designed Hall sensor. The hall sensor is composed of the Hall plate, ROIC and PMIC. The designed Hall sensor uses LDO for stable supply voltage. The clock pulse for chopping and switching operation is supplied using the clock generation. The 400kHz frequency generated from the clock is divided for the current spinning frequency of 100kHz. The magnetic field of 0~20mT is supplied at 10kHz for

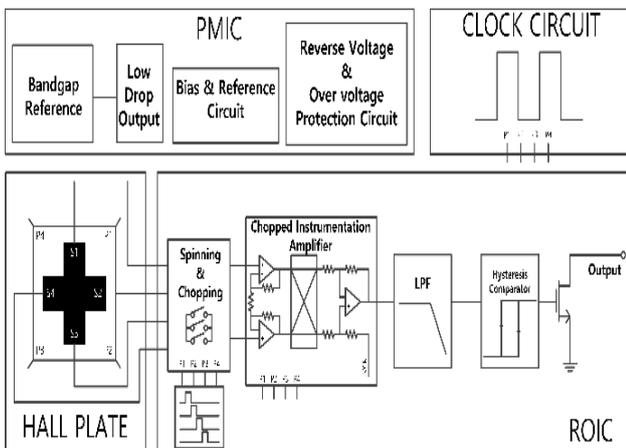


Fig. 11. The top block diagram of the designed Hall sensor

simulation. Fig. 12. shows the output of the Hall plate behind the current spinning and chopping. This means that the magnetic signals and the noise are separated. However, it has small signal that exist in large noise.

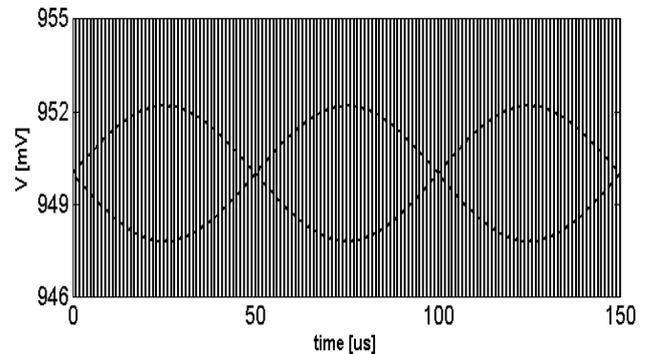


Fig. 12. The output of the Hall plate behind the current spinning and chopping

This output is amplified and demodulated through the proposed IA. The LPF filter is used for reduces chopping ripple behind the amplify stage. Fig. 13. shows the gain and bandwidth of the ROIC that have 64dB and 61kHz respectively. Reduced noise could be verified by the result that difference between the noise gain and signal gain is 43dB. It is shown in Fig. 14.

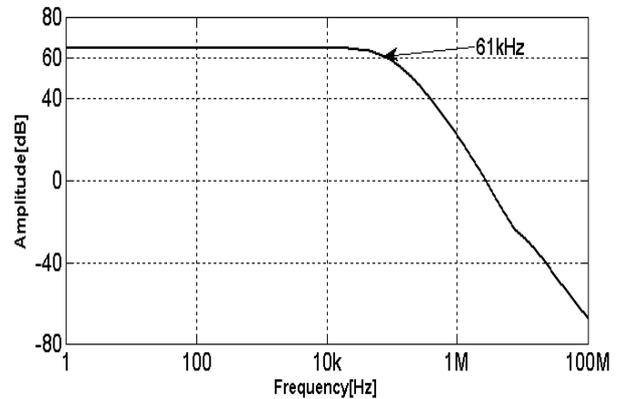


Fig. 13. The gain and bandwidth of the ROIC

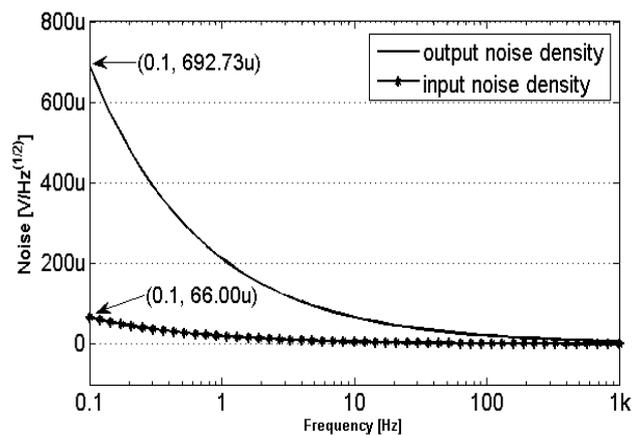


Fig. 14. Difference between the noise gain and signal gain

The comparator is used to switch signal after LPF filter. The output behind the comparator is shown in Fig. 15. It shows switch operation based on magnetic signal.

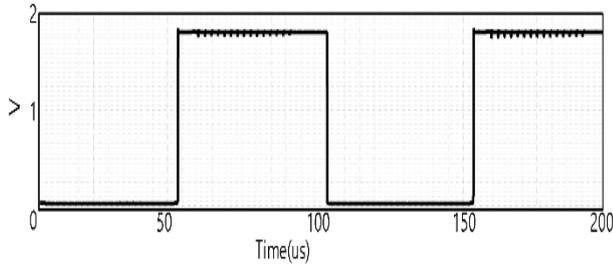


Fig. 15. The switch operation based on magnetic signal

III. RESULTS AND DISCUSSION

The test conditions are shown in TABLE II. The supply voltage is 3.3V and CM voltage is 0.9V. The current spinning frequency is 100kHz and the clock frequency for chopping is 200kHz. 1mA current applied to the sensor, and the magnetic field is applied through the 10Hz rotational motion of Neodymium magnet with 200mT. The experimental environment is configured as shown in Fig. 18. Supply voltage and CM voltage are applied using power supply. The output is measured using an oscilloscope.

TABLE II
The test conditions

Specification	Value
Process [um]	0.18
Supply voltage [V]	3.3
CM voltage [V]	0.9
Current spinning frequency [Hz]	100
Clock frequency [Hz]	200
Bias current [mA]	1
Magnetic field frequency [Hz]	10

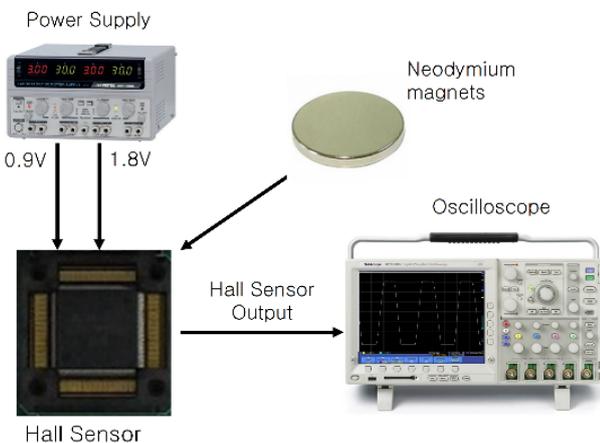


Fig. 18. Environment of the Hall sensor test

Fig. 19 shows the Hall sensor output in response to a magnetic field. It can be confirmed that the output is outputted according to the distance of the magnetic field based on the CM voltage of 0.9V. This output signal can be used to output a switching signal as shown in Fig. 20. using a comparator.

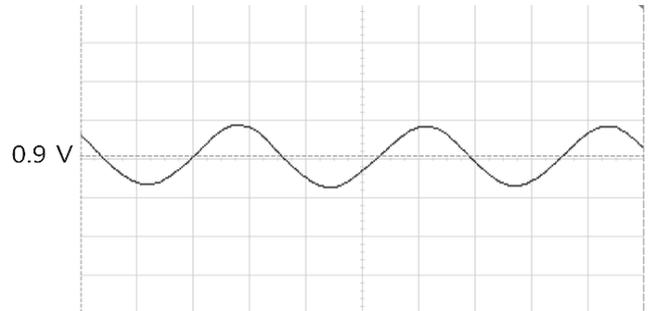


Fig. 19. Output of the Hall sensor

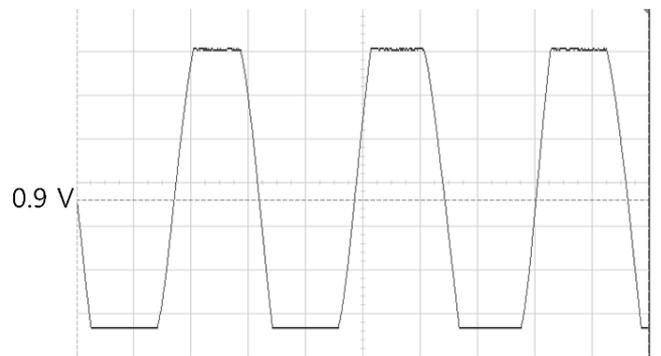


Fig. 20. Hall sensor as switch

IV. CONCLUSIONS

In this paper, the low noise ROIC for CMOS Hall sensor is designed. The CMOS Hall plate has been modeled using the Verilog-A language for simulation. The IA is used to amplify the modeled signal. Current spinning with chopping technique is used for low noise. When de-chopping is performed at the last amplifying stage, there is a problem that the chopping noise is increased by amplified swing range as gain of last amplifier. To solve that, the designed Hall sensor in this paper has de-chopping inside the IA, The required slew rate and bandwidth of the op amp are decreased to reduce the chopping ripple. The designed Hall sensor has 100kHz switching frequency. It operates as a switch at 0~20mT magnetic field in 10Hz with 1mA bias current. The difference between the noise gain and signal gain is 43dB. Further research about the offset reduction of the last amplifier in the proposed ROIC needs to be conducted.

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REFERENCES

- [1] Samuel Huber Lindenberger, "Active Stabilization of the Magnetic Sensitivity in CMOS Hall Sensors" A Ph.D. the Albert-Ludwigs-University Freiburg, 2017
- [2] Popovic, Radivoje S, Hall Effect Devices, 2nd ed. C RC Press, 2010.
- [3] Sandra Bellekom, "CMOS versus bipolar Hall plates regarding offset correction" Sens. Actuators A Phys., vol. 91, no. 1, pp.178-182, 1999.
- [4] Yue Hu, Wen-Rong Yang "CMOS Hall Sensor Using Dynamic Quadrature Offset Cancellation" Proc. 8th Int. Conf. on Solid-State and Integrated Circuit Technology, pp. 284-286, Oct 2006.
- [5] Bilotti A, Monreal G and Vig R "Monolithic magnetic Hall sensor using dynamic quadrature offset cancellation" IEEE J. Solid-State Circuit 32 pp. 829-36, 1997.
- [6] H.P. Balts, and R. S. Popovic, "Integrated semiconductor magnetic field sensors," Proc. on IEEE, vol. 74, no. 8, pp. 1107-1323, Aug 1986.
- [7] Hadi Heidari, "Current-mode high sensitivity CMOS Hall magnetic sensors" A Ph.D. University of Pavia. 2015.
- [8] Yue Xu and Hong-Bin Panm, "An improved equivalent simulation model for CMOS integrated Hall plates," Vol. 11, no.6, pp.6284-9296, 14 April 2011.
- [9] Demierre, M., "Improvements of CMOS Hall Microsystems and Application for Absolute Angular Position Measurements" Ph.D. Thesis, EPFL, Lausanne, Switzerland, 2003.
- [10] H.-C. Seol, Y.-C. Kwon and O.-K. Kwon "Small-area low-ripple chopper instrumentation amplifier using sample-and-hold circuit," Vol. 49, pp.1203-1205, Sept 2013.



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