A 10-bit Single-Ended SAR ADC with Split Dual-Capacitive-Array for Multi-Channel Neural Recording System

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Abstract **- This paper presents a power and area efficient SAR ADC for the interface of multi-channel neural recording system. A SAR-ADC with the split dual-capacitive array for the multi-channel is proposed to promote multiplexing between channels, thus eliminating the linearity degradation owing to the offset mismatch between multiple comparators. Additionally, the proposed scheme has the equivalent capacitance between differential comparator inputs, which minimizes the kickback noise error in the conventional scheme. The proposed ADC additionally reduces the total capacitance and switching energy by 84.8% and 91.3% compared with conventional SAR ADCs for multi-channel applications, respectively.**

I. INTRODUCTION

Since advances in low-power integrated circuits, multi-channel neural signal acquisition systems for ECG, EEG, and EMG have been widely studied for portable and implantable biomedical devices. In the design of these ADCs, the key features are towards low power and small area, resulting in SAR architectures with a segmented capacitive-array to be the most preferred solution [1-5]. One of the segmented SAR architectures is the dual-capacitive-array (DCA) structures [1,2,5] in order to reduce the switching energy of the capacitive-array, but higher bandwidth and larger area are required for analog front-ends (AFEs) as the number of channels increases due to the use of a single sample-and-hold (S/H) circuit. In [2], the modified DCA structure that uses dedicated S/H for each channel is proposed to overcome the bandwidth problem in [1]. However, required number of comparators is proportionally increased as the number of channels increases and the offset mismatch among individual comparators is problematic for better linearity. In addition, the kickback noise in DCA structures causes linearity performance degradation due to the difference of capacitance in differential comparator inputs. Another segmented SAR architecture to r

educe area is the split capacitor array scheme with two attenuation capacitors, which can be applied to both a single -ended and a differential-input SAR ADC [4]. Even though the attenuation capacitors are additionally split to decrease the switching energy, linearity performance is degraded due to their mismatch.

In this paper, a single-ended SAR ADC by using split dual-capacitive-array (S-DCA) with shifted input range for multi-channel systems is proposed. This work has several advantages: (1) dramatically reduced switching energy by using S-DCA as well as by shifting sampled input voltage, (2) released bandwidth limitation in AFEs, (3) minimized chip size without degradation in performance due to the kickback noise, and (4) enhanced speed of a comparator at low supply voltage operation because of the aforementioned input-range shifting scheme of sampled input voltage. The total capacitance and the switching energy of the proposed ADC can be reduced by 84.8% and 91.3% compared with the conventional DCA in [1], respectively.

Section II shows the conventional and proposed architectures. Section III shows the circuit description about two representative advantages of this work. Section IV and V shows simulated results and conclusion.

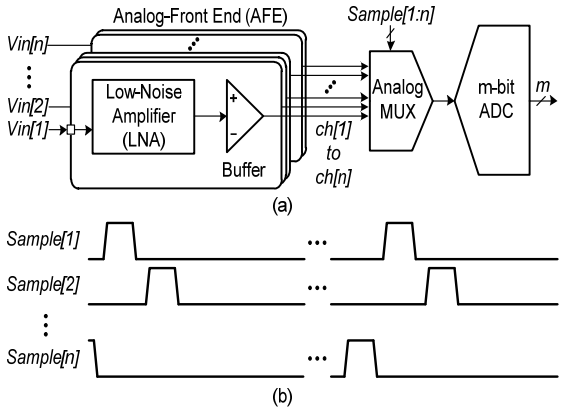

Fig. 1. (a) Block diagram of conventional multi-channel architecture for neural recording system. (b) Timing diagram of sampling signals for channel inputs.

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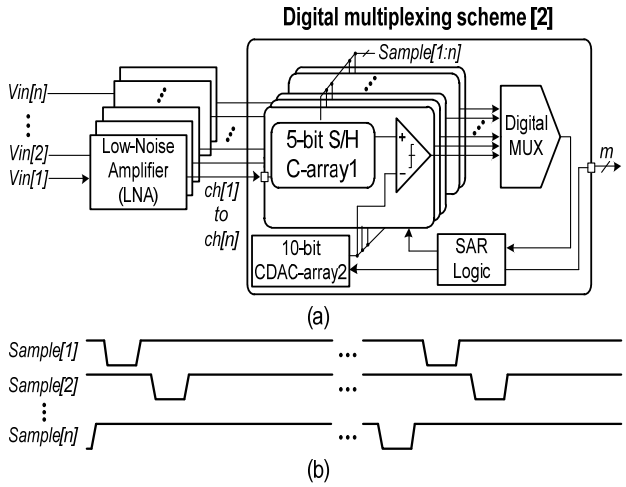

Fig. 2. (a) Block diagram of multi-channel architecture with digital multiplexing scheme [2] (b) Timing diagram of sampling signals for channel inputs.

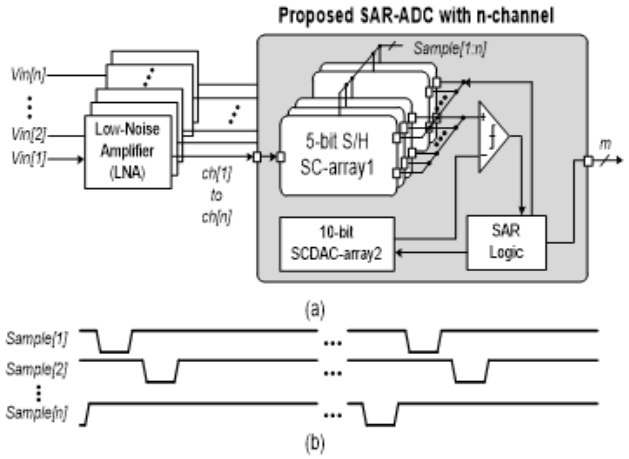

Fig. 3. Block diagram of multi-channel system with proposed n-channel SAR ADC.

II. ARCHITECTURE

Fig. 1 (a) shows the block diagrams of conventional neural recording system with *n* channels configuration. It is composed of n AFEs, an analog multiplexer (MUX) and an m-bit ADC. The AFE consists of low-noise amplifier (LNA) and buffer. Successive-approximation register (SAR)-type ADCs are preferred for the m-bit ADC owing to inherent low-power and small area compared with other type ADCs. Because every channel shares only one ADC, the sampling operation is performed sequentially for each channels and the sampling time of each channels is limited by the number of channel. Fig. 1 (b) illustrates the timing diagram of sampling signals for channel inputs (Vin[1], Vin[2] … Vin[n]). The sampling operation of ADC is performed for each ADC input (ch[1], ch[2], … , ch[n]) in sequential order. Because the settling time for ADC is limited in multi-channel system, one ADC can handle as many as 32 channels [1,2,5], which means that the sampling window becomes smaller when the number of channel increases. Consequently, both the analog MUX and ADC must be preceded with a driving buffer with sufficient bandwidth and slew rate to minimize sampling error in ADC. These buffers consume much higher power consumption than those of front-end amplifiers because of large bandwidth and high slew rate requirements. This explains the excessive power dissipation for buffers in a conventional multi-channel system.

To overcome this problem, digital multiplexing scheme [2] is developed by merging the multiplexing function with an ADC, thus effectively eliminates analog MUX and associated buffers in conventional structure. Fig. 2 (a) shows the block diagram of multi-channel system with the digital multiplexing scheme. Because the analog MUX is replaced by digital MUX, the AFE contains only LNA block. Unlike conventional neural recording system, the block containing an S/H circuit and a comparator is independently assigned for each channel in [2], which means that the sampling time is not related with the number of channels. As shown in Fig. 2 (b), the sampling period is not limited by the number of channel because of the independent S/H circuit for each channel. Furthermore, the sampling period for each input channel is extensively increased compared with the conventional neural recording system. However, the architecture of [2] needs comparators as many as the number of channels, which leads to the linearity performance degradation owing to offset mismatch between comparators and the large area. In the proposed ADC architecture, these drawbacks are eliminated in aspect of architecture level. Furthermore, total capacitance and switching energy are greatly reduced in circuit level. Fig. 3 shows the block diagram of the proposed architecture for multi-channel applications. It is composed of *n* upper capacitive-arrays (5-bit S/H SC-array1), a lower capacitive-array (10-bit SCDAC-array2), a comparator and a SAR logic. The single comparator is shared for the multi-channel, which eliminates the offset problem of digital multiplexing scheme [2]. 5-bit S/H SC-array1 are assigned for each channel (*ch[1:n]*) and theirs outputs are connected to the positive input of the comparator. 5-bit S/H SC-array1 plays a role of S/H for each channel input and a DAC for upper 5 MSB bits. 10-bit SCDAC-array2 capacitive-array is used for lower 5 LSB bits.

III. CIRCUIT DESCRIPTION

As shown in Fig. 4, the proposed ADC with 10-bit resolution consists of 10-bit split dual-capacitive-array (S-DCA), *n* PMOS switches (M_1), a comparator, and a SAR logic. The 10-bit S-DCA includes *n* 5-bit S/H split capacitive (SC) array1s in each channel and a 10-bit split capacitive-DAC (SCDAC) array2. When one channel input is selected, the dedicated 5-bit S/H SC-array1 is activated and connected to comparator by turning on the M_1 transistor and the other 5-bit S/H SC-array1s sample associated inputs. After the sampling operation, the sampled input signal is resolved to 5MSB bits by using the 5-bit S/H SC-array1. During the decision of 5MSB bits, the top-plate of the 10-bit SCDAC-array2 is set to the V_{REF} by the M_2 transistor. The remained 5LSB bits are resolved in the 10-bit SCDAC-array2 with the same manner in the 5-bit S/H SC-array1. The proposed S-DCA has several advantages and these will be described in the following sub section.

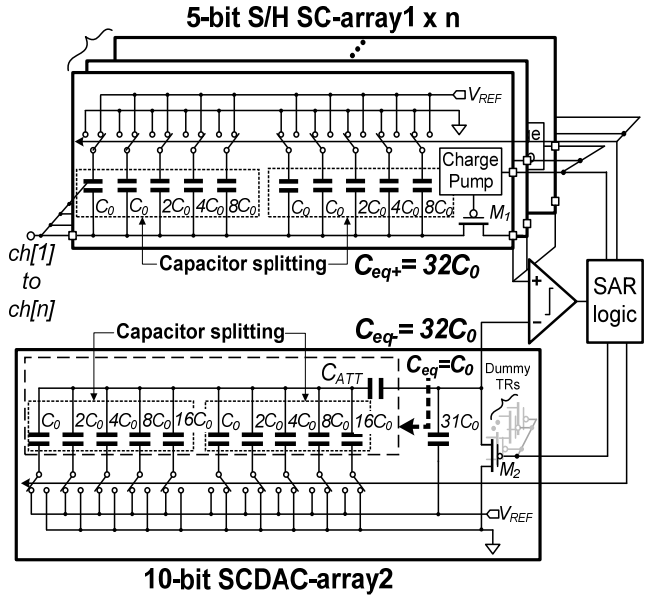

Fig. 4. Block diagram of proposed SAR ADC for multi-channel neural recording system.

A. Kickback noise reduction

The kickback noise is critical error comes from dynamic comparator in SAR ADC. When comparator is activated, parasitic capacitances of input transistors in comparator disturb the input voltages of comparator. This fluctuated voltage is accumulated through the bit-cycle and degrades the linearity of ADC. In case of the DCA structure as shown in Fig. 5, the capacitances of two capacitive-arrays are different from each other, which lead to the different amount of kickback noise to the inputs of comparator. To minimize the kickback noise error, DCA structure uses large unit capacitances over 50fF. In the proposed design, however, the capacitances of two capacitive-arrays are same with $64C_0$, which has the same voltage fluctuation to the two capacitive-arrays when comparator is activated. In order to consist of identical amount of capacitive-arrays, this ADC uses the attenuation capacitor (C_{ATT}) to make the equivalent capacitance same in both differential input of comparator.

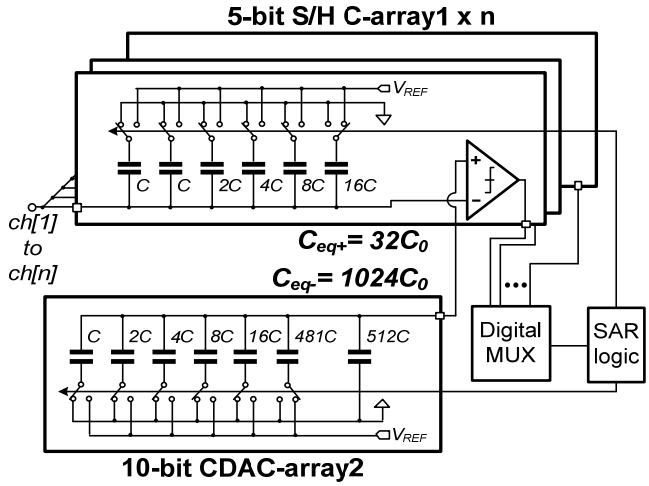

Fig. 5. Block diagram of digital multiplexing scheme [2] with multi-channel system.

Also, the effect of kickback noise is reduced compared to the DCA structure and its level is same as the differential-input SAR ADC with single-channel. However, when the number of channel increases, parasitic capacitances of switches for channel selection is dominant and increase the comparator error from kickback noise. To minimize the channel effect, dummy transistors for modeling of channel selection switches is also considered in the proposed ADC.

B. Energy-efficient switching scheme

In a single-ended SAR ADC, the capacitive-array is the most power hungry block owing to the large amount of switching energy. Although the DCA SAR ADC reduces the switching energy at the expense of the additional 5-bit sample and hold (S/H) array, the DCA SAR ADC still consumes large amount of switching energy during the S/H operation. Several techniques using additional voltage reference of V_{CM} (=V_{REF}/2) have been introduced to reduce the switching energy [6, 7]. When V_{CM} is lower than the threshold voltage of the MOS switches, however, it cannot be applied to low-voltage applications [4]. The proposed ADC with no extra voltage reference achieves at least 42.7% less switching energy as compared with other single-ended SAR ADCs.

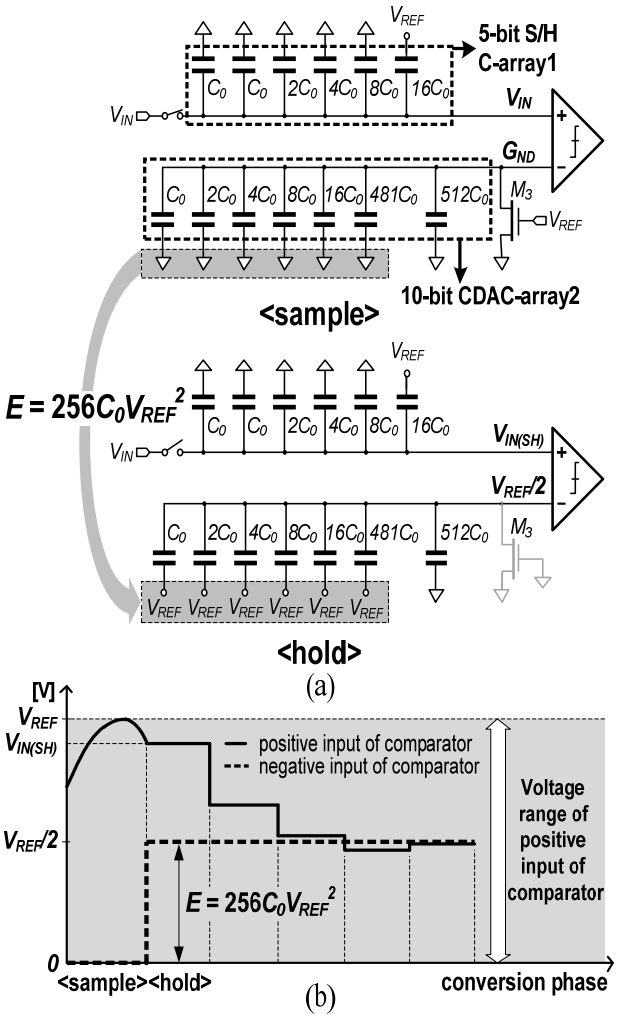

Fig. 6. Block diagram and switching energy generation of 10-bit DCA SAR ADC. (a) block diagrams of the sample and hold operations (b) waveform of the comparator inputs (only the upper 5 MSBs are shown)

Fig. 6 (a) shows the block diagrams when the phase changes from sample to hold in the DCA SAR ADC, where the 10-bit DCA includes a 5-bit S/H C-array1 and a 10-bit CDAC-array2. The largest capacitor of $512C_0$ is not for switching operation but for the binary ratio of the 10-bit CDAC-array2. In the sample phase, the positive input of a comparator is connected to the V_{IN} and the negative input is set to G_{ND} through M_3. Once the positive input of the comparator is sampled and held to be $V_{IN(SH)}$, the halves of the capacitors $512C_0$ (C_0, $2C_0$, $4C_0$, … , $481C_0$) in the 10-bit CDAC-array2 are reconnected from G_{ND} to V_{REF}, which results in $V_{REF}/2$ voltage shift of the negative input with the large switching energy of $256C_0V_{REF}^2$. Fig. 6 (b) shows the waveform of the comparator inputs, where the voltage range of positive input of comparator is ranged from 0 to V_{REF}.

Fig. 7 (a) shows the block diagram of the proposed ADC for the S/H operation. The capacitor of $62C_0$ is for the binary ratio of the 10-bit CDAC-array2. The proposed ADC with S-DCA not only has the same capacitance between two capacitive-arrays but also contains the less total capacitance compared to the DCA SAR ADC.

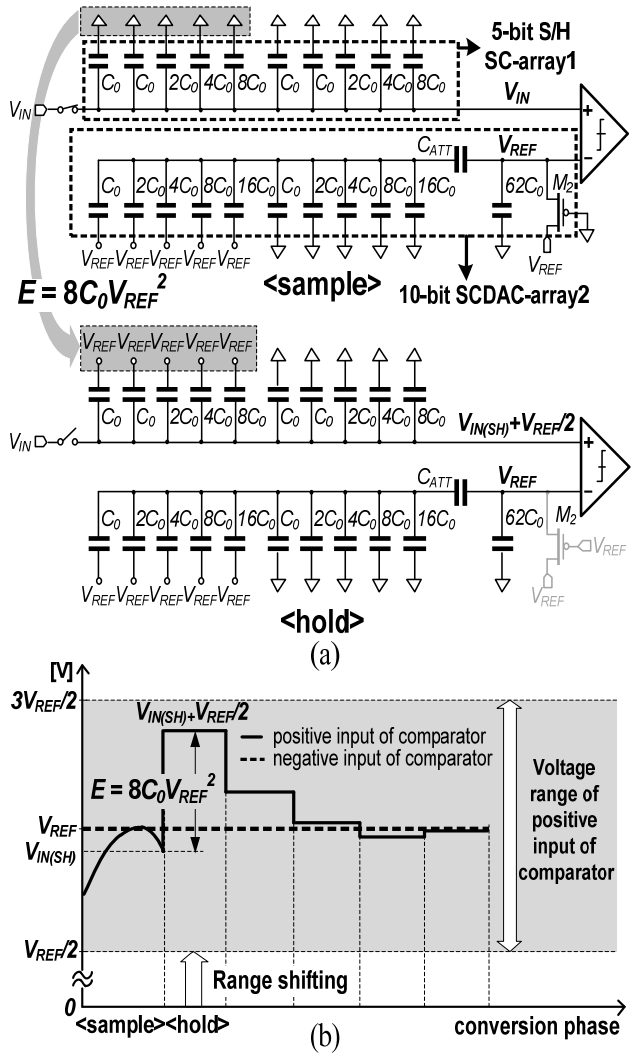

Fig. 7. Block diagram and switching energy generation of the proposed 10-bit SAR ADC with S-DCA. (a) block diagrams of the sample and hold operations (b) waveform of the comparator inputs (only the upper 5 MSBs are shown)

The analog voltage transition of the proposed ADC is different from the DCA structure. Unlike the DCA that the negative input of the comparator is shifted up by $V_{REF}/2$, the positive input of comparator in the proposed S-DCA is shifted up by $V_{REF}/2$ to reduce the switching energy by 96.9% during the S/H operation. In the sample phase, the positive input of comparator is connected to the V_{IN} and the negative input is set to V_{REF} through M_2. In the hold phase, the halves of capacitors 16 C_0 (C_0, C_0, $2C_0$, … , $8C_0$) in the 5-bit S/H SC-array1 are reconnected from G_{ND} to V_{REF}, which results in $V_{REF}/2$ voltage shift of the positive input with the switching energy of $8C_0V_{REF}^2$. Eventually, the positive input of comparator becomes $V_{IN(SH)}+V_{REF}/2$ and its voltage range is shifted up by $V_{REF}/2$ as shown in Fig. 7 (b). The switching energy of the proposed S-DCA for the S/H and conversion phases is $80C_0V_{REF}^2$ and $12.1C_0V_{REF}^2$, which corresponds to 3.1% and 30% when compared with the DCA [4], respectively.

IV. SIMULATED RESULTS

Fig. 8 shows MATLAB behavioral simulation results of the switching energy in 10-bit SAR ADC with various switching schemes. The proposed ADC shows the saw-type waveform which is the lowest switching energy over the entire output codes when this idea was proposed. The average values are summarized in Table 1.

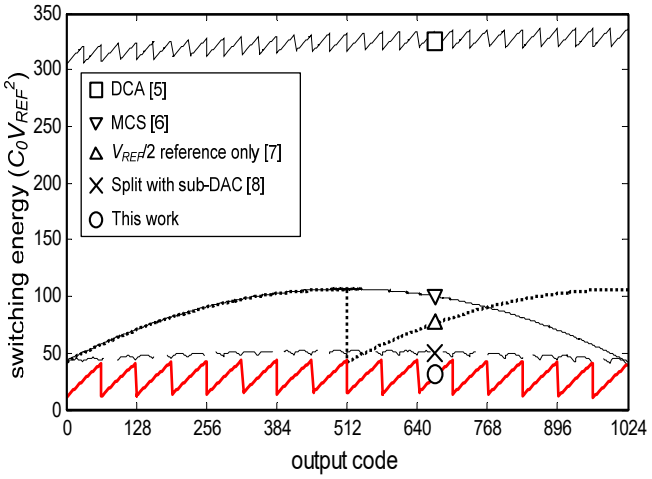

Fig. 8. Comparisons of the switching energies.

TABLE 1.
Comparisons of the various switching schemes
(only for single ended SAR ADCs).

Switching procedure	Average switching energy ($C_0V_{ref}^2$)	Energy saving (%)
DCA [5]	323.0	reference
MCS [6]	85.3	73.6
$V_{REF}/2$ reference only [7]	84.7	73.7
Split with sub-DAC [8]	49.1	84.8
This work	28.1	91.3

TABLE 2.
Performance summary of the proposed 10-bit ADC.

Process	55nm CMOS process
Supply	0.5V
Resolution	10bit
Sampling rate	500kS/s
SFDR	74.51dB
SNDR	58.6dB
ENOB	9.44bit
Power consumption	2.51uW
FOM	7.2fJ/conversion-step
Unit capacitance	5fF
Core area (only 1-channel)	0.13 x 0.07 mm^2

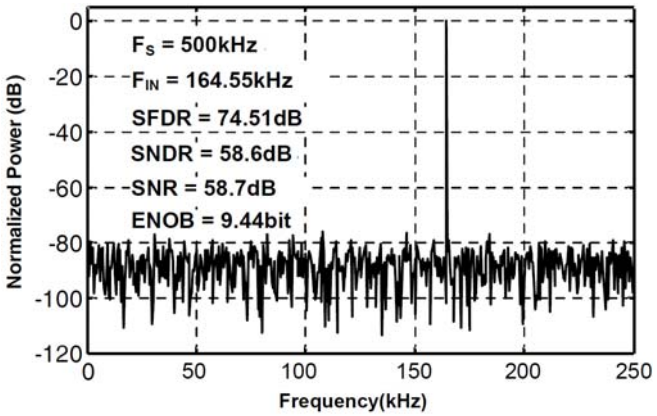

Fig. 9. Dynamic performance (FS = 500kHz, FIN = 164.55kHz).

The proposed ADC reduces the average switching energy by 91.3% and 42.7% when compared with the DCA SAR ADC [5] and the split with sub-DAC [8], respectively. Table 2 shows the performance summary of the proposed 10-bit SAR ADC in 1P6M 55nm CMOS process. As shown in Fig. 9, SNDR of 58.6dB and SFDR of 74.5dB are achieved at 500kS/s and 0.5V supply. The analog circuits (comparator, S/H, CDAC) consume 1.58uW while the digital power consumption is 0.93uW. The FOM of the proposed 10-bit SAR ADC is 7.2fJ/conversion-step.

V. CONCLUSIONS

In this paper, single-ended SAR ADC with S-DCA for multi-channel neuron sensor system is proposed. The proposed SAR ADC arranges the S/H for each channel as in the [2], which results in removing the buffer block in AFE. Additionally, the large amount of kickback noise in [2] is reduced by setting the same amount of capacitance ($64C_0$) in two comparator inputs, which save the total unit capacitance 84.4% compared to the DCA structure and enable the proposed ADC to use small unit capacitance as in [4]. By shifting up the range of sampled input, the switching energies of the proposed ADC for the S/H and conversion phases are dramatically reduced compared with the conventional DCA SAR ADC. As a result, the proposed ADC reduces the switching energy by at least 42.7% as compared with the other schemes [5-8] and achieves the state-of-the-art performance with regard to the switching energy among the single-ended SAR ADCs.

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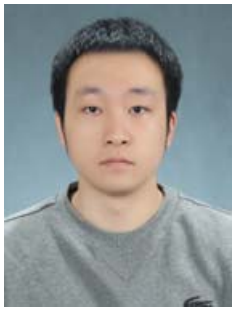

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