Multi Stage Noise Shaping Delta-Sigma Modulator

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***Abstract* – This paper presents a multi stage noise shaping (MASH) delta-sigma modulator (DSM) for high speed data signal processing. This delta-sigma modulator (DSM) is discrete-time modulator (DT) and sampling of the input signal occurs prior to the loop filter. Discrete-time (DT) modulator has lower performance degradation from excess loop delay, clock jitter, process variation than Continuous-time (CT) modulator. A 4-Phase buck converter is used to supply power in delta-sigma modulator (DSM). The delta-sigma modulator (DSM) power supply is 1.8V. The buck converter has low EMI using spread spectrum. To implement spread spectrum, the paper proposes random clock generator. The buck converter supply voltage 3V and Output voltage is 1.8V. Switching frequency ranges from 7 to 9 MHz and Maximum load current is 500mA. The delta-sigma modulator (DSM) and buck converter is fabricated in 0.18㎛ CMOS process and circuit type is Mixed-design.**

I. INTRODUCTION

With the increasing development of wireless communication systems, high-performance analog circuit building blocks with wide signal bandwidths of several mega-hertz are required. Analog-to-digital converter (ADC) is one of the most important building blocks in the communication systems. Delta-sigma modulator (DSM) is a very popular architecture in the ADC for wireless communication application because it is possible to implement oversampling [1]. DSM can be realized in either continuous-time (CT) of discrete-time (DT) method. DT DSM is popular than CT DSM because it is more robust to excess loop delay and clock jitter problems [2].

The emergence of Internet of the Things (IoT), sensor and power management IC's importance is becoming increasingly in the industrial world. Buck converter is one of the power management IC [11], they are widely employed in devices to supply power in systems. Especially, portable devices are required to have low noise processing power as the performance of sensor and application process are improved [17], [18]. Supplying low noise power is very important in sensor and healthcare industry [19], [20]. This paper proposes a 4-phase buck converter with low EMI. Random clock generator is used to implement spread spectrum. Spread spectrum is one of frequency dispersion technology. By using spread spectrum, EMI of buck converter can be reduced considerably. Therefore, the buck converter can supply low noise power in DSM.

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II. EXPERIMENTS

A. Multi Stage Noise Shaping DSM

MASH DSM is suitable for the recent communication applications because the advantages of wideband operation and stability. MASH DSM improves stability and noise shaping performance by cascade of low-order modulator.

Sampling frequency of wideband modulator is proportional to the speed and power consumption of the circuit. So over sampling ratio (OSR) is must be low [3]. In order to keep the noise shaping characteristics at low OSR, modulator has high-order and multi-bit quantization is required. However, the high-order single-loop structures have higher performance than low-order, there is a problem in stability. In addition, high-order modulator input range is limited for stability. To overcome the stability problem of the loop filter, some methods may be used, but decreasing the noise shaping performance. MASH DSM has stable due to the use multiple-stage which has a stable low-order modulator respectively [4].

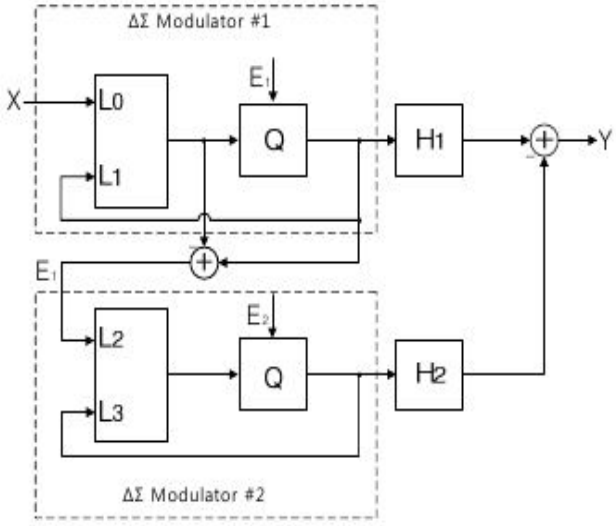

Fig. 1. Two-stage MASH delta-sigma modulator architecture.

Fig. 1 shows two-stage MASH DSM block diagram. MASH DSM has a high-order performance by cascade of low-order modulator. Since each DSM has the local feedback, it has an advantage with low-order stability. E1 only on subtract the quantization input and output of the first stage, as shown in fig 1, which is the first stage quantization noise which is applied to the input of the second stage.

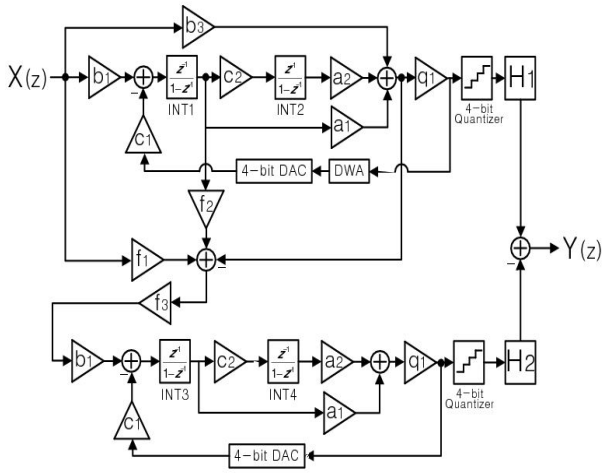

Fig. 2. Two-stage CIFF 4-bit MASH delta-sigma modulator.

Fig. 2 shows two-stage CIFF 4-bit MASH DSM architecture. This structure is implemented by MATLAB. Using coefficient and seek transfer function of this two-stage MASH DSM as (1)

$$Y = Z^{-2}(2 - Z^{-1}) \times X + (1 - Z^{-1})^4 \times E_2 \quad (1)$$

As applied to the second stage input E1 shown at equation (1), it is not appeared in the output. Because this is canceled by digital filter H_1, H_2. Therefore, the second stage quantization noise E2 is only appeared on the entire transfer function. Eventually entire quantization noise can be seen that forth-order noise shaping.

As shown in Fig. 2, the DSM uses a CIFF type. CIFF type is a method that has recently been widely used in small output voltage swing of the integrator. So operational transconductance amplifier (OTA) of headroom, slew rate can be mitigated because the chain of Cascade of Integrators with Feedback (CIFB) is way more efficient in terms of power. However, CIFF method has the disadvantage that Signal transfer function (STF) is the peaking phenomenon that appears in the out-of-band [5],[6]. Peaking phenomenon of STF may be present when the out-of-band interference in a communication system application has a problem to decrease the Dynamic range (DR) of the modulator occurs [7]. STF peaking of ADC front end can be reduced by the anti-aliasing filter, but thereby amplifying the out-of-band peaking due to the feedforward path. Therefore, when using the CIFF structure, it is important to reduce out of band-STF peaking phenomenon as much as possible [8]-[10]. 2-2 MASH DSM has the advantage of appearing out-of-band STF peaking phenomenon lower because they are determined by the 2nd-order non-STF is 4th-order.

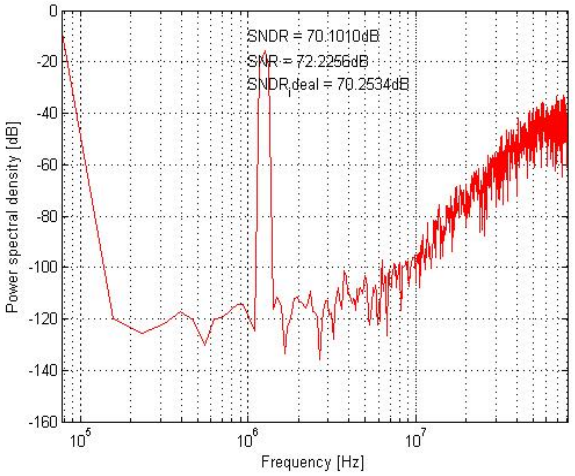

Fig. 3. Output spectrum of MASH DSM (32 k-points FFT).

Fig. 3 shows output spectrum of MASH DSM. The main performance parameters are summarized in Table 1. The power consumption is 45 mW, excluding the power consumption of the digital output buffers.

TABLE I.
Summary of simulation results

Parameter	Value
Supply voltage	1.2 V
Signal bandwidth	10 MHz
Sampling frequency	160 MHz
Oversampling ratio	8
SNDR	70.1 dB
Total power consumption	45 mW

B. A 4-Phase Buck Converter with Low EMI

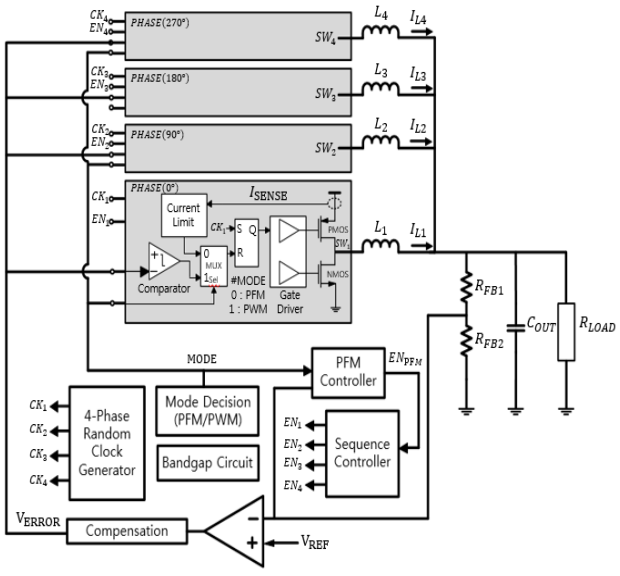

Fig. 4. Proposed DC-DC Buck Converter.

Fig. 4 shows a proposed 4-phase DC-DC Buck converter, which includes four single-phase modulators that are controlled in an interleaved manner [12], [13]. And the buck converter is composed of 4-phase clock generator, power transistor, power transistor controller, PWM/PFM mode controller [15], [16], [21], bandgap circuit, error amplifier. The buck converter achieves low EMI through random clock generator.

Conventional buck converters are generally operated in fixed switching frequency. Therefore, High EMI and noise are generated at switching frequency and harmonic frequency. It can cause malfunction of buck converter and latch-up and it degrades the performance of sensor and other devices.

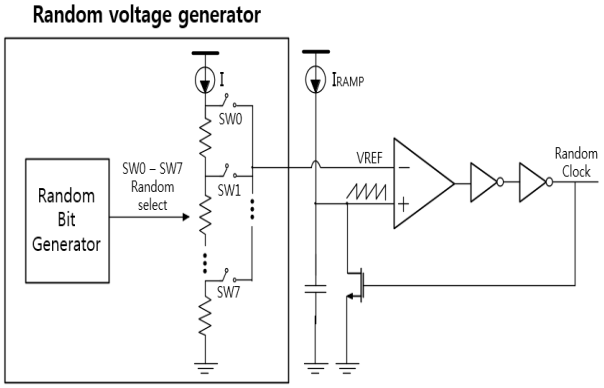

Fig. 5. Proposed Random Clock Generator.

Fig. 5 is a proposed random clock generator, which includes random bit generator. Random bit generator operates 3 bit randomly and those bits are input of decoder. Output of decoder has only one high between 0-7. It makes sw0-sw7 turn on and V_{ref} is changed randomly. Clock signal is made by comparing two input; V_{ref} and ramp signal. Ramp signal is occurred through capacitor charge and discharge. If the NMOS switch is turn off, capacitor is charged by current; I_{RAMP}. If the NMOS switch is turn on, current flow the NMOS and ramp signal is zero. V_{ref} is changed randomly in defined region. Therefore, clock generator can operate various frequency randomly.

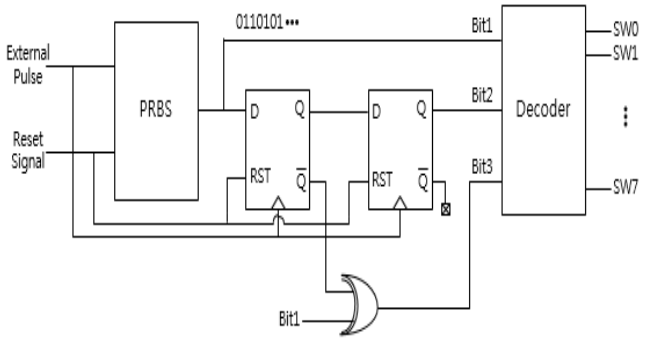

Fig. 6. Random bit generator.

Fig 6 shows a random bit generator [14]. Random bit generator is composed of pseudo random binary sequence (PRBS), d flip-flop, decoder and exclusive or gate. PRBS operate random binary sequence and bit 1 is output of PRBS, bit 2 is an output of second d flip-flop and bit 3 is an output of exclusive or gate of first d flip-flop output and bit 1. Bit 1, bit 2, bit3 are input of decoder and outputs are from sw0 to sw7. Only one switch turns on.

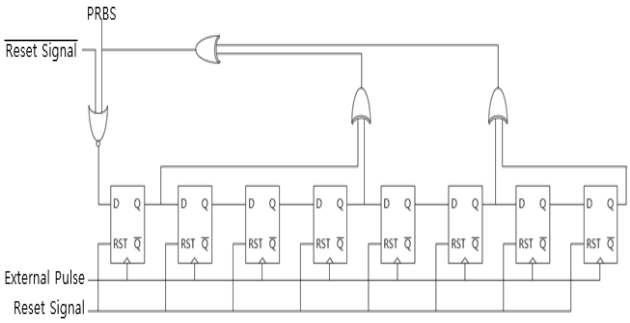

Fig. 7. Pseudo random binary sequence (PRBS).

Fig. 7 is a pseudo random binary sequence, which composes 8 d flip-flop. When reset signal is high, 8 d flip-flops turn off and operates signal each cycle. Nor of $\overline{reset\ signal}$ and output of PRBS is entered input of first d flip-flop. Therefore, this pseudo random binary sequence can operate bits similar random bit generator output.

Switching frequency ranging from 7-9MHz and EMI is reduced over -10dB. Fig. 8 and Fig. 9 present FFT simulation result of inductor current. Conventional buck converter has sharp noises switching frequency and harmonic frequency. EMI of proposed buck converter is distributed. Table 2 is a comparison of EMI between conventional and proposed buck converter.

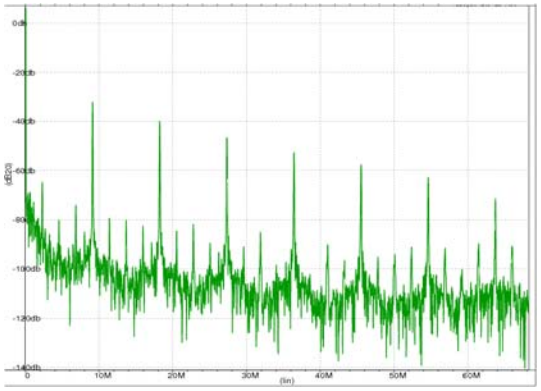

Fig. 8. EMI of conventional buck converter.

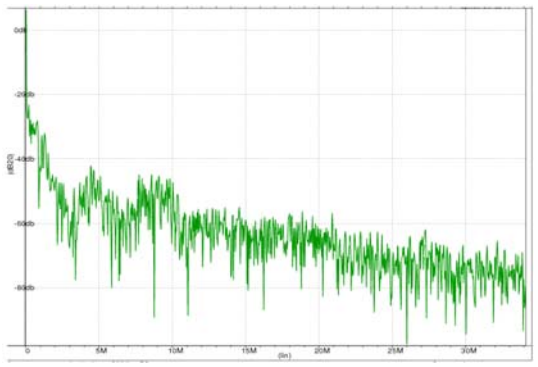

Fig. 9. EMI of proposed buck converter.

TABLE II.
EMI comparison of buck converter

	Conventional buck converter	Proposed buck converter
Switching frequency	8MHz	7-9MHz
Peak EMI (Switching Frequency)	-32.2dB	-45.7dB
Peak EMI (2st Harmonic Frequency)	-40dB	-56dB

III. RESULTS AND DISCUSSION

Delta-sigma modulator (DSM) and 4-phase DC-DC buck converter are designed and fabricated using 0.18㎛ CMOS process. A high-bandwidth, multi-bit two-stage MASH DSM was presented. CIFF architectures are applied to the first and second stages. The extra active adder in CIFF is eliminated and the adder-less integrator is proposed in the first stage of the two stage MASH DSM. Instead of providing all the digital outputs from the first stage quantizer to operate the feedback DAC in the interstage, an analog summing is implemented in the designed DSM. The modulator achieves the SNDR of 70.1 dB over the 10-MHz bandwidth from a 1.2-V supply with 45 mW and A buck converter includes four phase for small output ripple. Fig. 10 displays the chip photo of the proposed delta-sigma modulator (DSM) and buck converter.

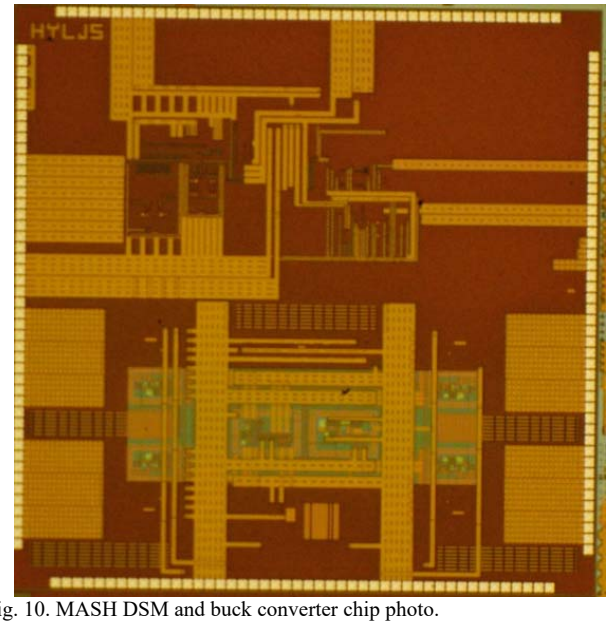

Fig. 10. MASH DSM and buck converter chip photo.

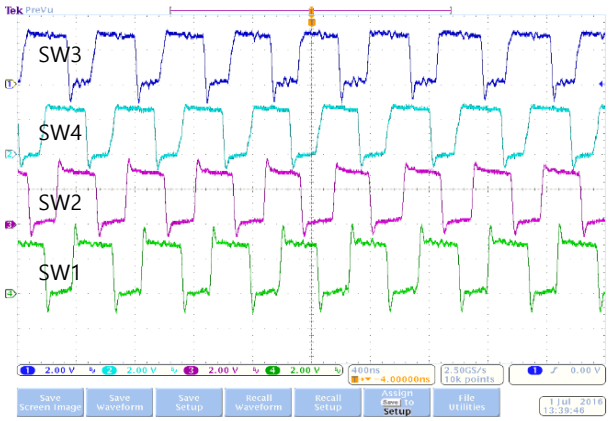

Fig. 11. Measured waveforms of SW nodes in buck converter.

Fig. 11 displays the waveform of SW nodes in each phase during the operation of the proposed multiphase buck converter in PWM mode. Switching nodes are measured when load current is 1mA. Undershoot and Overshoot in switching node occurs due to dead time. Dead time is required to prevent PMOS and NMOS power transistors turn on at the same time. If PMOS and NMOS Power transistor turn on simultaneously, high current flows power transistors and it causes malfunction of buck converter and breakdown of power transistors. When PMOS is on and NMOS off, switching node is high. In dead time, PMOS switch turns off suddenly and parasitic capacitance is discharged and NMOS body diode turns on. When NMOS is on and PMOS is off, switching node is low. In dead time, NMOS switch turns off suddenly and parasitic capacitor is charged and PMOS body diode turns on. Therefore, undershoot and Overshoot are occurred. The waveform shows that all phases are modulated with a phase difference of 90°.

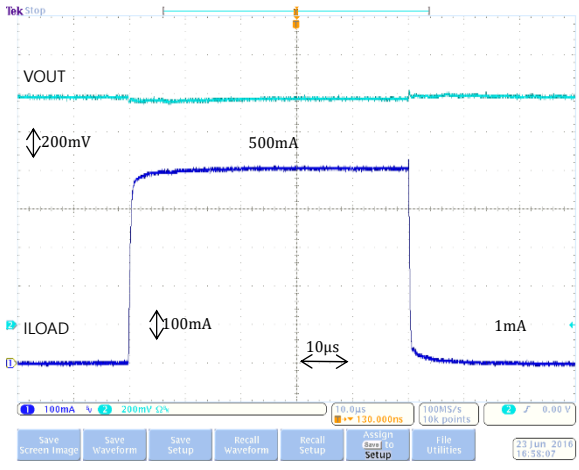

Fig. 12. Measured waveforms of SW nodes in buck converter.

Fig. 12 shows the measured output voltage waveform of the converter with respect to the variation in the load current; the load current varies between 1mA and 500mA, with $V_{IN} = 3\ V, V_{OUT} = 1.2\ \ V, and\ \ F_{SW} = 8MHz$. The voltage waveform (V_{OUT}) shows PWM operations

depending on load current level. When the load current increase, output voltage decreases in a short time because output load requires high current, so the capacitor is discharged. But output voltage is returned back to the original value due to feedback system. In Fig. 12, when load current is 500mA, output voltage is smaller than the output voltage when load current is a 1mA. Because voltage drop power transistor increases, load current increases.

Table III outlines the performance of the fabricated chip. The proposed buck converter has four phases to enable a small output ripple. Each phase operates at a switching frequency of 2MHz. The maximum allowable output current is 0.5A.

TABLE III.
Measurement result of Buck converter Performance

Technology	0.18 μm CMOS
No. of phases	4
Die size	3.8 × 1.9 mm
Switching Frequency	2MHz (Each phase)
Inductor	470nH / phase
Output capacitor	47 × 2 μF
Output current range	0 - 0.5A

IV. CONCLUSIONS

A high-speed, high-bandwidth input-feedforward MASH delta-sigma modulator was implemented for wideband applications, such as a communication system. The modulator was based on a 2-2 4-bit input-feedforward architecture. To implement the summing function of the feedforward paths, the designed architecture included differentiators in front of the last integrator. An efficient switched-capacitor circuit was also developed to implement the differentiators. It significantly reduced power dissipation and complexity compared with the conventional input-feedforward architecture. This architecture is suitable for high-speed ADCs, because the time constraints are relaxed by removing the switched-capacitor adder block. Instead of providing all the digital outputs from the first stage quantizer operating the feedback DAC in the interstage, an analog summing is implemented in the designed DSM. The prototype achieves the peak SNDR of 71.1 dB over the 10-MHz bandwidth from a 1.8-V supply with 45 mW.

Buck converter is used to supply power in delta-sigma modulator (DSM). The buck converter has small output ripple due to multiphase and low EMI by using distributing sharp noise in switching frequency and harmonic frequency. Buck converter is becoming popular power management IC as improvement of technology in sensor and devices. Proposed buck converter can be used widely in Internet of Things (IoT) and healthcare sensor sstem since the buck converter has low EMI. Therefore, It can be attractive technologies in electrical communication industry.

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