A Wide-Range Duty-Independent All-Digital Quadrature-Phase Clock Generator

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***Abstract* - A wide-range, input-duty-independent, all-digital qaudrature-phase clock generator is proposed. By using a supply noise filtering block, the power supply noise effect is reduced. Furthermore, because the proposed clock generator consists of all-digital logic gates, it can easily be migrated to a different process within a short time and operate at a low supply voltage. The circuit was fabricated with a 0.18μm 1P4M CMOS technology and operates over the frequency range from 300MHz to 1.5GHz within 5 cycles of the reference clock. Due to its open-loop scheme without jitter accumulation, the increased peak-to-peak jitter from the delay line to the output buffer is only 4.7ps.**

I. INTRODUCTION

Traditionally, Delay-Locked Loops (DLLs) and Phase-Locked Loops (PLLs) were generally used for clock synchronization and multiphase generation [1]-[4]. Conventional digital PLL/DLLs [2]-[4] make it possible to achieve a fast lock-time, low voltage operation, low power consumption, easy migration, and small area, while their applications may be restricted by the phase error due to the limited resolution of the time-to-digital converter. With the scaling down of technology to the very deep-submicron level, digital PLL/DLLs are now able to achieve reasonable resolution compared to their analog counterparts.

Several digital PLL/DLL architectures have been proposed to reduce the lock-time, such as the binary-search algorithm, which results in a lock-time of less than 50 cycles. However, their closed-loop characteristics cause the lock-time to be greater than 32 cycles, which is unsuitable for fast power down operation [5]-[7]. The lock-time of the all-digital DLL described in [8] is as fast as 8 cycles, due to the use of an asynchronous binary search (ABS) algorithm, but it operates at only 100MHz.

In order to achieve a fast lock-time, various schemes without a feedback loop were proposed [9]-[11]. However, a conventional clock generator requires accurate phase interpolation and a precise complementary clock and may suffer from large phase errors [9] and resolution problems and experience a large amount of jitter caused by power supply noise [10]. Furthermore, its duty dependent feature makes the clock phase error unacceptably large [10]. But, when using the feedback loop to reduce the phase error, the lock time becomes longer [12]-[14]. In this paper, a wide-range, duty-independent, all-digital quadrature-phase clock generator, whose lock-time is 5 cycles of the reference clock, with supply noise filtering and fine resolution, is proposed.

This paper is organized as follows. The overall architecture and the operation of each building block are explained in Section II. Section III shows the experimental results and the die photo. Finally, our conclusions are presented in Section IV.

II. THE PROPOSED ALL-DIGITAL CLOCK GENERATOR

To overcome the problems of conventional digital clock generators with a fast lock-time, a wide-range duty-independent, all-digital quadrature-phase clock generator is proposed, as shown in Fig 1. It consists of a multiphase generator with an inverter delay line, a 1-to-0 transition detector which is similar to the one used in the conventional multiphase generator described in [10], a supply noise filter, a select signal generator, a multiplexer and a phase interpolator. For fast locking, no jitter

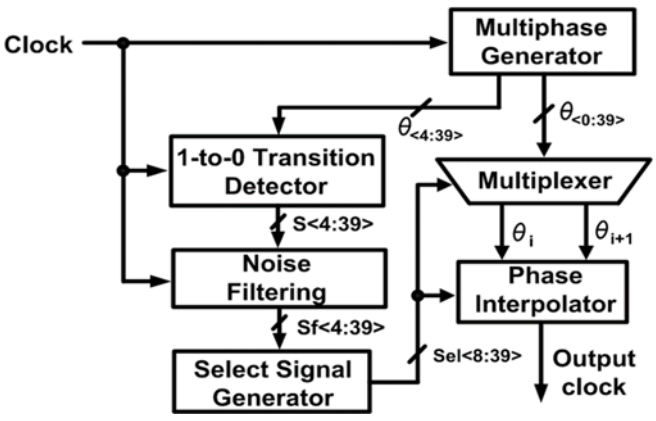

Fig. 1. Overall architecture of the portable all-digital clock generator.

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accumulation, and low-voltage operation, an open-loop and all-digital scheme is used along with noise filtering and delay compensation of the output path. The transition detector is different from the conventional one described in [10], in that the rising edge of the reference clock is compared for the sake of achieving an input-duty-independent scheme. The noise filtering block is added to eliminate the effects of noise, such as supply voltage glitches, which are fatal to the transition detector. The conventional clock generator described in [10] is designed to have a maximum operating frequency, which is about twice the minimum frequency, which makes the design simple at the cost of a narrow operation range. To overcome this limitation, the select signal generator is modified to achieve a wide operating frequency range. The building blocks of the proposed all-digital clock generator are explained in detail as follows.

A. Inverter Delay Line

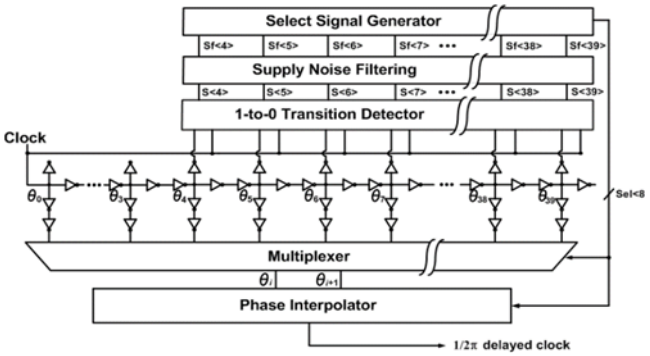
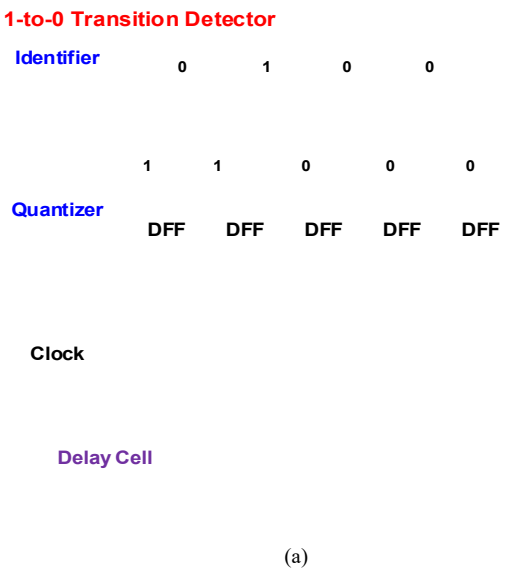
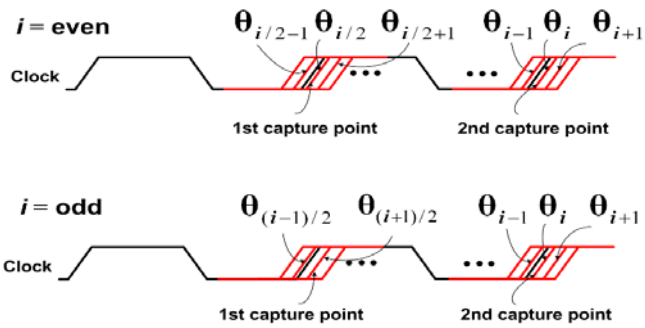


Fig. 2. Overall block diagram of the portable clock generator.



(a)



(b)

Fig. 3. The 1-to-0 transition detector. (a) block diagram and (b) its operation.

The delay line consists of delay cells (two static inverters in series), that produce a series of multiphase clocks with a minimum interval at a particular process. Using this inverter-based time-to-digital converter, the proposed multiphase clock generator can overcome the false-lock problem, which is one of the main issues in the case of conventional DLLs [2]. The number of delay cells determines the operating frequency range. Each delay cell has a delay τ and the delay line consists of 39 delay cells. Hence, the delay line produces multiphase clocks θ_0, θ_1, θ_2, … , θ_{38}, θ_{39} and can have a minimum and maximum delay of 0τ and 39τ, respectively, as shown in Fig. 2. The 36 multiphase signals, from θ_4 to θ_{39}, are transferred to both the 1-to-0 transition detector block and the multiplexer block, while the 4 multiphase signals, from θ_0 to θ_3, are only transferred to the multiplexer.

B. 1-to-0 Transition Detector

The 1-to-0 transition detector of the multiphase generator in [10] senses a π phase-delayed clock, which results in duty-dependent operation. To solve this problem, the modified 1-to-0 transition detector senses the position of the delay cell stage that is delayed for one cycle or multiple cycles (2, 3, 4, 5, 6, 7 and 8 cycles) of the input clock, i.e. the 2π, 4π, 6π… , 16π phase-delayed clock. Thus, the proposed quadrature phase clock generator has an input-duty independent feature. In addition, it senses multiple 1-to-0 transition points in order to increase the operating frequency range. The multiple 1-to-0 transition signals are filtered in the select signal generator.

The block diagram and operation of the 1-to-0 transition detector which consists of a quantizer and an identifier, as shown in Fig. 3(a). In the quantizer, using an array of negative edge-triggered D/FFs, the rising edges of the multiphase clocks are compared with that of the input clock and the D/FFs produce logic one or zero states. The identifier detects the output signals of the D/FFs, changing from high to low at the 2π and 4π phases at the minimum operation frequency. At the maximum operation frequency, the detection occurs at the 2π, 4π … 14π, and 16π phases, which makes the proposed generator independent of the duty ratio of the input clock. The clock signal fed to each D/FF is delayed by one inverter and one transmission gate: The inverter is used to match the inverter insertion delay of the D/FF data path and the transmission gate to guarantee the setup time of the D/FF for the purpose of reducing the phase errors. Let the second capture point at 4π be θ_i as shown in Fig. 3(b). If i is even, the first capture point at 2π will

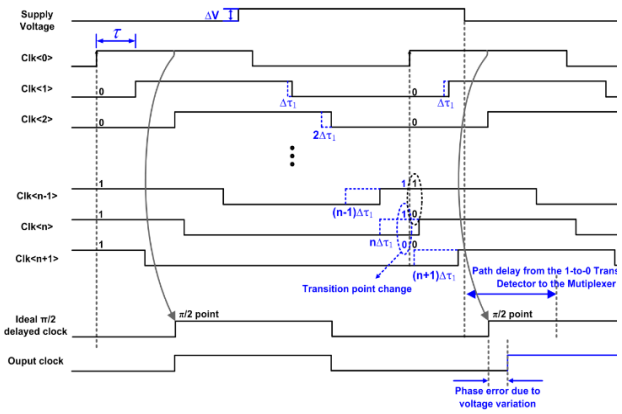


Fig. 4. The supply noise effect with +ΔV variation.

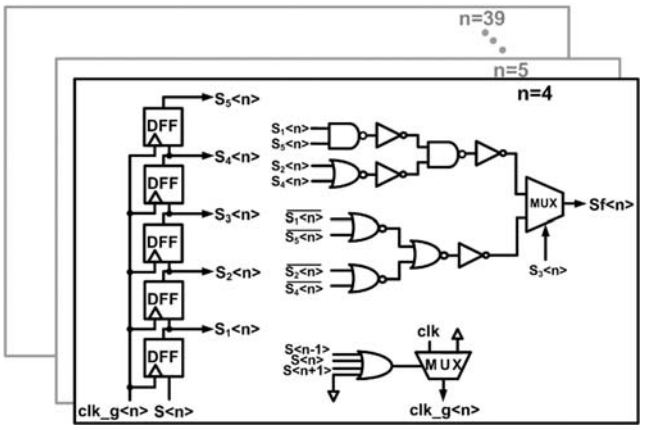


Fig. 5. The supply noise filtering block.

certainly exist in between the three points, $\theta_{i/2-1}$, $\theta_{i/2}$, and $\theta_{i/2+1}$. If i is odd, the first capture point will be in between the two points, $\theta_{(i-1)/2}$, and $\theta_{(i+1)/2}$. These capture points will be used in the noise filtering block and the select signal generator for proper phase selection.

C. Supply Noise Filtering Block

If the power supply experiences a glitch which changes the select signal code, the open-loop all-digital circuits are likely to experience a fatal error. If the power supply voltage experiences a glitch noise of +ΔV, the delay of each delay cell will be changed from τ to τ-Δτ1. As a result, the transition point of the 1-to-0 transition detector will be changed, as shown in Fig. 4. In the case where there is no supply noise, clk<n> will be detected as a transition point by the D/FF and the clock generator will output a π/2 delayed clock. However, in the case where there is a supply noise variation of +ΔV, the variation in the delay of the clk<n> signal is -nΔτ1 and the transition point may be changed from clk<n> to clk<n+1>. Even after the supply voltage returns to normal, the select signal will remain on, because of the path delay from the 1-to-0 transition detector to the output buffer, which may increase the phase error. Similarly, in the case where there is a supply noise variation of -ΔV, the variation in the delay of the signal clk<n> is +nΔτ2 and the transition point may be changed to clk<n-1>. In summary, during the increased (decreased) supply voltage period, the clock generation process adjusts to the modified delay in order to produce the

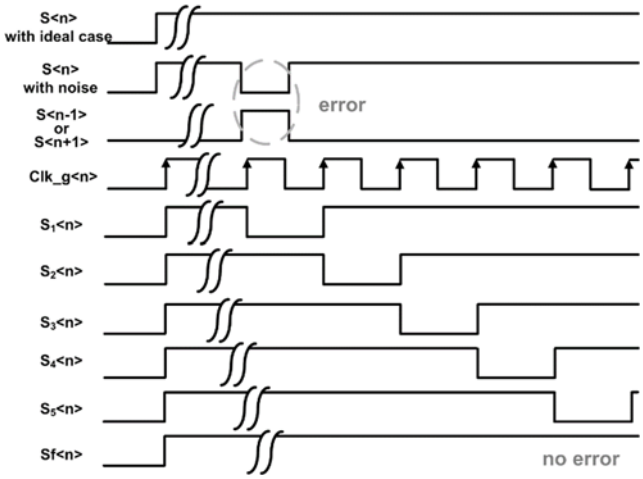


Fig. 6. The timing diagram of noise filtering.

multiphase clocks. However, due to the delay path from the 1-to-0 transition detector to the Output Buffer of the quadrature phase clock generator, the unwanted change of the select signal caused by the glitch noise at the supply will also be applied for a couple of cycles, even after the power supply noise has disappeared. This causes an increase of the phase error, as shown in Fig. 4. To overcome this drawback, the supply noise filtering block is implemented in the proposed quadrature phase clock generator. Fig. 5 is a block diagram of the noise filtering block for each output signal of the 1-to-0 transition detector. The 1-to-0 transition detector output signals, S<4:39>, are transferred to the noise filtering block and the signal clk_g<n> is a gated clock generated by a reference clock. If either S<n> or one of the adjacent signals, S<n-1> or S<n+1>, is high, then clk_g<n> is activated. On the other hand, if neither of them is high, clk_g<n> is not activated. In this way, the gated clock significantly reduces the power consumption for the input bits with no transition. Hence, it can filter supply noise with negligible additional power consumption, although the area penalty is significant. The timing diagram of the noise filtering block is shown in Fig. 6. The five D/FFs generate five output codes, S_1<n>, S_2<n>, S_3<n>, S_4<n>, and S_5<n>, respectively, from S<n> with one clock cycle interval. If more than three signals among the five D/FF output signals are high, Sf<n> will go high. With this filtering operation, the supply glitch noise can be eliminated.

D. Select Signal Generator

The output signals of the noise filtering block feed the select signal generator that generates only one high signal for the purpose of selecting the properly delayed clock. The select signal generator consists of 32 select signal generator cells (SSGC), where one 4-to-1 OR and one 2-to-1 MUX are used, as shown in Fig. 7. For even n, the MUX selects Sf<n> if Sf<n/2-1>, Sf<n/2> or Sf<n/2+1> is high. Similarly, for odd n, MUX selects Sf<n> if either Sf<(n-1)/2> or

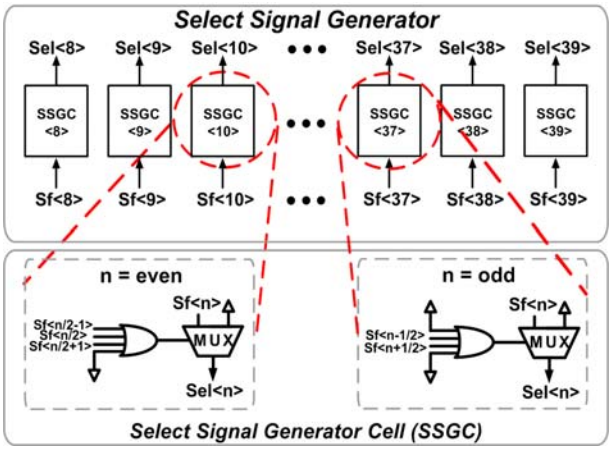


Fig. 7. The block diagram of the select signal generator.

Sf<(n+1)/2> is high. The operating frequency range of the all-digital open-loop non-PLL/DLL type clock generator is limited by the number of delay cells and their control block design. The operating frequency of the proposed quadrature phase clock generator is 2.5 times higher than that of the conventional ones described in [10],[12],[13] and the calculated operation frequency range of the clock generator is explained as follows. When the proposed quadrature phase clock generator operates at the minimum frequency, only two signals (S<19> or S<20> and S<39>) are high, which indicates that the first and second 'high' signals represent the 2π and 4π delayed points, respectively and the clock period is about 39τ/2. When it operates at the maximum frequency, on the other hand, there are eight 'high' signals which represent the 2π, 4π, … , 14π and 16π delayed points, S<4>, S<8>, … , S<19>, … and the clock period is about 8τ/2 as shown in Fig. 8.

$$f_{max} = 1/(8\tau/2), \quad f_{min} = 1/(39\tau/2). \tag{1}$$

$$f_{max}/f_{min} = (39\tau/2)/(8\tau/2) = 4.875. \tag{2}$$

In order to select the proper signal, only the first and second capture points are needed. The second capture point is matched to the proper select signal, while the other signals are filtered at the multiplexer. Using this method, the operating frequency range can be extended by about 5 times.

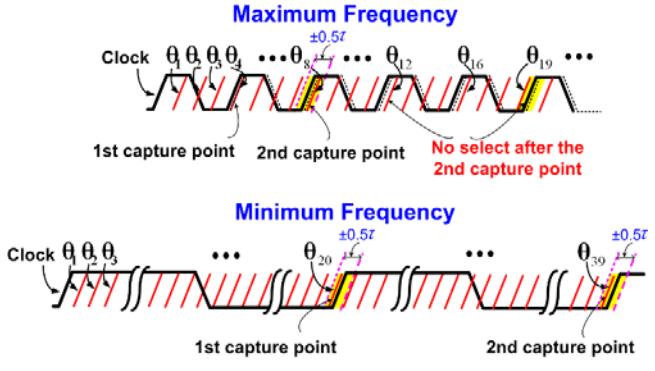


Fig. 8. The operating frequency range of the proposed clock generator.

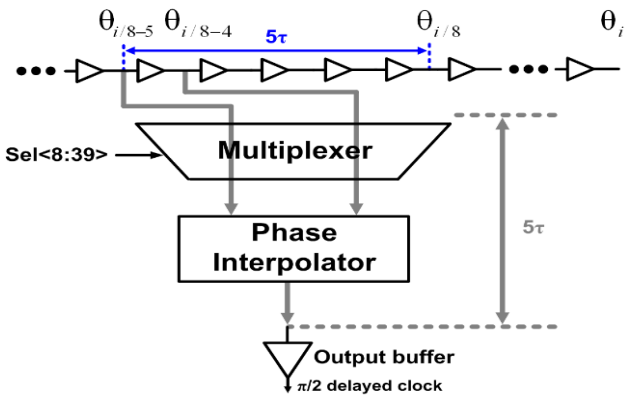


Fig. 9. The delay from the multiplexer to the output buffer compensation.

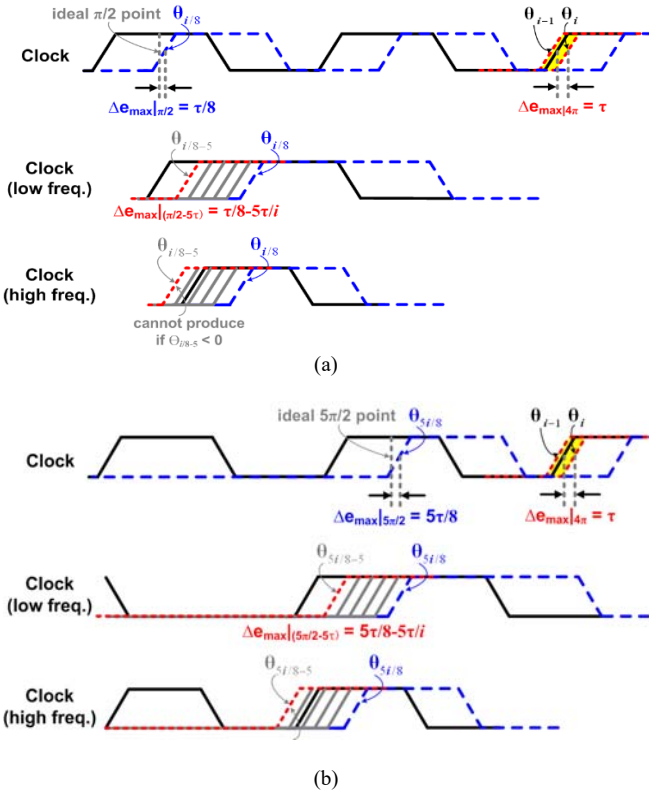


Fig. 10. The π/2 delayed clock selection method: comparison (a) 1/8 of 4π selection and (b) 5/8 of 4π selection.

E. Multiplexer

With the select signals Sel<8:39>, the multiplexer selects the properly delayed clock, which originates from the multiphase signals of the delay line, such as θ_0, θ_1, … , θ_{38}, θ_{39}. The 4π delayed point, θ_i, is checked by the 1-to-0 transition detector and then the π/2 delayed clock can easily be selected by choosing the $\theta_{i/8}$ signal. However, the path delay from the delay line to the output buffer is 5τ under various PVT conditions, as shown in Fig. 9, which is five times bigger than that of the delay cell, τ. To obtain the correct phase at the output, this 5τ delay should be compensated. For example, if the 4π delayed clock and π/2 delayed clock are θ_i and $\theta_{i/8}$, respectively, $\theta_{i/8-5}$ should be chosen, rather than $\theta_{i/8}$, when considering the required 5τ compensation. However, in some

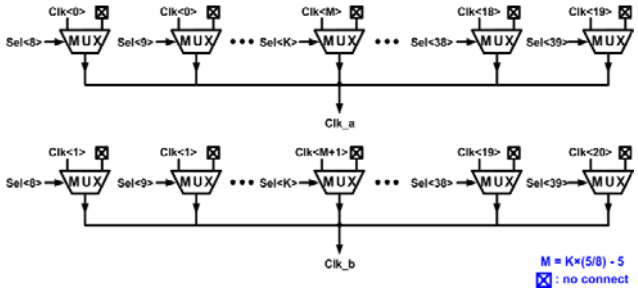


Fig. 11. The multiplexer.

cases, it may be impossible to extract the $\theta_{i/8-5}$ point above a certain high frequency range where i/8-5 has a negative value. To prevent i/8-5 from having a negative value, the maximum operation frequency, f_{max}, is limited to $1/20\tau$, as follows.

The minimum value of i for which (i/8-5) does not have a negative value can be expressed as

$$i/8 - 5 = 0. \quad (3)$$

From (3), we obtain i = 40.
Therefore, to be locked at 4π with 40 delay cells, we have

$$40\tau = 2/fmax, \quad (4)$$

which results in $f_{max}=1/20\tau$ and this constitutes a bottleneck for high-frequency operation.

In addition, the clock generator with this condition needs a lot of delay cells, which results in a large area, large power consumption and large jitter induced by the long delay line. For high-frequency operation, the $\pi/2$ delayed clock can be selected by choosing the $\theta_{5i/8}$ signal instead of the $\theta_{i/8}$ signal, as shown in Fig. 10(b).

In this case, the minimum value of i for which i/8-5 does not have a negative value can be expressed as

$$5i/8 - 5 = 0. \quad (5)$$

From (5), we obtain i = 8.
Therefore, to be locked at 4π with 8 delay cells, we have

$$8\tau = 2/f_{max}, \quad (6)$$

which results in $f_{max}=1/4\tau$ where f_{max} is five times higher than that in Fig. 10(a).

Hence, in the implemented clock generator, a $\pi/2$ delayed clock is generated from the $5\pi/2$ delayed phase by reducing the number of delay cells required, although the maximum output phase error is increased from $\tau/8$-$5\tau/i$ to $5\tau/8$-$5\tau/i$, as shown in Fig. 10(b). If the second select signal is Sel<K>, then Clk<(K×5/8)-5> is the desired signal point. However, Because <(K×5/8)-5> may not be an integer, The M of the desired clock signal Clk<M> is expressed as

$$M = [\, K\times(5/8) - 5\,], \quad (7)$$

* $x = [\,x\,] + \alpha\ (0 \le \alpha < 1)$

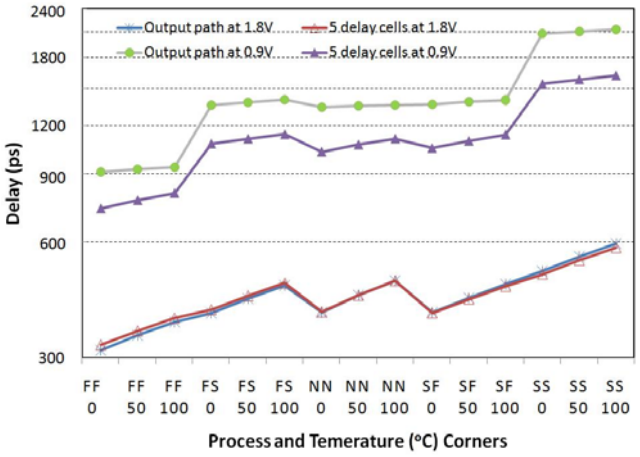
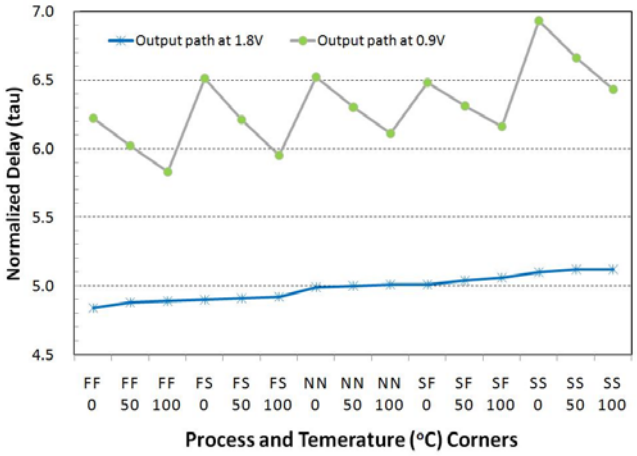
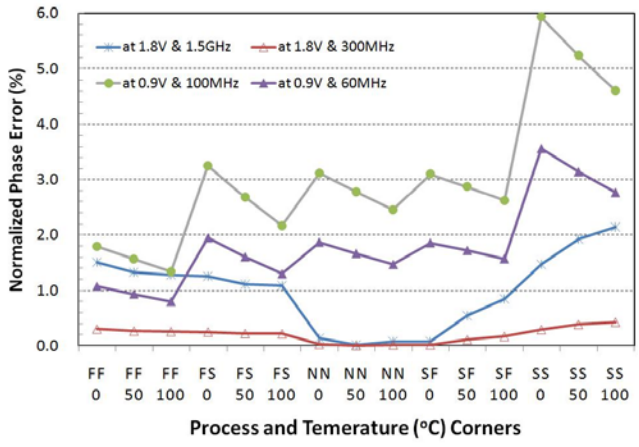


Fig. 12. The simulated delay comparisons of 5 delay cells and output path (MUX to PI) at the supply voltages of 1.8V and 0.9V, respectively.



(a)



(b)

Fig. 13. (a) The output path delay normalized by tau at 1.8V and 0.9V. (b) The normalized absolute phase error at supply voltage of 1.8V and 0.9V at different frequencies.

and the phase interpolator block is implemented. Fig. 11 shows the block diagram of the multiplexer. The multiplexer generates two output signals, Clk_a and Clk_b, whose phase difference is equal to the delay of the delay cell, τ.

The delay variations of 5 delay cells and output path

TABLE I.
Phase error due to delay mismatch.

	1.8 V supply			0.9V supply		
Process corner	FF	NN	SS	FF	NN	SS
Temperature (ºC)	0	50	100	0	50	100
Delay from MUX thru PI (ps)	314.4	435.4	592.4	910.6	1348	2127
Delay of 5 delay cells (ps)	324.5	435.3	578.0	731.6	1070	1614
Normalized delay from MUX thru PI (τ)	4.84	5.00	5.12	6.22	6.30	6.43
Phase error (ps)	10.1	-0.1	-14.3	-179	-278	-703
Normalized Phase error (%)	1.51 @1.5G Hz	0.015 @1.5G Hz	2.15 @1.5G Hz	1.79 @100 MHz	2.78 @100 MHz	4.61 @100 MHz
Normalized Phase error (%)	0.30 @300 MHz	0.003 @300 MHz	0.43 @300 MHz	1.07 @60M Hz	1.67 @60M Hz	2.76 @60M Hz

(MUX through PI) are shown in Fig. 12 and Table I. In Table I, delay variations of only six corners are listed and more data can be found in Fig. 12. The supply voltages were 1.8V and 0.9V, respectively and the y axis in Fig. 12 is log scaled to show the difference in delay at 1.8V more clearly. The output path delay is normalized by the delay amount of one delay cell, τ, and each variation at the supply voltages of 1.8V and 0.9V is shown in Figs. 13(a). The ranges of delay variation are from 4.84τ to 5.12τ at 1.8V and 5.83τ to 6.93τ at 0.9V. Delay mismatches due to PVT variations between 5τ and the delay of output path (MUX through PI) cause a phase error. Normalized absolute phase errors at different operating frequencies are shown in Fig. 13(b). For example, at SS (slow nMOS and slow pMOS), 100°C, and 0.9V supply, the delays of 5 delay cells and output path are 1614ps and 2127ps, respectively as shown in Table I and Fig. 12. Therefore the normalized delay of output path is 6.43τ and the phase error is 703.4ps as shown in Table I and Fig. 13. Normalized phase errors due to different clock periods are shown in Fig. 13(b). Although the difference in delay is large at 0.9V, the percentage phase error is not big because the operating frequency is low at 0.9V. The simulated phase errors caused by 5τ delay mismatch are within 2.1% at 1.5GHz and within 0.4% at 300MHz at normal supply voltage. If the supply voltage is halved, the simulated phase errors are within 2.8% at 60MHz and within 4.6% at 100MHz.

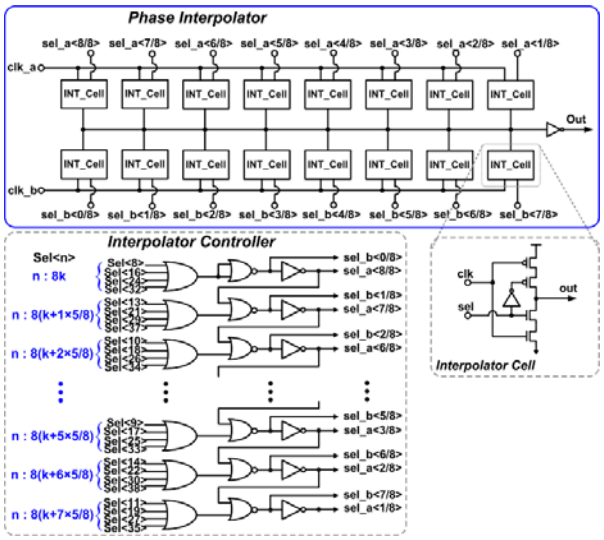


Fig. 14. The phase interpolator.

F. Phase Interpolator

Fig. 14 shows the phase interpolator. The time interval between clk_a and clk_b is the same as the delay of the delay cell, τ. By using the phase interpolator, the resolution of the proposed quadrature phase clock generator is improved to τ/8. The interpolator controller determines the ratio of interpolation between clk_a and clk_b. To achieve an accurate interpolating ratio, each interpolator cell has a slightly different size [8]. Furthermore, only one phase interpolator is used in front of the output buffer to save power and reduce the area. If the second select signal and desired output signal are Sel<15> and Sel<15×5/8-5>, respectively, the multiplexer chooses Sel<9> as clk_a and Sel<10> as clk_b. Finally, the interpolator controller selects sel_a<5/8> and sel_b<3/8> to adjust the interpolation ratio between clk_a and clk_b.

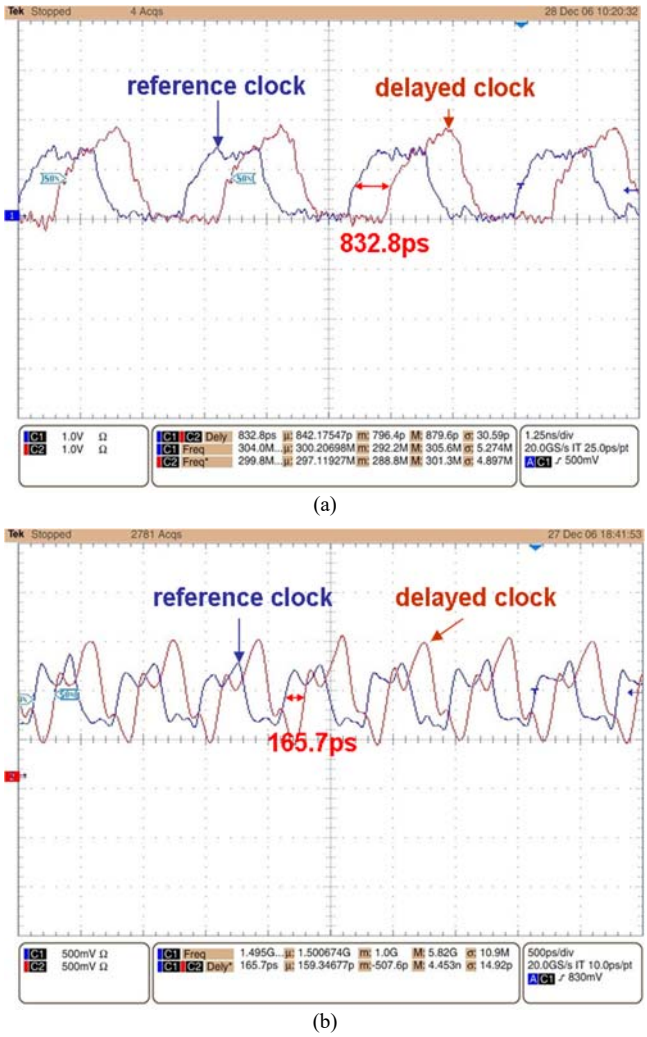
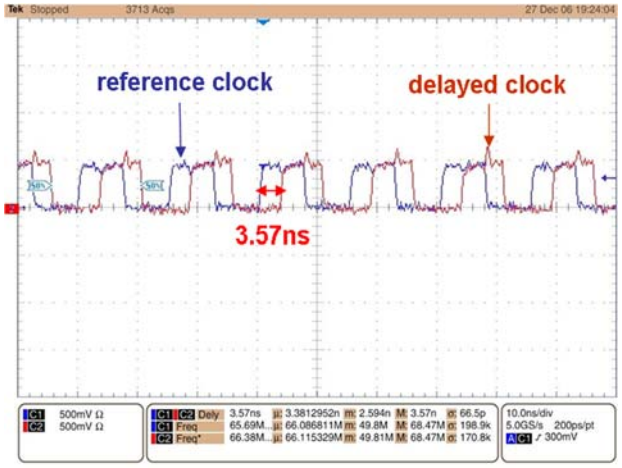
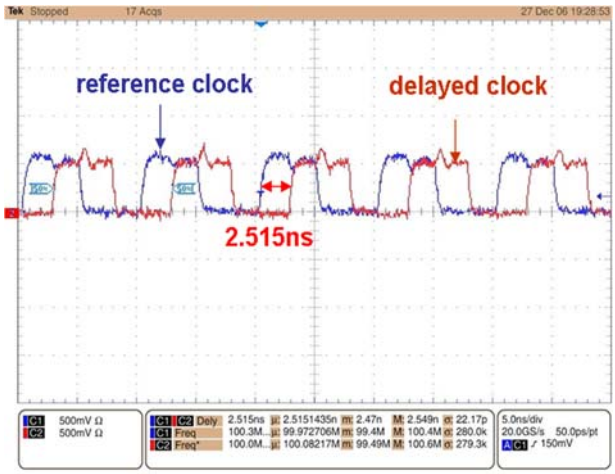


Fig. 15. Measurement results at supply voltage of 1.8V (a) at 300MHz and (b) 1.5GHz.

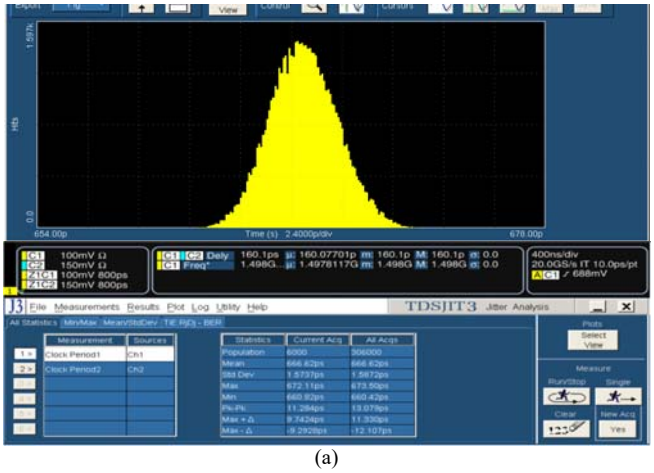


(a)

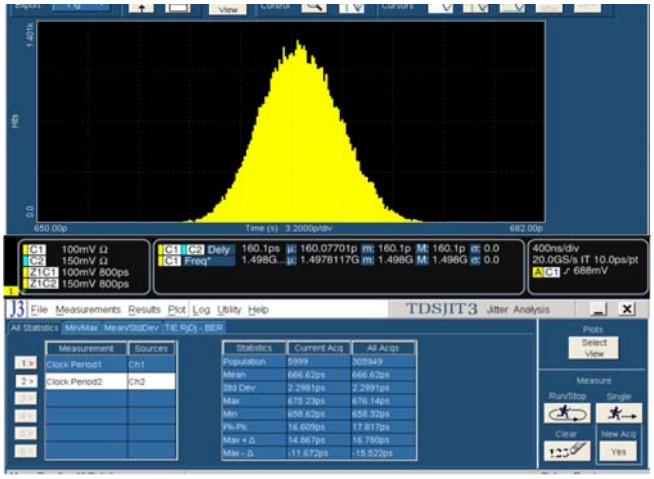


(b)

Fig. 16. Measurement results at supply voltage of 0.9V (a) at 66MHz and (b) 100MHz.



(a)



(b)

Fig. 17. Jitter measurement results at 1.5GHz (a) jitter histogram and characteristics of the input clock and (b) output clock.

III. RESULTS AND DISCUSSION

The proposed quadrature phase clock generator is designed in a 0.18μm 1P4M CMOS technology. The clock generator consumes 31mW at 1.5GHz. The proposed quadrature phase clock generator operates from 300MHz to 1.5GHz at 1.8V, as shown in Figs. 15(a) and (b). The calculated operating frequency ratio using (1) is f_{max}/f_{min}= 4.875. At the boundary of S<8> and S<39>, the 1-to-0 transition detector can detect 7.5τ and 39.5τ, respectively, which extends the operating frequency ratio to 39.5/7.5=5.26. Due to the use of an all-digital scheme, the proposed clock generator can operate at half the normal supply voltage of 1.8V, viz. 0.9V, with an operating frequency range from 66MHz to 100MHz, as shown in Figs. 16(a) and (b). Also, The open-loop scheme enables a lock time of 5 cycles, of which three cycles are for the supply noise filtering block and two cycles for the 4π delayed clock detection and output clock generation, respectively.

The peak-to-peak jitter was measured by a jitter measurement tool, TDSJIT3, in a TDS6154C of Tektronix, and the input and output jitters were found to be 13.1ps and 17.8ps, as shown in Figs. 17(a) and (b) , respectively. The jitter induced from the external clock generator to the delay line is 13.1ps and the increased jitter from the delay line to the output buffer is 4.7ps. The measured jitter histograms and characteristics of the input clock and output clock at 1.5GHz are shown in Fig. 17(a) and (b), respectively. Fig. 18 shows the microphotograph(400μm×120μm) of the proposed quadrature phase clock generator. Table II show the performance characteristics of the proposed quadrature phase clock generator and comparison with other digital clock generators. It shows that the proposed clock generator occupies small area and achieves fast lock with supply noise filtering.

Fig. 18. Microphoto

TABLEII
Performance Summary and Comparison

	ISSCC2005[8]	TCASII2008[10]	TCASII2015[12]	TCASI2017[13]	This work
Process	0.25um CMOS	0.18um CMOS	65nm CMOS	0.13um CMOS	0.18um CMOS
Type	Digital	Digital	Digital	Digital	Digital
Operating frequency	100MHz	300MHz-1.5GHz	400MHz-800MHz	1.5GHz-3.3GHz	300MHz-1.5GHz
Supply voltage	2.5V	1.8V	1.1V	1.2V	1.8V
Noise filtering	X	X	X	X	O
Lock time	8 cycles	1 cycle	38-41 cycles	16-32 cycles	5 cycles
RMS jitter[rms]	4.157 @ 100MHz	-	4.8 @ 800MHz	1.629 @ 3.3GHz	2.3 @ 1.5GHz
Peak to peak jitter[ps]	30 @ 100MHz	7.6 @ 500MHz	26.1 @ 800MHz	12 @ 3.3GHz	17.8 @ 1.5GHz
Active die area[mm^2]	0.096	0.01	0.017	0.0077	0.048
Power consumption	0.243mW@600MHz	7.48mW@600MHz	3.6mW @ 1GHz*	7mW @ 3.3GHz	31mW @ 1.5GHz

IV. CONCLUSIONS

A wide-range, duty-independent, all-digital, qaudrature detector -phase clock generator is proposed. The 1-to-0 transition finds the delayed point at every 2π phase and the select signal generator selects only the 4π delayed point. Hence, wide-range and duty-independent features are obtained. The supply noise filtering block prevents select signal shifting, which makes the proposed clock generator robust to power supply noise. Additionally, the resolution of the proposed clock generator is improved by the phase interpolator. With the open-loop scheme, the quadrature phase clock can be produced within 5 cycles. Specifically, the proposed quadrature phase clock generator is applicable to a microprocessor, which needs dynamic voltage scaling, because it can operate at voltages down to one half of the normal supply voltage of 0.9V.

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