High-efficiency analog front-end design of passive NFC tag based on 65nm

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***Abstract* – The high-efficiency NFC AFE(Analog Front-End) was proposed and implemented in 65nm CMOS process. We proposed the novelty architecture of Envelope Detector which is the most important block in passive mode tag because those generate their own power. The Envelope Detector generating negative voltage and it can generate the negative voltage of -0.68V that is used for body bias and can detect the small voltage swing of 0.5V. The area of the high-efficiency NFD AFE is 1.9mmx2mm and it is very small compared with the conventional NFC AFE. The digital part of NFC is also verified by FPGA board. So the proposed NFC tag is feasible for many applications.**

I. INTRODUCTION

Wireless power transfer has broad applications from mobile phone chargers to biomedical implants [1]. NFC(Near field Communication) is wireless technology that enables the variety of additional services including the transceiver within 20cm at 13.56MHz band and equipped in mobile communication terminal. NFC does not require physical contact, and therefore, it allows more convenient access for information delivery [2]. A number of multi-media equipment like digital camera, personal computer, PMP, and MP3 Player, Samsung pay and white pay have adopted the NFC technology nowadays. [3] ISO(International Organization for Standardization) sets the various standards of NFC and RFID depending on types and modulations based on the standards as shown in TABLE I [3-5].

TABLE I
Modulation specification of 13.56MHz RFID and NFC

ISO Standard	Data rate	Modulation (Reader to Tags)	Modulation (Tags to Reader)
14443 Type A	106kbit/s	ASK 100%	ASK 10% OOK
14443 Type B	106kbit/s	ASK 10%	ASK 10% BPSK
18092 Passive	212kbit/s	ASK 10%	ASK 10%

ASK(Amplitude Shift Keying) modulation on TABLE I is adopted in many communication systems such as NFC and RFID(Radio Frequency Identification) [6]. The ASK modulations is different according to ISO standard types, different circuits should be used when the signal is demodulated from Tag. Tag takes charge of demodulation in analog part and memory block is in charge of digital part. Analogue part has its own power supply when Tag is on as active mode. However, in passive mode, if signal is sent wirelessly form the Reader, the power is self-generated by coupling through antenna made of inductor. Therefore, the role of AFE(Analog Front-End) is very important in passive mode tag. AFE block includes the low-voltage bandgap, the LDO(Low-Drop Out regulator) with the bias-boosted gain stage, and the adaptive dc limiter [2]. This paper proposed the AFE part that can demodulate every signal with ASK 8 ~ 100% modulation using 65nm CMOS process and verified its operation with the measurement of chip. The digital part that can process data are configured using FPGA. The operation of the NFC Tag is verified by linking the packaged chip and the digital part.

The remainder of this paper is organized as follows. In Section II, the proposed high-efficiency AFE of NFC Tag design is presented. The post-simulation results are described in Section III and experimental results are provided in Section IV. Finally, the conclusion is given in Section V.

II. HIGH-EFFICIENCY PASSIVE NFC AFE TAG DESIGN

A. Envelope Detector

The AFE block diagram of the proposed high-efficiency passive NFC Tag is shown in Fig. 1.

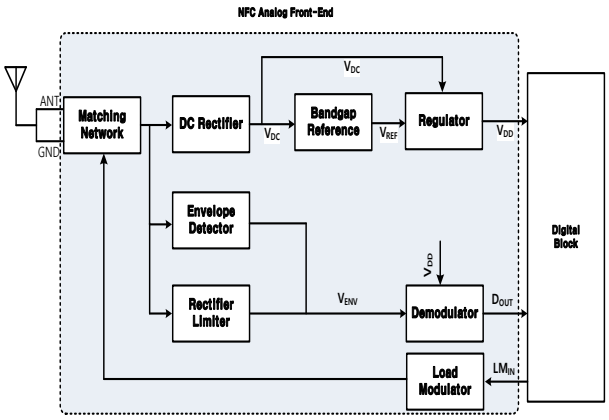

Fig. 1. AFE block diagram of the proposed passive multi-mode NFC Tag

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When the Reader antenna and Tag antenna are within 10cm, signals are transmitted by inductor coupling of Tag antenna. The transmitted signal goes through matching network and is delivered to the DC rectifier and the envelope detector without any loss. The DC rectifier is the first block to incoming signal with amplitude changing depending on ASK modulation ratio is received and corrected by the relatively steady DC 2V voltage. In BGR (Band-Gap Reference), the DC Rectifier output, V_{DC} is applied and steady DC voltage 0.67V is generated without the dependency to the surrounding temperature change. The regulator receives V_{DC} and BGR output, V_{REF}, and creates the steady 1V DC voltage that can operate with the demodulator and digital part. The Envelope detector output, V_{ENV}, and the regulator output, V_{DD}, are entered to the demodulator and the demodulator demodulates the emitted signal to antenna.

Envelope Detector is used in various ways such as ET(Envelope-Tracking), AM radio receiver, and so on [9]. The proposed Negative Voltage Generating Envelope Detector is shown in Fig. 2 [3].

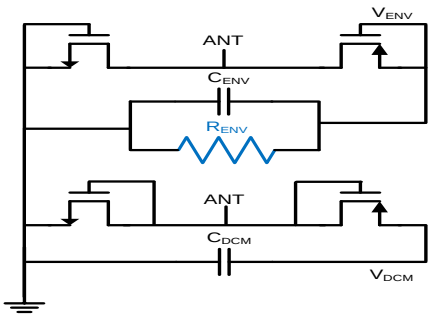


Fig. 2. Schematic of the proposed Negative Voltage Generating Envelop Detector

As the proposed Tag has one input signal form ANT, it was designed to have single input compared with the conventional circuit. Also, the resistance, R_{ENV}, was added beside the capacitor, so the amplitude of V_{ENV} was increased by 55% compared with the conventional Envelope Detector that has no resistance [3], and it can detect the small voltage swing of 0.5V. Also, when ASK modulation is applied in Modulator block and the response signal was sent through antenna, minus voltage called V_{DCM} can be generated to use $-V_{DD}$ to increase the output amplitude. After the simulation, maximum V_{DCM} is about 0.68V.

B. Voltage Limiter

The NFC Signal of 13.56MHz is received via the NFC antenna and generates the DC voltage through the DC Rectifier. The DC Rectifier in this paper is the Voltage Multiplier structure and it is composed of 4 stages to increase the distance between NFC Reader and NFC Tag. It could be possible to generate the stable DC voltage even though low voltage is applied. But if the distance between the NFC Reader and NFC Tag is in short and tag generates the large DC voltage, it may cause damage to the internal circuitry like Bandgap Reference and LDO Regulator. The Voltage Limiter is required to prevent damages to the internal circuit and its schematic is shown in Fig. 3.

When the output voltage of DC Rectifier is lower than the sum of the threshold voltage with M2, M3, M4 and the current flows through R, so it turns on M1. The size of the NMOS which is turned on is large when the current is discharged.

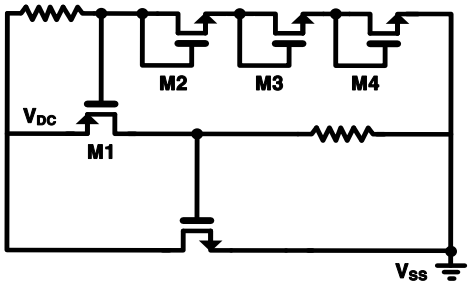
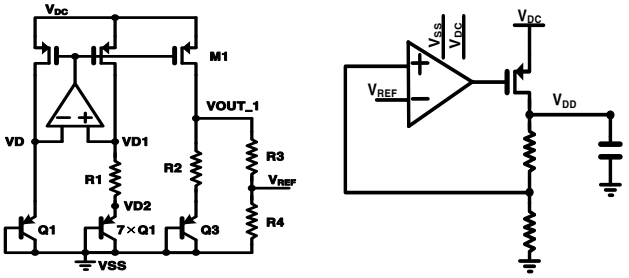


Fig. 3. Schematic of the Voltage Limiter

C. Bandgap reference and regulator

The conventional circuit of BGR and Regulator was used in this design, and those circuits were modified suitable for 65nm process and its schematics are shown in Fig. 4 [11]. The amplifier used in BGR and regulator was designed to have two amplification stages and the PNP transistor used in BGR is implemented in CMOS process using N-well.

Because the regulator output is easily changed according to the external temperature and environment, the output of the voltage Multiplier (VDC) is inappropriate as the power source for the internal circuit. The BGR circuit is suitable, because the output voltage is not sensitive to the changes in external temperature and environment.



(a) (b)

Fig. 4. (a) Schematic of BGR (b) Schematic of LDO Regulator

The LDO regulator is a circuit that provides accurate and stable DC voltage with small difference between input voltage and output voltage. The circuit consists of pass elements, the error amplifier, the reference circuit, and the feedback network. The regulator uses the bandgap reference V_{REF} to provide the stable DC voltage.

D. Demodulator

The demodulator used the conventional circuit in this design and its schematic is shown in Fig. 5 [11]. In Fig. 5, V_{ENV} is the first input but starts to operate after the regulator output, V_{DD}, is entered. V_{REF} goes through the unit gain buffer and is the input to the amplifier and Schmitt trigger block. V_{ENV} goes through RC filter and only the rising edge and falling edge signals are entered to the amplifier [11]. The rising edge and falling edge are entered to the Schmitt trigger block and the Schmitt trigger demodulates them into square wave [11].

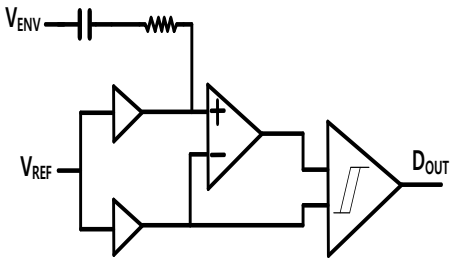


Fig. 5. Schematic of demodulator

E. Load Modulator

The Load Modulator circuit is shown in Fig. 6. It is composed of a NMOS and a MOS Capacitor. When the gate of the NMOS receive, the response signal of 847KHz from the Digital Block, it is connected the drain of the MOS connected antenna with the source of the MOS connected MOS capacitor, and it changes the amplitude of Reader signal.

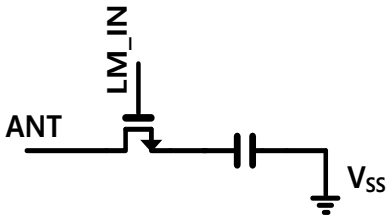


Fig. 6. Schematic of Load Modulator

F. Power-On Reset circuit

The Power-On Reset circuit used in this work is shown in Fig. 7. The circuit for resetting the Digital Block after sending data and the response data between the Reader and the Digital Block is the Power-On Reset. It is composed of MOS Capacitor and Schmitt Trigger.

The output voltage of the DC Rectifier was used as the supply voltage of the Power-On Reset. The current mirror to control the amount of current was used on the Stage-3.

Since the input of the Schmitt Trigger and the MOS Capacitor is connected, the current applied through the current mirror determines the reset wait time until the capacitor charging voltage goes the high switching point of the Schmitt Trigger.

After the reset, the data does not come from the Reader and the MOS Capacitor enters discharge state. This makes the switching point of the Schmitt Trigger pull down, it is possible to reset the high switching point when sending the data again.

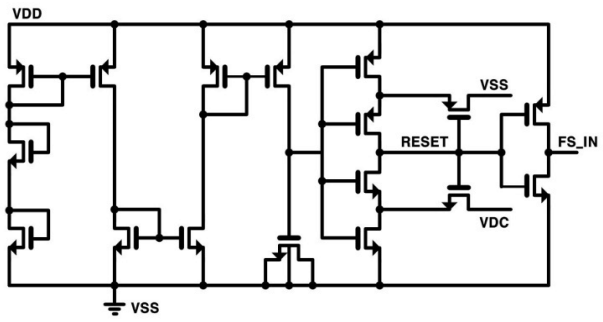


Fig. 7. Schematic of Power-On Reset

G. Digital block

The digital block receives the signal passed through the ASK demodulator, converts thoes into data stream, and determines the response signal. It modulates the response signal, and transmits data to the load modulator. In this paper, FPGA is used to verify digital part with the designed NFC Analog Front-End. The digital block diagram for data processing is shown in Fig. 8.

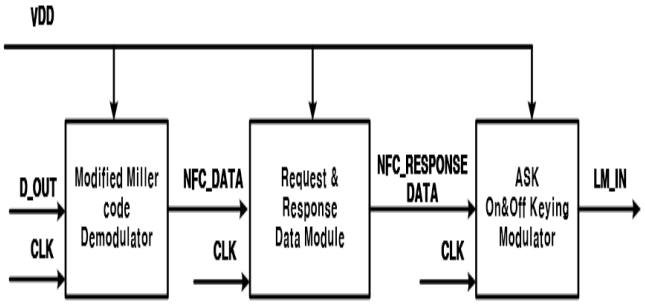


Fig. 8. Block diagram of NFC digital part

In 14443 Type A standard, the signal transmitted from the Reader to the Tag sends 1-frame data(8bits) as modified Miller-coded signal. For this reason, the digital block needs to convert the data through the Modified Miller-coded demodulator. The modified Miller coding signal discriminates 1 bit of data as 1 and 0 according to the position of the pulse appearing in 1 bit cycle. Fig. 9 shows the modified Miller coding signal [12].

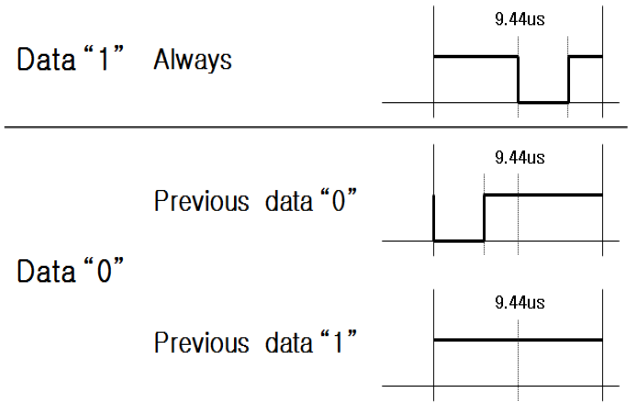


Fig. 9. Modified Miller Code Signal

The modified miller coded signal always shows data '1' when the pulse signal comes after the half period for 1 bit period. However, the data '0' is different according to the value of the previous data. If the previous data value is '1', the pulse is not displayed for 1 bit period. If the previous data value is '0', the pulse signal comes before the half period for 1 bit period. One frame is composed of 8 bits. MSB and LSB are represented by SOF(Start Of Frame) and EOF(End Of Frame), which indicate the start and end of data. The Modified Miller code Demodulator determines the SOF and EOF of the data and demodulates the signals from SOF to

EOF into data and stores it. The stored data is transferred to the next digital block, the Data Module.

The Data Module compares the data defined in NFC Protocol with the data received and defines the data and determines the corresponding response data. Unlike the input data, the response data consists of 2 frames and sends total 16 bits of data. The response data is also transmitted in the data defined in NFC protocol, and the tag ID and information are transmitted [12]. The response data is also modulated and transmitted to the load modulator of the AFE. The modulation of the response data is modulated by the ASK OOK(On & Off Keying) Modulator of the digital block. The modulation scheme of the response data is shown in Fig. 10.

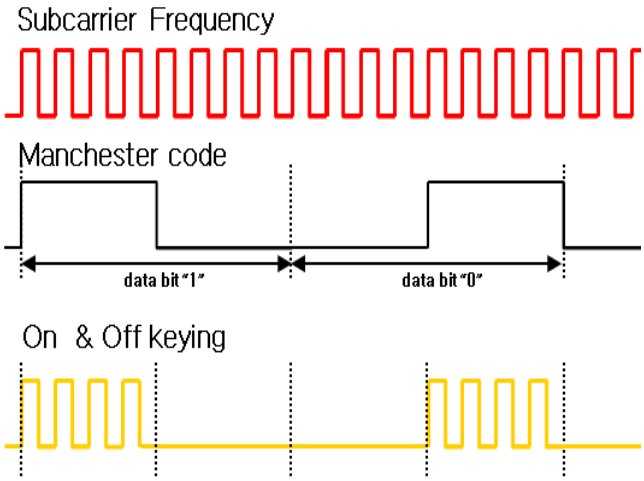


Fig. 10. Scheme of response data modulation

The response data is modulated with the Manchester code. In the Manchester code, when one bit is transmitted, the transition of voltage occurs at the center of each bit time. Therefore, the receiver can see the transmission speed only by looking at the transmitted signal. '1' is expressed as High to Low, and '0' is expressed as Low to High. The modulated response data is generated by signal transmitted to the load modulator through the 847KHz subcarrier frequency and the OOK modulation scheme. The subcarrier frequency is output when the modulated response data is high, and when it is low, output is 0. The modulated OOK signal is transmitted to the LM_IN of the AFE load modulator and the load modulator transmits the response signal to the reader via the antenna.

III. SIMULATION RESULTS

The proposed high-performance passive NFC Tag was designed using 65nm CMOS process and CADENCE Spectre was used for the verification.

The simulation results of the proposed Negative Voltage Generating Envelope Detector depending on ASK modulation value are shown in Fig. 11. By the simulation, it shows that 8 ~ 30% ASK modulation specifications were satisfied using the proposed NFC Tag.

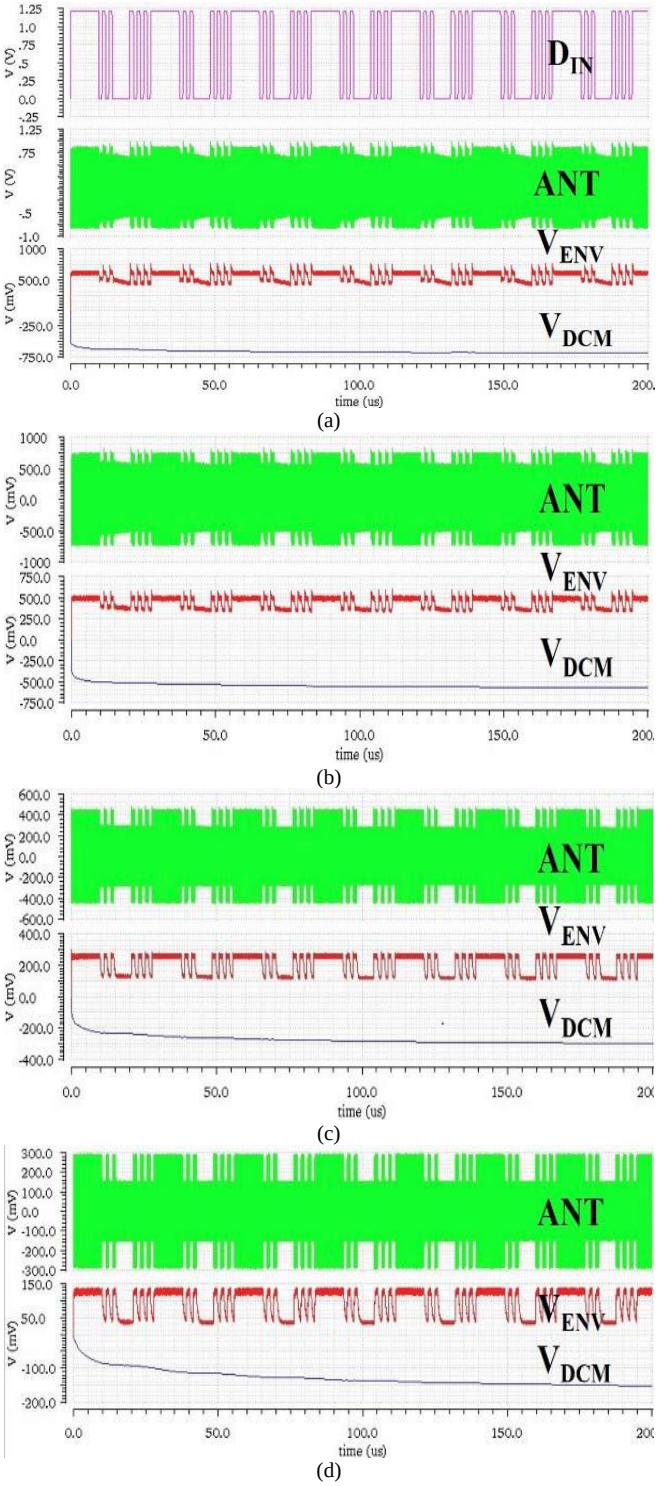


Fig. 11. Simulation result of VENV and VDCM versus ASK modulation ratio (a) 8% (b) 10% (c) 20% (d) 30%

Fig. 12 shows the simulation result between the envelope detector with and without resistance R_{ENV}. According to the simulations, it showed that the proposed circuit operates better compared to the previous works [3].

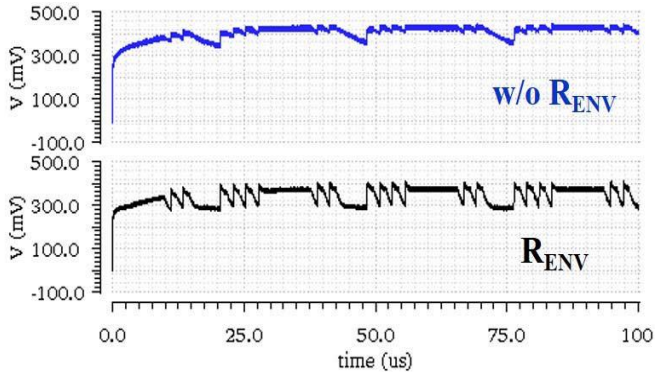


Fig. 12. Simulation comparison result of the proposed Negative Volta ge Generating Envelope Detector and conventional Envelop Detector

The simulation results for the operation of BGR, Regulator, and Demodulator are shown in Fig. 13. According to the simulation, it shows that the waveform was demodulated correctly by constant V_{REF} voltage.

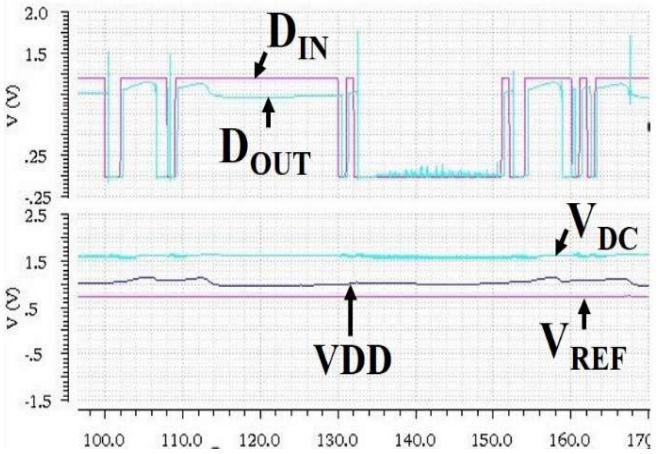


Fig. 13. Simulation result of Demodulation

Fig. 14 is the simulation results of the Power supply consist of DC Rectifier, Bandgap Reference, LDO Regulator and Power-On Reset.

The ASK signal of Modified Miller coding, RX_IN coming from the Reader goes in the DC Rectifier. It makes the output voltage of the ASK signal (RX_IN) which is entering low at this simulation.

Power-On Reset and Bandgap Reference is supplied with the output voltage of DC Rectifier (V_{DC}). The Bandgap Reference outputs the constant voltage (V_{REF}) and the Schmitt Trigger operates the reset function (POR_RST) after passing the charging time of the high switching point of the Schmitt Trigger.

After the LDO Regulator receives the V_{REF} from the Bandgap Reference, VREG could be obtained through the Error Amplifier operation. It is used as the Power supply voltage(VDD) of the NFC Analog Front-End.

Fig. 15 is the simulation result of Demodulation operation. The ASK signal of Modified Miller coding, RX_IN coming from the reader enters the proposed Envelop Detector for ASK 8 ~ 100% Modulation. RX_IN is the modulated 100% ASK in this simulation. VREC is the output of the Envelope Detector. VREC is passed through the filter, which enters the one input of the Comparator. The other input of the Comparator receives the VREF, the Comparator output (OUT_FILTER) is generated around the VREF. The comparator receiving the OUT_FILTER and VREF is connected to the Schmitt Trigger, which produces the demodulated Signal, OUT_DEMOD.

OUT_DEMOD goes to the interfacing buffer for the Digital Block. This operation is done by the PAD in this design. The Digital Block receives the data through the operation of demodulation and sends the response signal.

The Response signal of Manchester coding has the carrier frequency of 847KHz. Receiving the response signal can watch that the amplitude of the RX_IN changing at the rate of 847KHz.

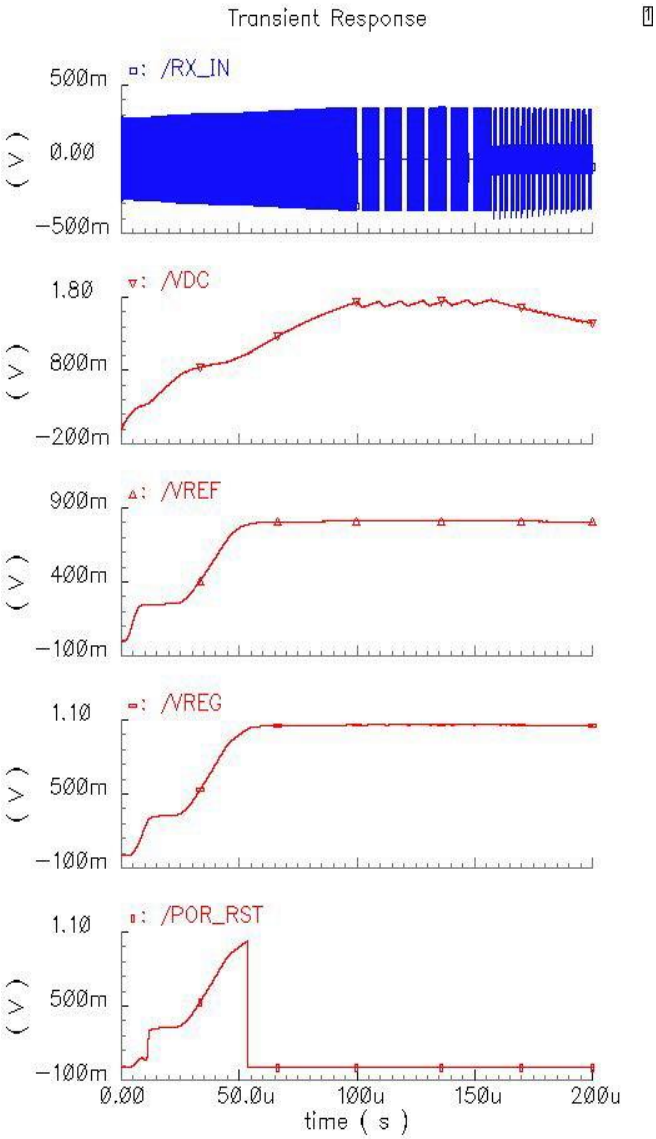


Fig. 14. Simulation result of Power Supply

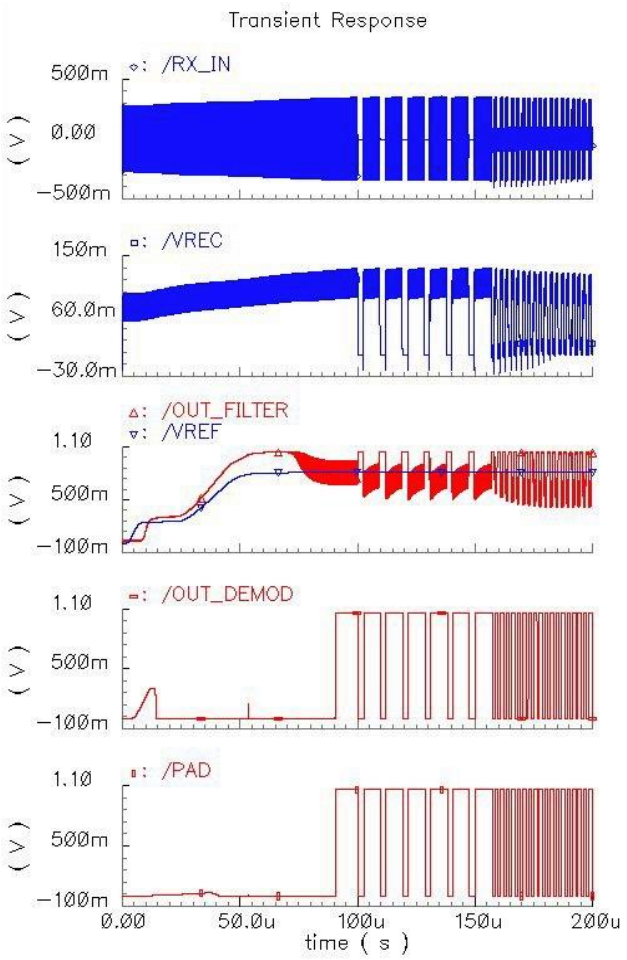


Fig. 15. Simulation result of Demodulation

IV. MEASUREMENT RESULTS

A. on-wafer measurement

The chip measurement was conducted using the probing test process in probe station and connection with the antenna is implemented with the resonant frequency of 13.56MHz. The size of the implemented ship is 1.9mm x 2mm and the chip microphotograph is shown in Fig. 16.

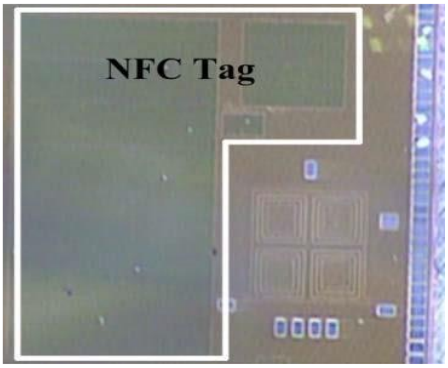


Fig. 16. Chip microphotograph

The proposed NFC AFE receives the signals from the Reader antenna by connecting the antenna which should be placed within 10cm distance. The Reader sends the regular signals for Tag with the programmed communication protocols depending on ISO standard, the different waveforms with ASK 8% to 100% could be sent. The pictures of chip measurement and test result are shown in Fig. 17 and Fig. 18 respectively.

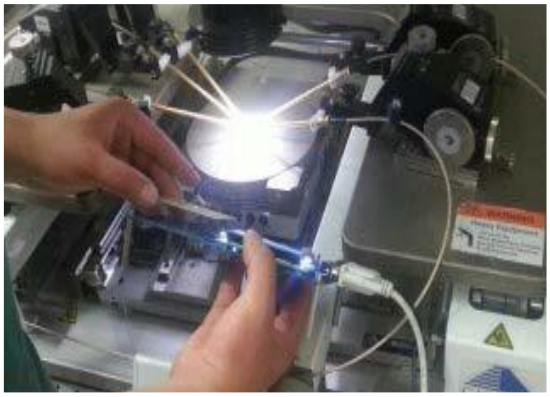
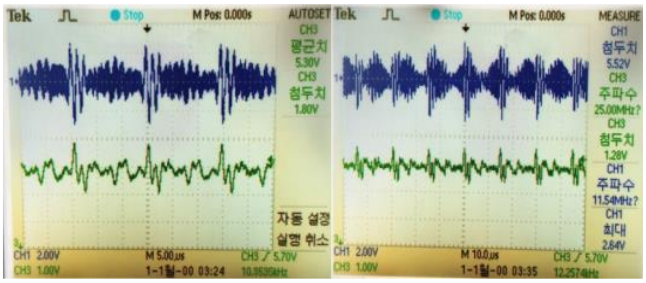


Fig. 17. Measurement environment of the proposed high performance NFC AFE



(a) (b)

Fig. 18. Measured waveforms of high performance NFC AFE versus ASK modulation rate of reader (a) 30% (b) 50%

After the chip measurement, it shows that the demodulation operation is verified correctly using the designed chip.

B. chip measurement

The package measurement was performed to the package and the FPGA, and the reader signal was input via the antenna. By implementing the operation of the digital block through the FPGA, NFC AFE was verified with digital block. The chip measurement environment and test result are shown in Fig. 19 and Fig. 20 respectively.

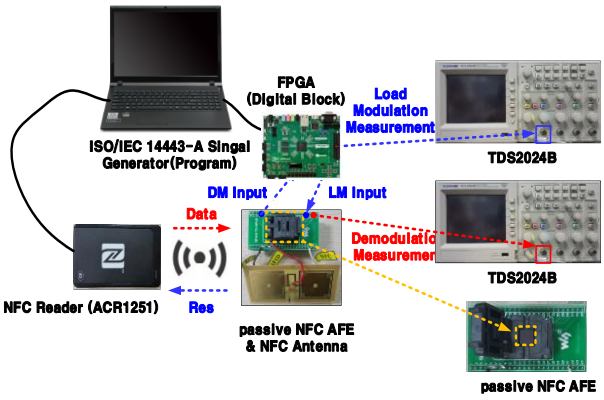
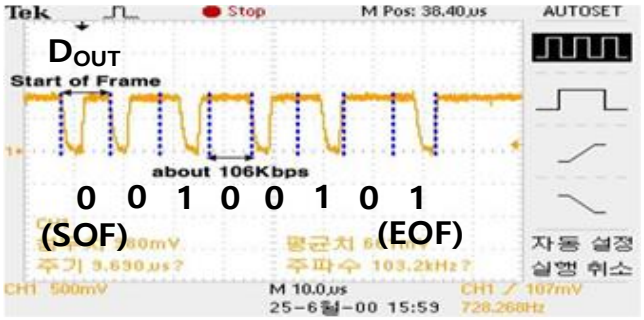
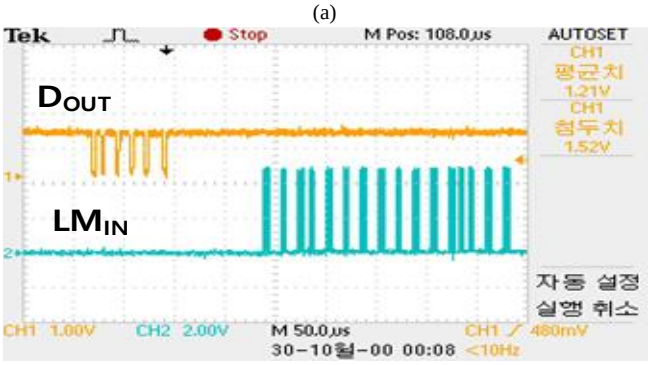


Fig. 19. Measurement environment of the NFC AFE package



(a)



(b)

Fig. 20. (a) Measured of NFC AFE ASK demodulator signal (b) measured of FPGA response signal

After the chip measurement, it shows that the proposed NFC AFE operation is verified using the packaged chip.

V. CONCLUSIONS

The high-efficiency passive NFC AFE is proposed and implemented in 65nm CMOS process. We proposed the novel architecture of Envelope Detector that is most important block in passive mode Tag, because those generate their own power. The Negative Voltage Generating Envelope Detector is proposed and it can generate the negative voltage of -0.68V that is used for MOSFET body bias. Also it can detect the small voltage swing of 0.5V. The digital blocks capable of data processing were implemented in FPGA and is used for NFC AFE verification. The operation of the NFC AFE was verified on-wafer and the packaged chip in test environment. The area of the NFC AFE is 1.9mm x 2mm and it is very small compared with the previously reported NFC AFE.

Since the proposed passive NFC AFE Tag has high efficiency in power and area, it is feasible to use the proposed tag for NFC applications for various wireless communication systems.

ACKNOWLEDGMENT

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