Implementation of RVDT Signal Conditioner Based-on Costas Loop

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***Abstract* - A rotary variable differential transformer (RVDT) shows superior performance compared with the conventional rotation detection sensor. In this paper, we propose a RVDT signal conditioner based on Costas loop. The proposed RVDT signal conditioner applying digital signal processing techniques has an advantage that no additional circuit for phase correction is needed. We implement the proposed RVDT signal conditioner using Magna Chip/SK Hynix 180 nm CMOS process. The proposed signal conditioner is successfully verified in a test environment which is implemented by using a FPGA board and Matlab. The proposed signal conditioner shows a processing time of 0.045 seconds to demodulate the message signal at the sampling frequency of 160 kHz. The area of the proposed signal conditioner is 195470.7 in the number of equivalent gates and a total power dissipation of 47.4 mW at a power supply voltage of 1.8 V and the operating frequency of 24 MHz is achieved.**

***Keywords*— DSP, LVDT, PLL, RVDT**

I. INTRODUCTION

Systems that convert input signals to useful output signals play an important role in industries requiring high-precision, non-fault-tolerant durability equipments. Especially, the system using the change of the electric force and the magnetic force is influenced by the electromagnetic wave generated from the outside. In high-precision system devices, electromagnetic waves are shielded and used so as not to be sensitive to such external environment changes. These magnetic conversion system devices include a linear variable differential transformer (LVDT) and RVDT that measure linear displacement and angular displacement, respectively. The advantage of RVDT is that it has excellent durability from vibration, impact, water, oil, dust and so on. In addition, RVDT is widely used in industrial facilities because reliability can be secured by using non-contact structure. The RVDTs are used in various precision control systems that require an external signal conditioner because the angular displacement of the RVDT sensor must be converted into an electrical signal. Typically, an RVDT analog signal conditioner consists of a separate module configured above a printed circuit board (PCB) using commercial passive elements. Recently, digital signal conditioners that can be embedded in RVDT sensors are being researched. [1][2][3][4]

The RVDT consists of a primary coil, a secondary coil and an eccentric rotor. Sine waves of different magnitudes are generated in the primary and secondary coils according to the rotation of the rotor. Therefore, the rotation angle can be detected by comparing the phase differences of the first and second sinusoidal waves. However, there may be the errors in the location of the rotor due to the phase mismatch error between the waves. In order to compensate the phase error, several methods have been proposed. This paper presents a Costas loop based RVDT signal conditioner, which finds the rotational information of the core from the output signal of a RVDT. This paper is organized as follows. In Section 2, we describe the Costas loop algorithm. In Section 3, we present simulation results and circuit verification results for the RVDT digital signal processor, and finally show some improvements in the conclusion.

II. ALGORITHM

An RVDT is an encoder sensor that outputs the binary position code or gray code high precision position data by converting the angle of one rotation from 0 to 4047 as an absolute position detector. As shown in Fig.1, RVDT can detect the current rotational position by detecting the phase difference between the sinusoidal waves of the primary coil and the secondary coil according to the rotation of the eccentric rotor by using the magnetic induction principle of the transformer. In the RVDT, the four poles are reversely wound around the primary and secondary coils. As the core rotates, it becomes possible to measure the displacement by the change of the mutual inductance induced in the primary and the secondary coils. [2][4]

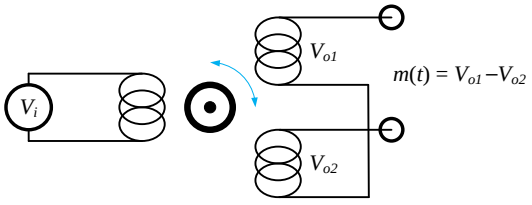

Fig. 1. RVDT structure

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In the RVDT, the input signal the position signal of the rotor, $m(t)$, is modulated with the carrier signal $\cos(w_c t)$ and transmitted to the receiver, where the phase changes due to the external environment and the delay time. The receiving section performs demodulation using the Costas loop to compensate this phase change. As shown in Fig. 2, Costas loop consists of a numerical control oscillator (NCO), three LPFs (low-pass filter) and three multipliers. [5][6]

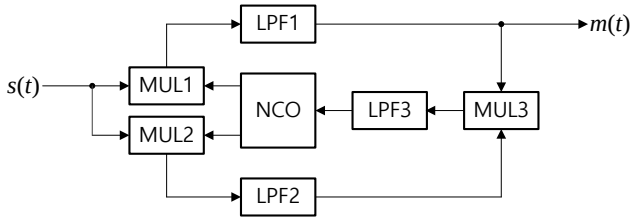


Fig. 2. Costas loop structure

Input signal $s(t)$ of a Costas loop is

$$s(t) = m(t)\cdot\cos[w_c t + \Theta_i(t)]. \quad (1)$$

The NCO has two output signals that have the same frequency as the carrier signal and the phase differences of zero and 90 degrees, respectively, as follows:

$$2\cos[w_c t + \Theta_o(t)] \quad (2)$$

$$2\sin[w_c t + \Theta_o(t)] \quad (3)$$

In order to compensate the phase difference, the signal output from the NCO is multiplied by the input signal. Outputs of MUL1 and MUL2 are calculated as follows:

$$\begin{aligned} &m(t)\cdot\cos[w_c t + \Theta_i(t)]\cdot 2\cos[w_c t + \Theta_o(t)] \\ &\quad = m(t)\cdot\cos[2w_c t + \Theta_i(t) + \Theta_o(t)] \\ &\quad + m(t)\cdot\cos[\Theta_i(t) - \Theta_o(t)] \end{aligned} \quad (4)$$

$$\begin{aligned} &m(t)\cdot\cos[w_c t + \Theta_i(t)]\cdot 2\sin[w_c t + \Theta_o(t)] \\ &\quad = m(t)\cdot\sin[2w_c t + \Theta_i(t) + \Theta_o(t)] \\ &\quad + m(t)\cdot\sin[\Theta_i(t) - \Theta_o(t)] \end{aligned} \quad (5)$$

The high-frequency components of (4) and (5) are removed by low-pass filtering (4) and (5) as follows.

$$i(t) = m(t)\cdot\cos[\Theta_g(t)] \quad (6)$$

$$q(t) = m(t)\cdot\sin[\Theta_g(t)] \quad (7)$$

where $\Theta_g(t)$ is $\Theta_i(t) - \Theta_o(t)$. In MUL3, $i(t)$ and $q(t)$ are multiplied and low-pass filtered.

$$\begin{aligned} &m(t)\cdot\cos[\Theta_g(t)]\cdot m(t)\cdot\sin[\Theta_g(t)] \\ &\quad = (1/2)(\mathrm{k} + \Phi(t))\cdot\sin[2\Theta_g(t)] \end{aligned} \quad (8)$$

Low-pass filtering (8) produces

$$(1/2)(\mathrm{k})\cdot\sin[2\,\Theta_g(t)] \cong \mathrm{k}\Theta_g(t) \quad (9)$$

The message signal $m(t)$ is decoded by making the loop converge the Θ value to zero, where the NCO generates a signal with the same frequency as the input signal. Therefore, since the phase is automatically corrected by applying the feedback using the NCO, there is an advantage that an additional circuit for compensating the phase error is not necessary.

III. IMPLEMENTAOIN

A. Simulation

The above Costas loop is simulated by using MATLAB as in Fig. 3. The sampling frequency of the filter is 160 kHz and the number of the bits in the output of the NCO is 12 bits, which is the resolution of the Analog to Digital Converter (ADC). The system clock is generated by dividing 24 MHz to 2.4 MHz and is used for the ADC. The clock is also used for sine wave generation by dividing to 160kHz.

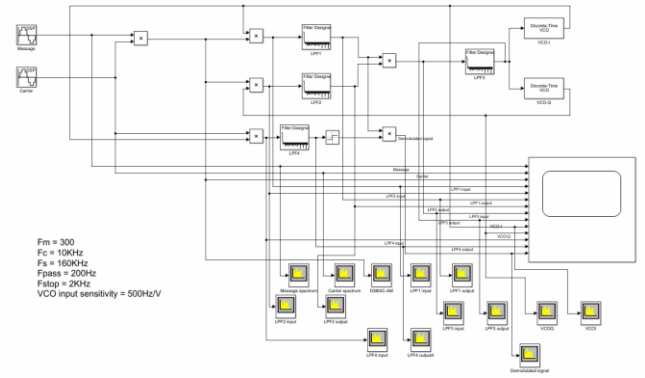


Fig. 3. Costas loop model using Matlab

For the simulation of Fig. 3 the sine wave in Fig. 4, which is a sine wave with a frequency of 300 Hz, is used as message signal.

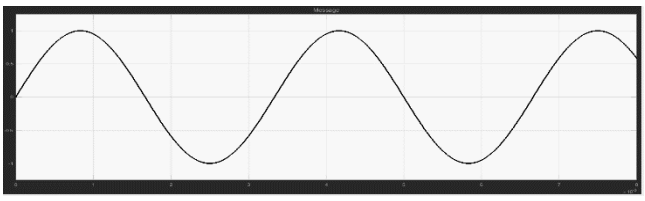


Fig. 4. Message signal

As shown in Fig. 5 and Fig. 6, the carrier signal has a frequency of 10 kHz and is multiplied with the message signal $m(t)$ producing the modulated signal.

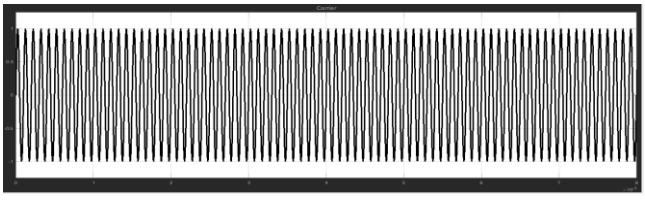


Fig. 5. Carrier signal

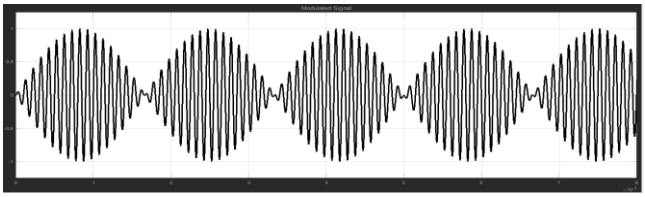


Fig. 6. Modulated signal

In order to demodulate the input signal in the Costas loop, the NCO generates $2\cos[w_c t + \Theta_o(t)]$ and $2\sin[w_c t + \Theta_o(t)]$. The outputs of LPF1 and LPF2 are $i(t)$ and $q(t)$, respectively. Then, these values are multiplied and passed through LPF3. As shown in Fig. 7, it can be seen that the phase difference of the Θ value converges to zero as time passes.

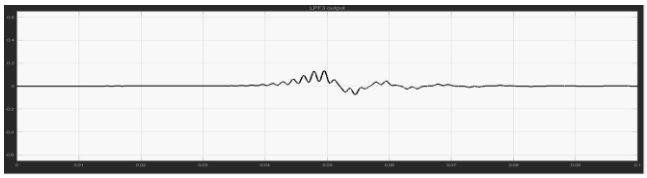


Fig. 7. LPF3 output

The signal passed through LPF1 is a demodulated message signal. It can be seen that this signal is demodulated after 0.045 seconds as shown in Fig. 8.

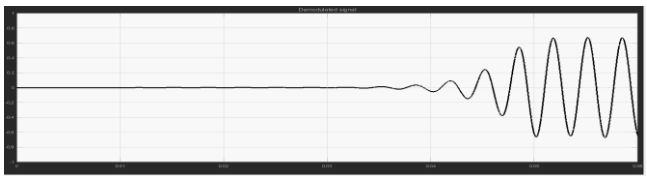


Fig. 8. Demodulated signal

B. Implementation

The RVDT digital signal processor based on the Costas loop is implemented in the following order. Based on the modeling results described above, the block diagram of the RVDT signal processor is described shown Fig.9 using VerilogHDL.

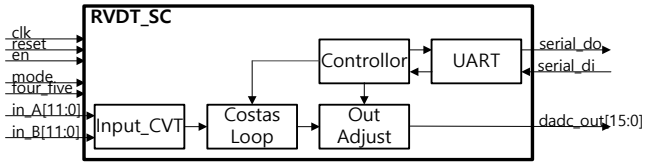


Fig. 9. Block diagram of proposed signal conditioner

When the 12-bit input is received from the input conversion block (Input CVT), it is converted to a 4-wire type signal in the case when a 5-wire type signal is applied. Receiving a 24MHz clock from outside, a clock divider generates 2.4 MHz and 160 kHz clocks. In the Costas loop block, the phase adjustment algorithm is executed to correct the phase error. By analyzing the loop coefficient that adjusts the output value of the low-pass filter that is input to the NCO, the phase locking time is reduced. Since it is impossible to set Θ to 0 completely in hardware, the threshold value is used. When the threshold value is large, the locking time is shortened, but the phase difference correction may be inaccurate. In the opposite case, the locking time may become longer. Therefore, it is necessary to adjust both the magnitude of the threshold value and the loop coefficient to change the locking time. The control block sets the gain and the offset used in the output adjustment block. For the linearity correction, the fifth order curve-fitting is used, where the coefficients are set by using the UART from the outside. The output adjustment block compensates the output by applying the gain and the offset set by the linearity correction block and the control block. All the control parameters and the coefficients are set by serial communication method using UART. The corrected digital output value is converted to serial data and output via the UART.

After the hardware simulation is verified, synthesis is performed using Synopsys' Design Complier using a 180nm standard CMOS process and TABLE I summarizes the implementation result. The total area of the synthesis result is 195470.7 represented as the number of equivalent gates, which is a NAND gate. After that, we extract the netlist from the synthesis result, which is the input to Timing-Simulation using Modelsim and P&R (Place & Route) using Synopsys's Astro. Fig. 10 shows the layout after P&R process. Thereafter, DRC (Design Rule Check) and LVS (Layout Versus Schematic) are performed. STA (Static Timing Analysis) is performed using Prime Time. Fig. 11 shows the message signal waveform and the post-simulation output signal waveform.

TABLE I. Implementation Result

Process Technology	CMOS 180 nm 1P6M	
Package	MQFP 208pin	
Supply Voltage	3.3V/1.8V	
Operating frequency	24 MHz	
Sampling frequency	160 kHz	
Area(GC)	195470.7 (100%)	
	Input_CVT	432.3 0(0.2%)
	Contrillor	6071.5 0(3.4%)
	Costas_Loop	142549.9 (72.9%)
	Out_Adjust	44901.1 (23.0%)
	UART	885.9 0(0.5%)
Power consumption	47.4 mW	
Data bit width	Input: Output: Filter:	12 bits 12 bits 16 bits

* The gate count (GC) is equivalent 2-port NAND-gate count.

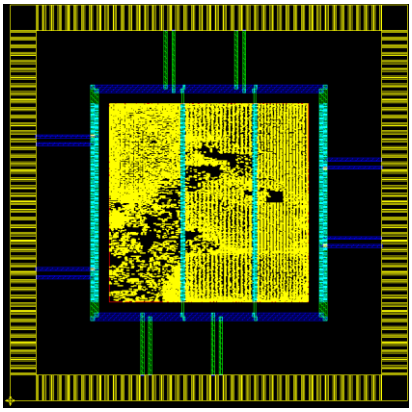
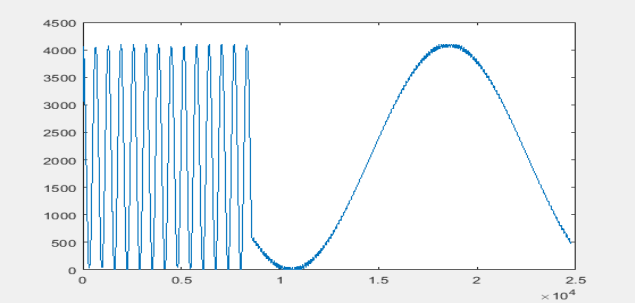


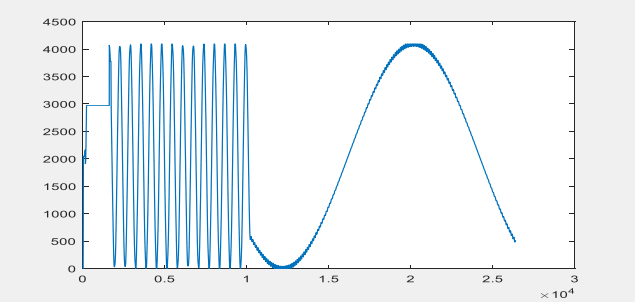
Fig. 10. Layout of proposed signal conditioner

C. Chip Test

Verification of the implemented RVDT signal conditioner proceeds as in Fig. 12(a). As shown in Fig. 12(b), a chip test environment is constructed by using a FPGA board and an oscilloscope. First, we use MATLAB to generate two signals, message and carrier signals, as 12-bit digital signals and store them in memory using FPGA. Next, these two signals are multiplied to produce an input signal $s(t)$ that is a modulated signal. The input signal and the carrier signal are applied to in_A and in_B inputs of RVDT_SC, respectively. The input signal is demodulated in the proposed RVDT_SC signal conditioner. The demodulated signal is fed into a DAC of the FPGA board and checked using an oscilloscope, as shown in Fig.13. The demodulated output signal is checked by using the signal verification module implemented in FPGA.

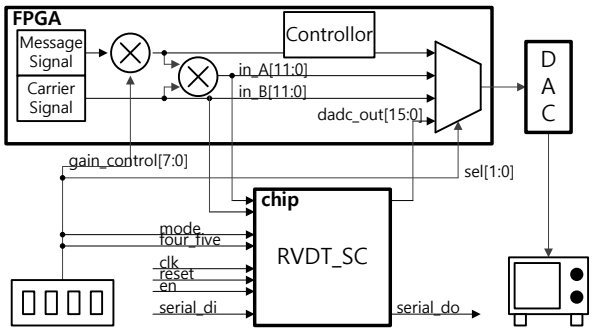


(a)

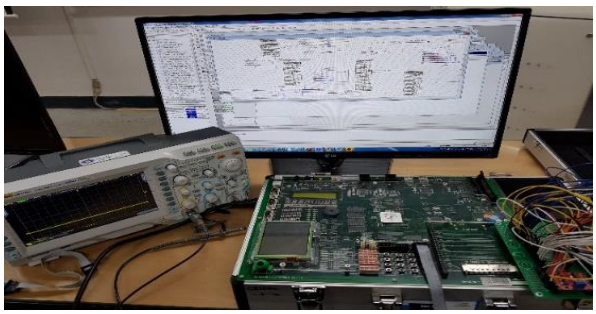


(b)

Fig. 11. Post-simulation result; (a) Message signal (b) post-simulation output signal

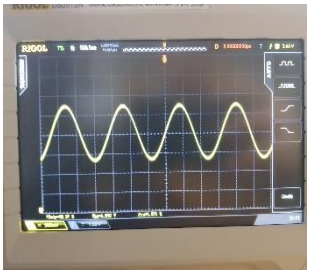


(a)

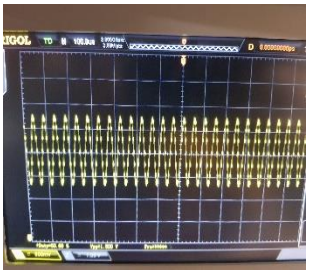


(b)

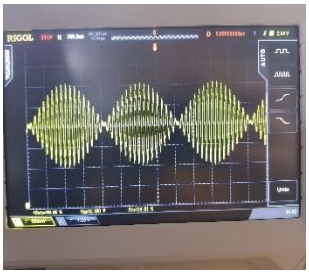
Fig. 12. Chip test; (a)Test block diagram (b)Test environment



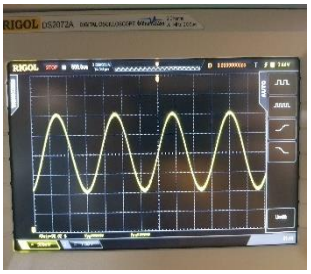
(a)



(b)



(c)



(d)

Fig. 13. Chip test result; (a)Message signal (b)Carrier signal (c)Modulated signal (d)Demodulated signal

The maximum linearity errors of some signal conditioners are shown in Table II, where the proposed structure shows a better linearity performance when compared with other structures. We can see that the proposed structure provides as good linearity performance as the commercial signal conditioner in [11].

Table II. Maximum Linearity Errors

Signal conditioners	[7]	[8]	[9]	[10]	[11]	proposed
Max. linearity error (%FSO)	0.14	0.18	0.16	0.2	0.01	0.01

IV. CONCLUSIONS

In this paper, we present the RVDT signal conditioner based on the Costas loop. After verifying a Matlab model, we implemented the signal conditioner by using VerilogHDL, which is synthesized by using a standard 180nm CMOS process. The implemented RVDT digital signal processor can be applied to 4-wire and 5-wire systems, and there is no need for external devices required for phase correction. In addition, the linearity compensation coefficients, the gain, and the offset can be adjusted through the UART communication, thereby increasing the linearity.

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