DC-DC buck converter using hopping technique and capacitor-less LDO regulator design for EMC

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Abstract **- In this paper, we increased the electromagnetic interference (EMI) reduction amount by improving frequency hopping control method and applying dead-time control technique. The original control method of frequency hopping creates unwanted frequency components during the transition of control clock. By improving the hopping control, unwanted frequency component is totally removed. Combining the optimized frequency hopping and dead-time method, the EMI reduced is up to 13.5dB at the fundamental switching frequency. Moreover, a low drop-out (LDO) regulator was designed with high noise immunity against the conducted EMI generated from the DC-DC converter. In this work, DC PSR (power-supply rejection) performance of the LDO regulator was enhanced by optimizing the DC PSR of the bandgap reference (BGR) circuit and the bandwidth was widen by eliminating the parasitic capacitances occurring at the gate of the pass transistor by adding the voltage dependent current source.**

Keywords**—Bandgap reference circuit, DC-DC converter, Frequency hopping control technique, Capacitor-less low drop-out (LDO) regulator**

I. INTRODUCTION

The switching node of DC-DC converter is the dominant source of EMI emission among the nodes of DC-DC converter. The frequency hopping technique is proposed to be applied to reduce the spur in the output node of the DC-DC converter [1]. The ideal of frequency hopping techniques is to spreading out the switching frequency of the DC-DC converter. By doing that, the frequency of the switching node is also spread out. Therefore, the power spectrum of the switching node is also reduced and EMI emitted from this node is reduced [2]

In the frequency hopping technique, an asynchronies clock is used to control the pseudo-random generator. The random bits are used to control the variation of internal saw-tooth signal as shown in Fig. 1 (a). By varying saw-tooth, the switching frequency is varied accordingly. In the operation case of this structure, there is high probability that rising edge of external clock is at middle of the saw-tooth signal. In that case, the saw-tooth cycle crossed by external clock is abnormally changed. The frequency of the abnormal saw-tooth makes the unwanted spur which is not include in the desire frequency sweep set as show in Fig. 1 (b).

With the DC-DC converter, the LDO regulator with high noise immunity against the conducted EMI noise generated from the DC-DC converter is designed. A PMIC usually consists of a DC-DC converter and a LDO regulator. The LDO regulator is usually placed at the stage that follows the DC-DC converter in the PMIC. Therefore, it is required to reject the noise from the DC-DC converter up to its operating frequency and its harmonics.

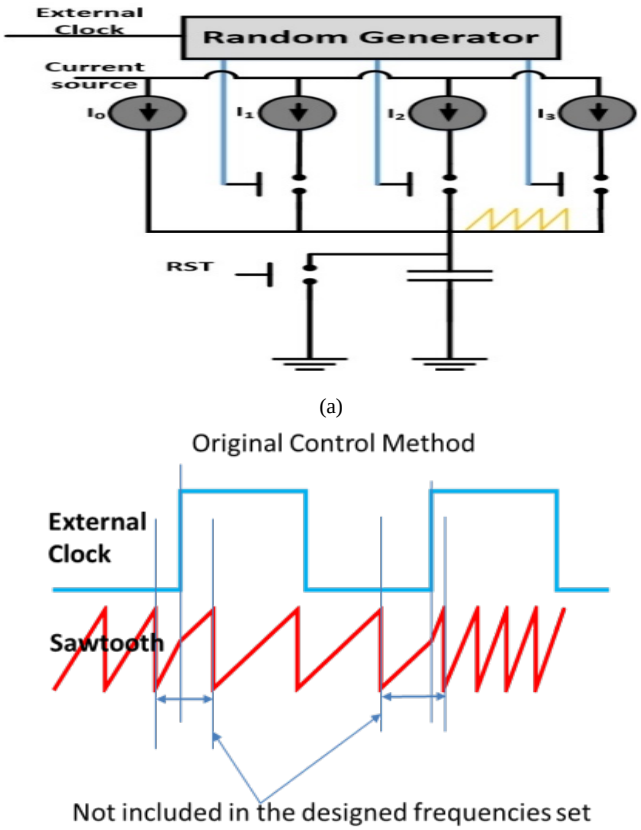

Fig. 1. Original saw-tooth frequency sweep. (a) Control circuit, (b) Saw-tooth waveform.

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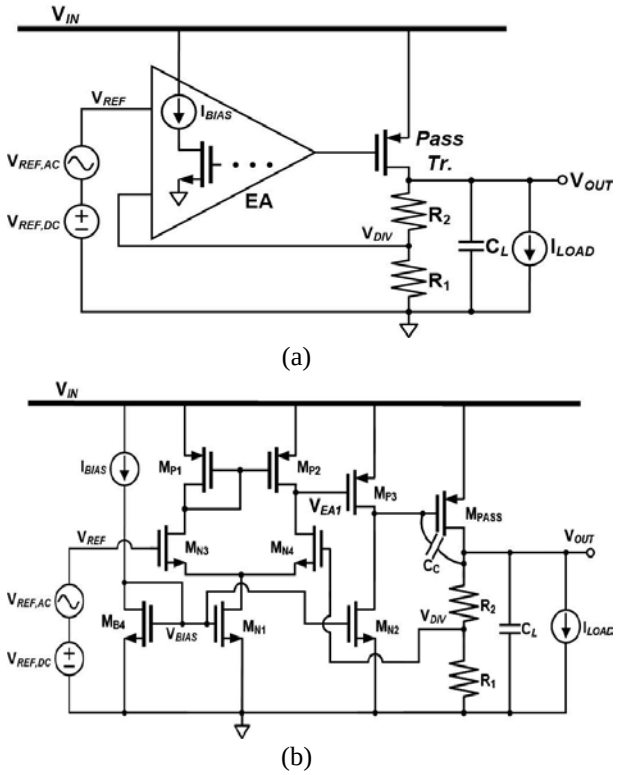


Fig. 2. (a) Block diagram and (b) the schematic of LDO_{conven}.

The structure of a conventional LDO regulator (LDO_{conven}) with a PMOS pass transistor and its schematic are presented in Fig. 2. A conventional LDO regulator usually consists of an error amplifier (EA), a bandgap reference (BGR) circuit, feedback resistors (R_1 and R_2), and a pass transistor. The EA compares the two inputs of a differential pair, coming from the divided voltage (V_{DIV}) produced by the feedback resistors and the reference voltage (V_{REF}) from the bandgap reference (BGR) circuit, and then controls the gate voltage of the pass transistor to maintain a constant DC output voltage [3]-[5]. Moreover, a supply-independent biasing circuit is used [7]. Fig. 3 shows the structure of the proposed output-capacitor free LDO regulator. Usually, the conventional LDO regulator consists of a large load capacitance of several microns or more. However, the fully-integrated LDO regulator becames a new design trend in the modern mobile IC design. PSR performance depends on the DC PSR and on bandwidth characteristics. To minimize DC

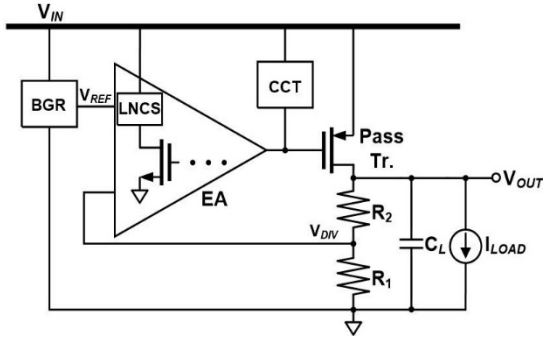
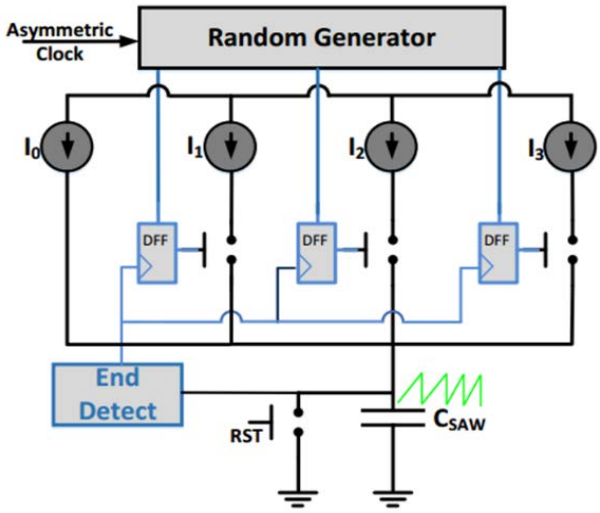


Fig. 3. Block diagram of the proposed LDO.

PSR, an optimization method for the DC PSR of the BGR is proposed. Moreover, the capacitor cancellation technique (CCT) is proposed to increase the PSR bandwidth. The design methodologies as mentioned above are verified using both analytic PSR models and SPICE simulation.

II. PROPOSAL OF IMPROVEMENT FREQUENCY HOPPING TECHNIQUE

To solve the problem of generating unwanted frequency component, additional control logic is added to postpone the change of input charging current until the recent saw-tooth cycle is finished as shown in Fig. 4 (a). The result of the additional control logic shows that the unwanted frequency component is removed from saw-tooth signal as shown in Fig. 4 (b). For further improving the EMI emission reduction amount, the dead-time control [6]-[8] is used to create the delay between switch control signals to reduce the jitter in the switching net. The overall schematic is shown in Fig. 5.



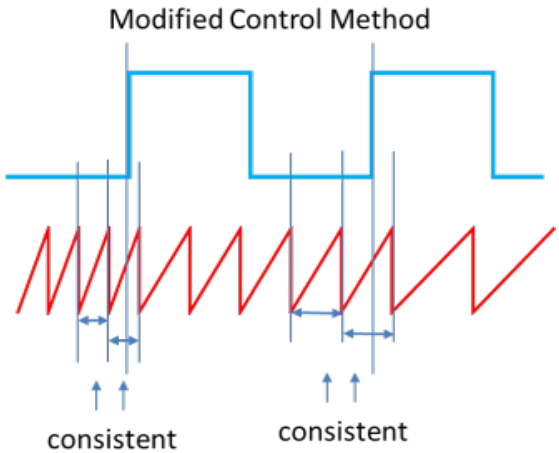


Fig. 4. Proposal of new saw-tooth controller. (a) Control circuit, (b) saw-tooth waveform.

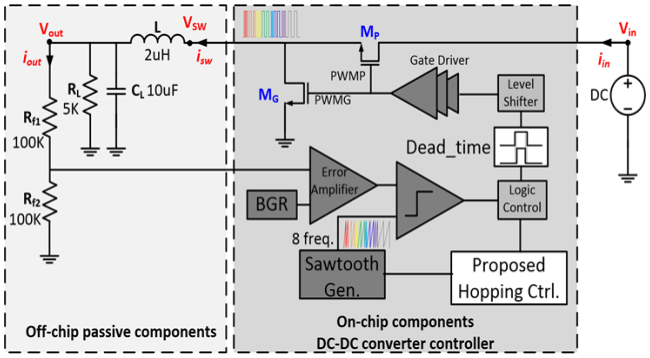


Fig. 5. Proposed DC-DC converter schematic.

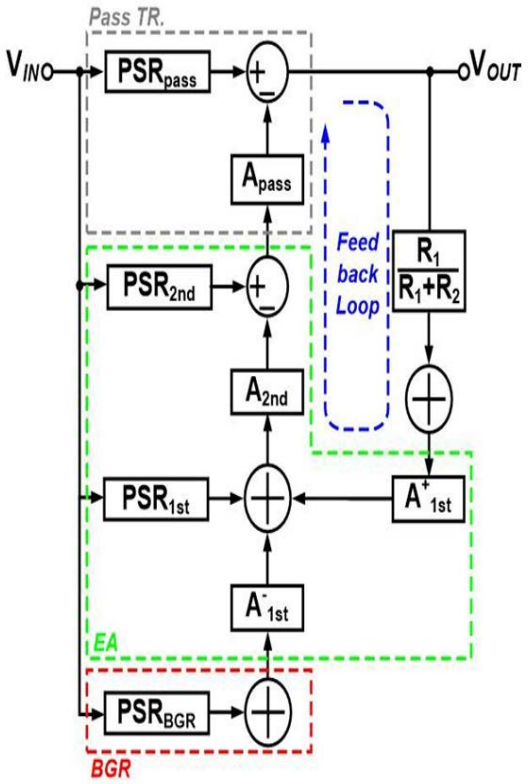


Fig. 6. Signal flow graph of LDO regulator [9].

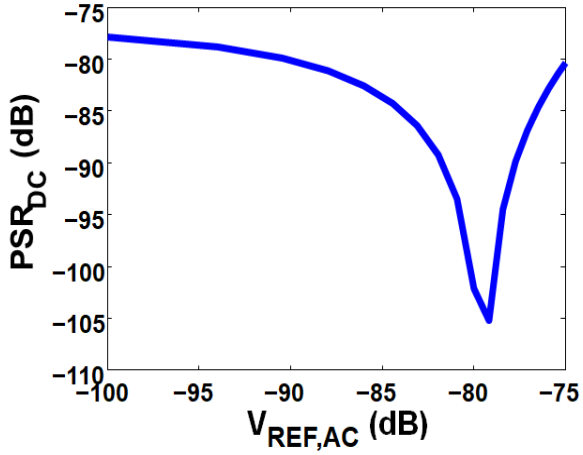


Fig. 7. The optimization results of PSRDC according to VREF,AC variation.

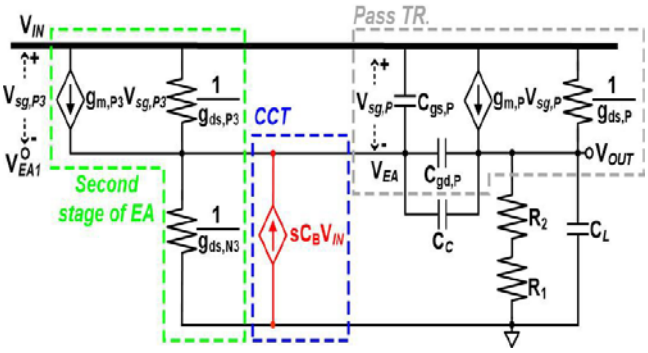


Fig. 8. Small-signal-equivalent circuits with CCT.

III. PSR ENHANCEMENT TECHNIQUES

In Fig. 2, the initially designed LDO regulator (LDO_{conven}) with two-stages EA with the PMOS active load and PMOS pass transistor is shown. LDO_{conven} has the ideal current source (I_{BIAS}) of 1 μA and the ideal voltage source to supply DC reference voltage ($V_{REF,DC}$), which is set to 0.9 V. Moreover, low-noise biasing circuit was designed with wide bandwidth as compared to the conventional voltage-dependent biasing circuit.

A. BGR optimization

In Fig. 6, the signal flow graph of the LDO regulator including the PSR (power-supply rejection) performance of BGR (PSR_{BGR}) is shown. As shown in Fig. 3, PSR_{BGR} affects the DC PSR performance of the LDO regulator without degrading the loop stability. Based on the Mason's gain formula, the equation for the DC PSR performance of the LDO regulator (PSR_{DC}) including PSR_{BGR} can be expressed as

$$PSR_{DC} = \frac{PSR_{pass} - A_{pass}(PSR_{2nd} - A_{2nd}(PSR_{1st} + PSR_{BGR}A_{1st}^{-}))}{1 + \beta A_{1st}^{+} A_{2nd} A_{pass}} \quad (1)$$

where PSR_{pass}, PSR_{1st}, PSR_{2nd}, and PSR_{BGR} are the DC PSR performances of the pass transistor, first/second stages of EA, and BGR, and A_{2nd} and A_{pass} are the voltage gain of the second stages of the EA and the pass transistor, respectively. And, A_{1st}^{+} and $A^{-}{}_{1st}$ are the voltage gains of the EA from the differential inputs. As seen in (1), PSR_{DC} is defined by considering the magnitude and phase of the DC PSR and voltage gain of each block. Therefore, it is possible for PSR_{DC} to be enhanced by optimizing PSR_{BGR} to have proper magnitude and phase.

In this work, we find the optimum value of PSR_{BGR} by sweeping $V_{REF,AC}$ shown in Fig. 7 to minimize PSR_{DC}. In Fig. 7, the AC simulation results of PSR_{DC} according to Fig. 7. The small-signal-equivalent circuit of the proposed LDO.

The variation of $V_{REF,AC}$ having opposite phase with V_{IN} is shown. Generally, it is easy to consider that lower PSR performance of BGR less affects the entire PSR performance

of the LDO. However, PSR_{DC} shows minimum PSR performance at approximately -79 dB of PSR_{BGR}. Based on this result, BGR is designed to have optimum PSR value obtained from the simulation result of Fig. 7.

B. Capacitor Cancellation Technique (CCT)

As mentioned in previous research [10], [11], the BW of the LDO can be analyzed considering Miller effect between the gate of the pass transistor and V_{IN}. In this work, capacitor cancellation technique (CCT) is used to compensate the BW of the LDO by adding voltage-dependent-current source (sC_BV_{IN}) at the gate of the pass transistor. In Fig. 8, the small-signal-equivalent circuits of the proposed LDO with CCT are described. After solving equations obtained by using KCL at the V_{EA} and V_{OUT} of Fig. 5, the 3dB BW of the PSR (ω_z (rad/s)) can be expressed as

$$\omega_z = \frac{g_{ds,P3}(1-A_0)+g_{ds,N3}-A_0 g_{m,P3}(1-PSR_{1st})}{C_{gs,P}(1-A_0)+(C_{gd,P}+C_C)\left(1+\frac{g_{m,P3}(1-PSR_{1st})+g_{ds,P3}}{g_{m,P}+g_{ds,P}}\right)} \quad (2)$$

where A_0 is the intrinsic gain ($A_0 = \frac{g_{m,P}}{g_{m,P}+g_{ds,P}}$) between the gate of the pass transistor and V_{IN}. Since the intrinsic gain is close to 1, the effects of $C_{gs,P}$ and $g_{ds,P3}$ almost disappear. In addition, PSR_{1st} is also close to 1, ω_z can be approximately expressed as follows:

$$\omega_{z,appox} = \frac{g_{ds,N3}}{C_{gd,P}+C_C-C_B} \quad (3)$$

As shown in (3), the BW can be enhanced because the effect of C_C and $C_{gd,P}$ can be eliminated if C_B has similar value with the sum of $C_{gd,P}$ and C_C. To verify this analysis, the simulation is implemented by adding CCT circuit shown in Fig. 9 at the gate of the pass transistor. The optimization results of f_z (Hz) according to C_B is shown in Fig. 9. In Fig. 10, the PSR performances of designed LDOs with BGR and CCT are presented. Moreover, the comparison results of the performances of the LDOs including the stability and the current consumption are summarized in Table. I. As mentioned in previous subsection, the phase margin is maintained regardless of the existence of BGR and CCT circuits. In Fig. 12, the DC offset variations of the LDOs are presented when a sine wave of an amplitude of 1 V was induced at V_{IN} are shown. Moreover, in Fig. 10, the noise immunity performance of the proposed LDO against the conducted EMI from the DC-DC converter. In the mid-frequency region, the DC offset variation is improved approximately 15 %. The conducted EMI reduction of the proposed LDO is also improved approximately 18 dB.

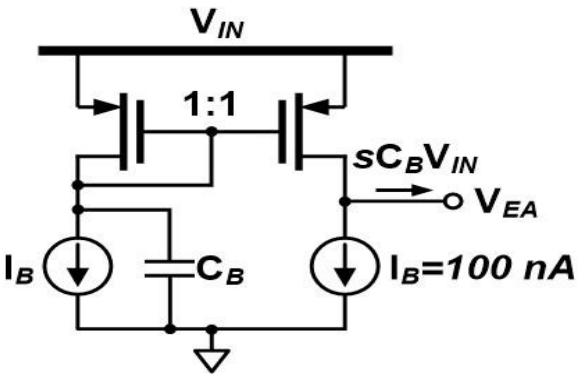


Fig. 9. The simple schematic of CCT.

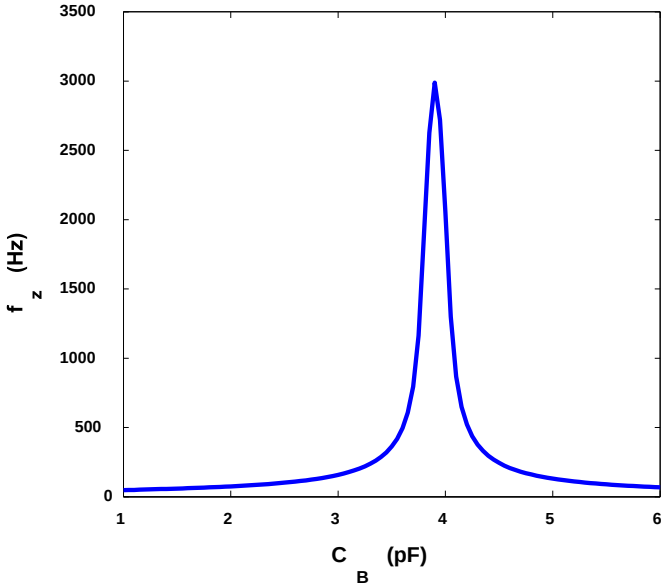


Fig. 10. The optimization results of fz according to CB.

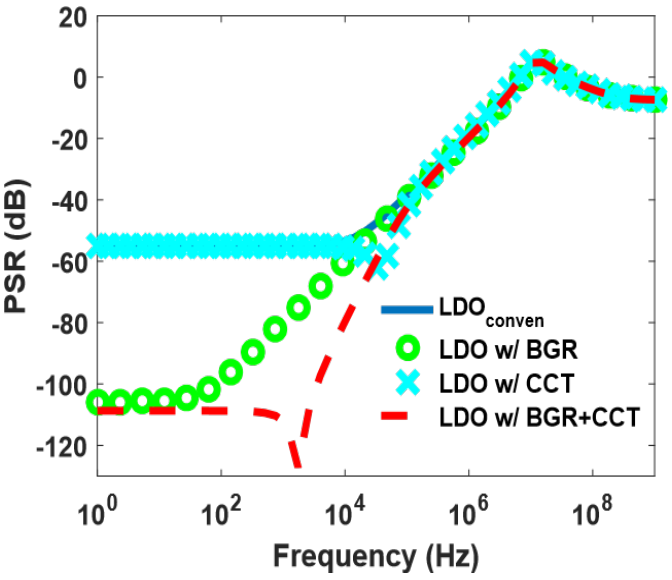


Fig. 11. PSR simulation results.

TABLE I. Performance comparison of the LDO regulators

	Unit	LDO*conven*	LDO*proposed*
VOUT	V	1.21	1.24
IQ	μA	35.24	48.8
Loop gain	dB	83.36	81.05
Phase margin	degree	45.73	46.3
PSR (@DC)	dB	-55.06	-108.71
PSR3*dB*	Hz	14.82k	2.93k
Conducted EMI reduction	dB	-5.76 (@2.5 MHz)	-23.92 (@2.5 MHz)

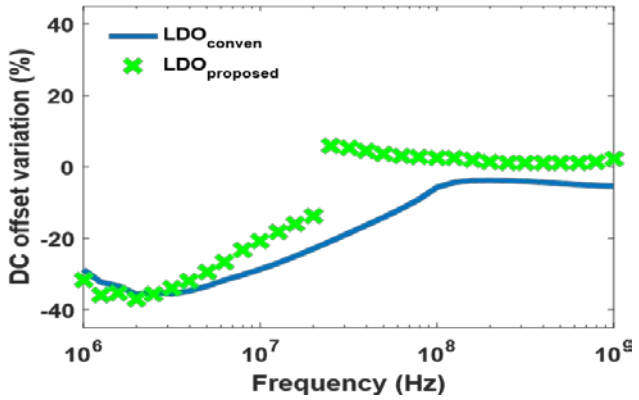


Fig. 12. DC offset variations of the LDOs.

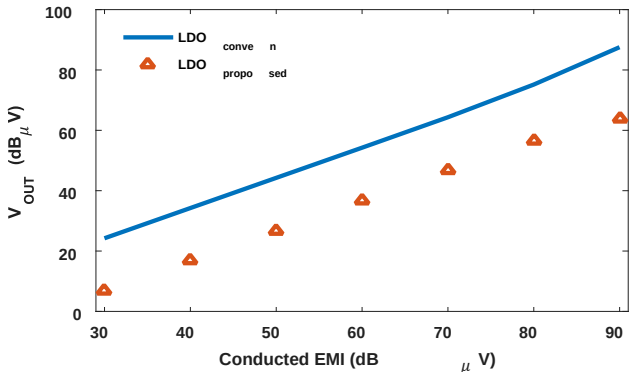


Fig. 13. Conducted EMI reduction.

IV. EXPERIMENTS

A. Measurement of optimal hopping control structure

The new version DC-DC converter are taped-out and measured for confirming the operation and performance. The switching node signal is measured along with the external clock control to confirm the performance of proposed feedback control logic. The measurement waveform is shown in Fig. 14.

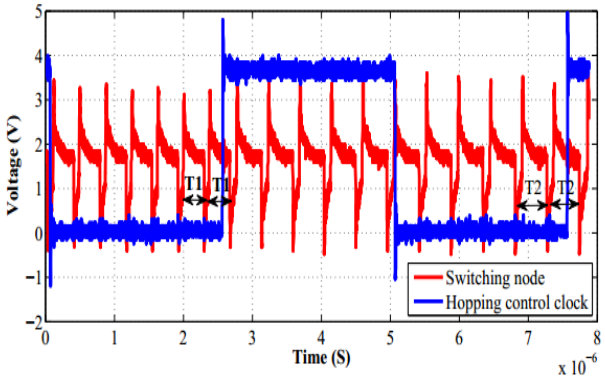


Fig. 14. Switching node voltage vs external control clock waveform.

By using the feedback control logic, during the transition time of external control clock, the cycle of saw-tooth signal is not changed. The changing of charging current is postponed until next saw-tooth cycle to take effect. The switching node signal has exact phenomenal as the saw-tooth signal. As shown in the two rising edge in the Fig. 14, one switching cycle is crossed by rising edge and it has same period as previous cycles.

B. Measurement of EMI reduction improvement

The power spectrum of the switching node is measured to perform the EMI reduction. The spectrum of switching node is compared with the same when frequency hopping technique is disable and with the previous version of frequency hopping DC-DC converter. The test results are shown in Fig. 15.

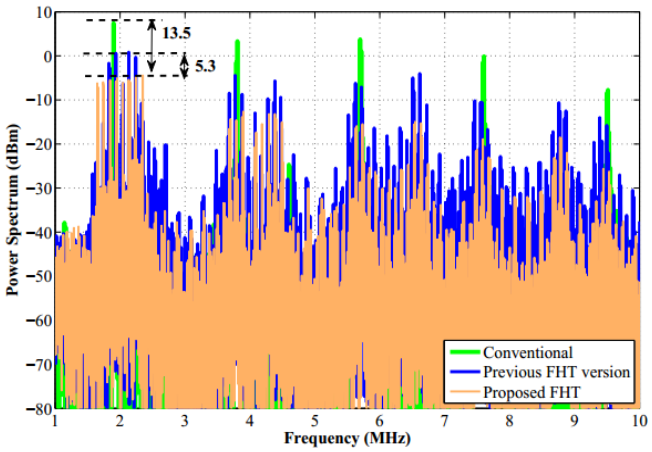


Fig. 15. Switching node power spectrum comparison.

The new version of DC-DC converter with frequency hopping adopt the feedback control logic for saw-tooth generator and dead-time control give a better EMI reduction amount comparing to previous version (up to 5dB higher). Comparing with the conventional DC-DC converter, the EMI reduction amount is up to 13.5 dB.

There is trade-off between EMI reduction and power conversion efficiency. This DC-DC converter gives a good performance in EMI reduction but maintains power conversion at a reasonable rate. The power conversion efficiency is up to 88% at heavy load condition (65 mA). The power conversion efficiency summary is shown in Fig. 16.

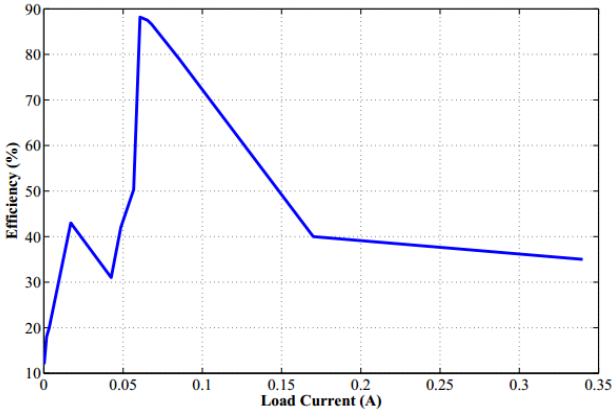


Fig. 16. Power conversion efficiency

C. PSR Measurement results of LDO regulator

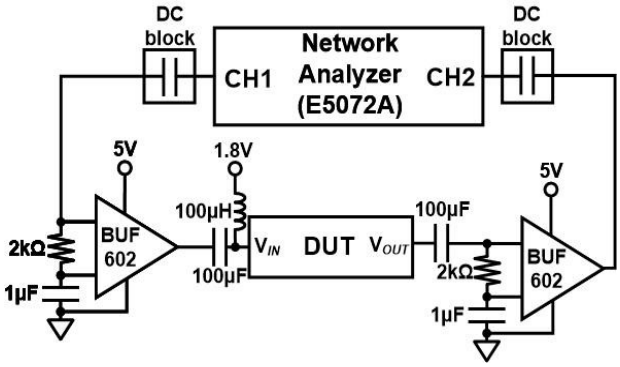


Fig. 17. Block diagram for PSR measurement

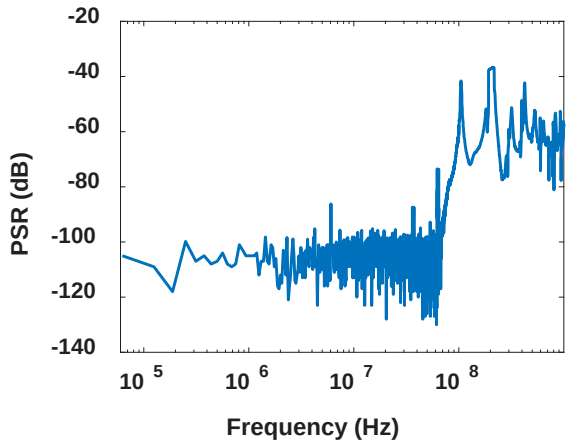


Fig. 18. PSR measurement result

The PSR performance of the LDO regulator designed by using Magna/Hynix 0.18 μm process was measured. The block diagram of measurement setup is illustrated in Fig. 17. For the PSR measurement, the network analyzer (Agilent E5072A [12]) and the AC coupled external buffer (T.I. BUF602 [13]) was used for the frequency dependent transfer function measurement over wide range of frequencies. A large capacitor (100μF) and an inductor (100μH) are used at the VIN and VOUT to separate DC and AC condition. Also, a resistor of 2kΩ and a capacitor of 1μF are used as recommended in [11]. The DC supply voltage for BUF602 and DUT are supplied by the power supply.

In Fig. 18, the PSR measurement results of the proposed LDO regulator is shown. The proposed LDO regulator maintains the PSR performance less than -80 dB up to few tens of MHz. The quiescent current when the load current is zero was 48 μA.

V. CONCLUSIONS

In this paper, we increased the reduction amount of EMI emitted from switching node of DC-DC converter by improving frequency hopping control method and applying dead-time control technique to the DC-DC converter. The original control method of frequency hopping creates unwanted frequency components during the transition of control clock. By improving the hopping control, unwanted frequency component is totally removed. Combining the optimized frequency hopping and dead-time method, the EMI reduced is up to 15dB at the fundamental switching frequency. The design is also be optimized to maintain high power conversion efficiency rate up to 88% at 65 mA load. Moreover, the LDO regulator shows excellent PSR measurement results. The proposed LDO regulator maintains the PSR performance less than - 80 dB up to few tens of MHz while consuming 48 μA of quiescent current.

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