# Design of RF CMOS Transceiver for Wireless Data Communication of Three-Dimensional Integrated Circuit Applications

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***Abstract* − In this study, a wireless type of chip-to-chip communication(WCC) technology is proposed as the next generation of three-dimensional(3D) semiconductor technology. To demonstrate the feasibility of the technology, we design a transceiver and receiver for wireless chip-to-chip communication method. The transceiver part for WCC circuit is designed using the conventional cross-coupled oscillator structure. To reduce the distortion of the signal, we input the data using the cascade structure. The receiver part for WCC circuit consists of coil. To confirm the characteristic of the proposed transceiver and receiver coil structures, we performed electromagnetic simulation. From the simulation results, the possibility of proposed wireless data transfer system was verified. The proposed wireless data transfer system has been designed using CMOS process. In simulation, the frequency of input data is 100 MHz and the peak-to-peak voltage of the input signal is 2 V. The peak-to-peak voltage of output signal is approximately 1.2 V and oscillation frequency is 1.75 GHz. The simulation result is shown that the transmitter part is transmitting signal which has only difference of 0.08 ns. Also it was found that wireless transceiver system has power consumption about 40%. In measurement result, data input setup 1MHz, and other setup is equal to that of the simulation. From the measured results, we successfully verify the feasibility of the proposed structure.**

## I. INTRODUCTION[1]

At the present, three-dimensional (3-D) integrated circuits (ICs) have been studied closely to enhance performance, small space, and reduced cost. Because of data transmission using two-dimensional (2-D) semiconductor in RF region, it is suffered from undesirable effects of parasitic inductance and capacitance caused by bonder-wire or PCB line. Because of effect of parasitic inductance and capacitance, 2-D semiconductor data transmission can be limited data transmission speed and suffered from signal distortion.

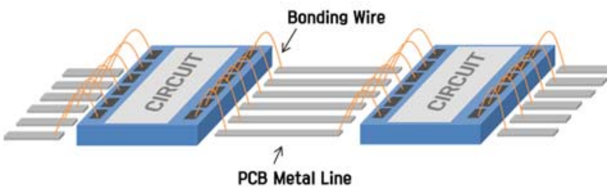
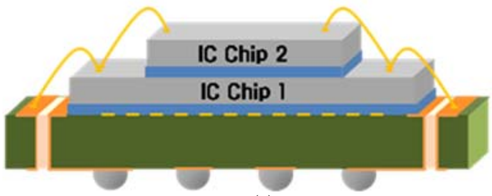
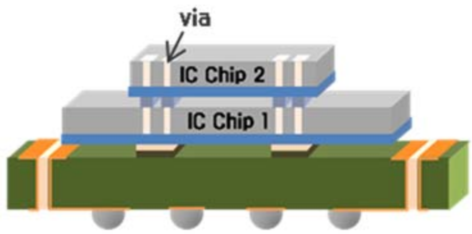



Fig. 1. Conceptual diagram of 2-D semiconductor technology




(a)




(b)

Fig. 2. 3-D IC (a)MCP technology (b)TSV technology

Wireless data transfer for 3-D ICs has some advantages as compared with 2-D semiconductors. First, 3-D ICs is able to reduce effects of parasitic inductance caused by bonder-wire. Because data transmission using 2-D semiconductor is performed through bonder-wire and PCB line as shown Figure 1, data transmission can be limited data transmission speed. Second, the physical path between the I/O PADs of each chip can be minimized compared with 2-D semiconductor cases. As shown Figure 2, there are no PCB metal lines between chips using 3-D ICs. So there are no parasitic inductances, and the signal or data transmission speed naturally increase. Third, Wireless data transfer for 3-D ICs can be miniaturized electronic devices and saved the unit cost of the systems. Therefore 3-D IC technologies provide an influential solution for the implementation of electronic systems.

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The wireless chip-to-chip communication (WCC) method is especially considered as next-generation of 3D semiconductor technology, while the multi-chip package (MCP) [1] and through-silicon via (TSV) [2,3] technologies are current technologies. MCP is packaging technology built up a number of chips in one. As stacking of several chips, it reduced the space between the chip and chip. However, there is a problem that the thickness of chip is extremely thin and each chip is connected as bonder-wire. TSV is a vertical electrical connection passing through a silicon wafer instead of connecting the chip using a wire. But, it is suffered from problems related to the development cost and the low yield.

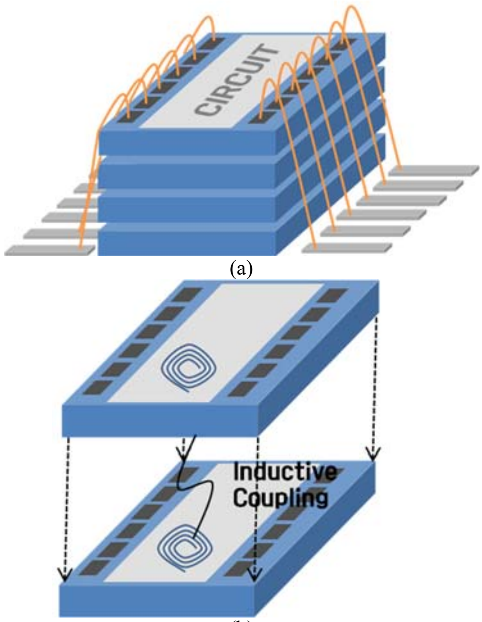

Fig. 3. (a) Conceptual diagram of wireless chip-to-chip communication (b) inductive coupling concept

Figure 3 shows a conceptual diagram of the WCC technology. As shown in Figure 3, stacked chips for communication need not wire. WCC communications select using inductive coupling method. Therefore WCC can eliminate the parasitic inductance and capacitance caused by PCB line and bonding-wire. Consequently, the cost of the overall system can be reduced compared to the MCP and TSV technologies. WCC technology can improve the problems of many long bonder-wires and various resonance frequencies resulting from MCP technology. Additionally, the problems about the development cost and the low yield of TSV technology can have solution using WCC technology. However, few studies have focused on WCC technology because this technology requires digital IC and electromagnetic field knowledge simultaneously. [4]

In this study, we proposed transceiver for wireless chip-to-chip communication method regarded as next-generation 3-D IC technology. We introduce WCC system architecture and design method. Finally, we demonstrate potentiality of WCC method through simulation and measurement.

## II. DESCPRITION

### *A. Description of transmitter part for WCC circuit*

Transmitter part of wireless data transfer for 3-D IC applications is designed applying conventional cross-coupled LC oscillator structure as shown Figure 4. The core part of conventional cross-coupled oscillator without varactor is used in the transmitter part. The inductor of the oscillator is used as coil of transmitter part. The oscillation frequency is determined by the values of the inductance and capacitance of the LC tank. To achieve the oscillation, two transistors are cross-coupled structure. Oscillator takes time to create a stable periodic oscillation waveform. This is called the starting time. If starting time takes a long time, it leads to a signal distortion. So it is very important to speed up the starting time in the data transmission system. Therefore, we obtain faster starting time adjusted LC value.

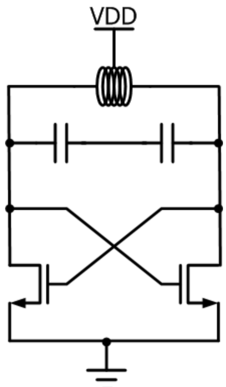

Fig. 2. Conventional cross-coupled oscillator structure

Furthermore, the oscillator added to data input part to transmission data. Figure 5 is shown as conventional current mirror data input structure. Conventional WCC transmitter has slow starting time because it consists of current mirror, which adjusts the current in the transmitter part. Accordingly, data signal and carrier signal have a little duty gap. Also structure of the circuit was complex because data input is through current mirror. Therefore, we proposed structure to switch oscillation directly. Also, it is designed that data input affects oscillation directly. As a result, it affects to reduce duty gap. We propose a cascade structure in which the gate nodes of the common-source transistor are connected to the source nodes of the common-gate transistor. This cascade transistor is functioned as switch which has a direct impact on the oscillation. Therefore, it makes oscillation waveform which has little duty gap between input clock and oscillation AC waveform.

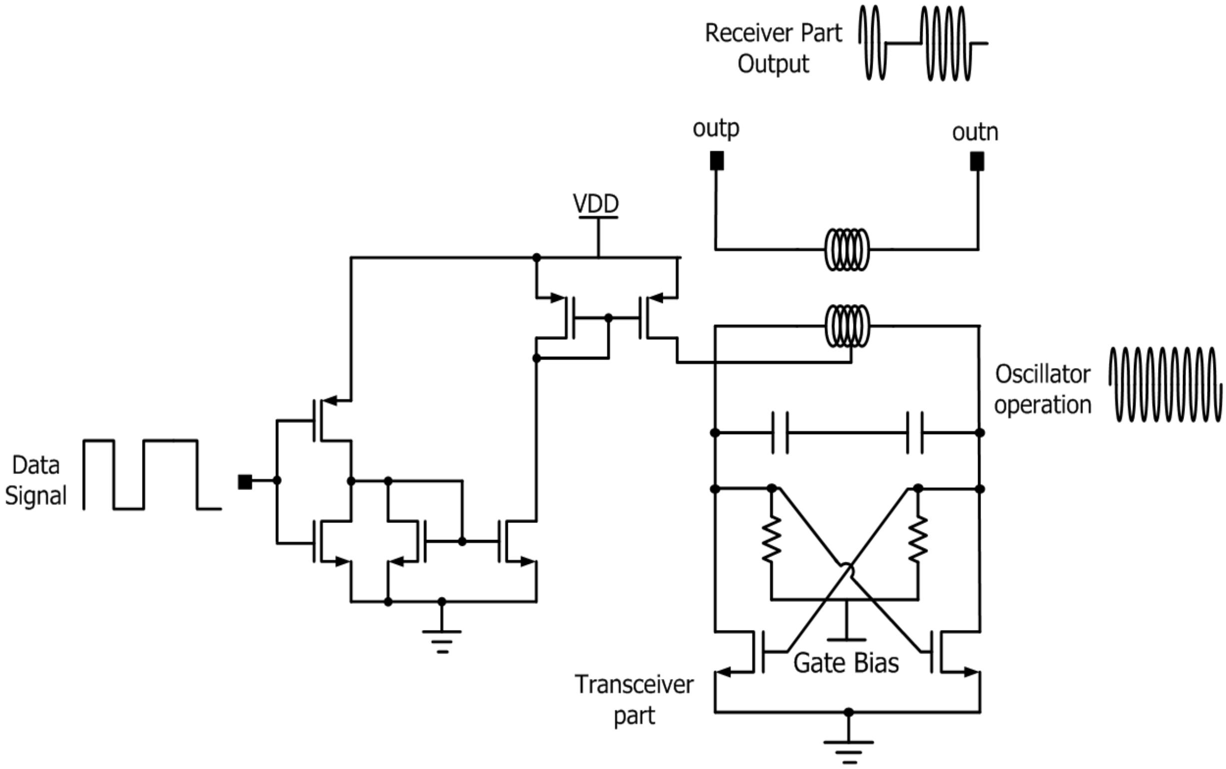


Fig. 5. Conventional wireless data transfer system for WCC circuit

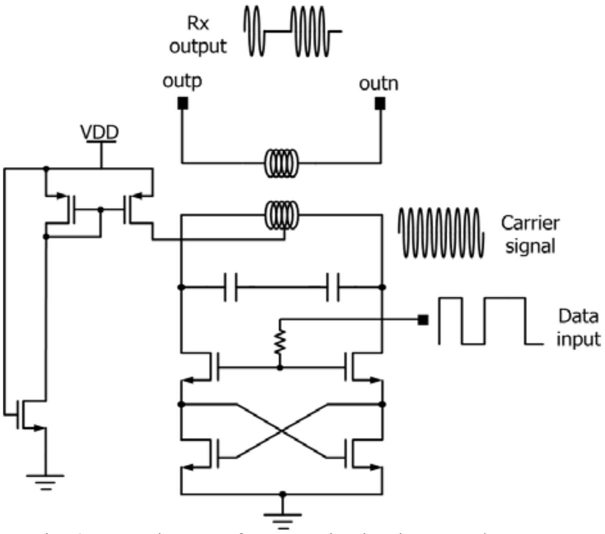


Fig. 6. Transmitter part for WCC circuit using cascade structure

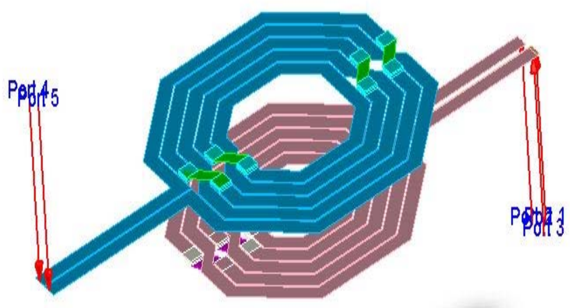

Fig. 7. EM simulation for Coil Characteristic

Additionally, transmitter part is added to cascode structure. The gate node of cascode structure is applied to the data input. Distortion-free signal transmission is very important in data transmission. Because cascade structure is functioned as switch of oscillation part directly, the data input can be made without distortion.

Figure 6 shows overall structure of proposed transceiver for WCC. As mentioned before, LC oscillator was generating a carrier signal. The circuit was constructed additionally to input data added cascade structure to set up turn on/off the oscillation directly. These two signals are combined in a transmitter part. The receiver part is conveyed a carrier signal that combined data input signal.

### *B. Design and Implementation*

The proposed transceiver is designed CMOS process. To verify the feasibility of the proposed transceiver and receiver coil structures, we performed electromagnetic (EM) simulation as shown Figure 6. Coil part is consisted as inductor of transmitter and antenna of receiver. Coil part is communicated using inductive coupling method. The distance between the chips is fixed at 100μm. The coil part was looking for a way having maximum transmission efficiency and was compared with the Q-factor, MAG, S-parameter through EM simulation. With the simulation parameter for the EM simulation, we simulated the overall circuits through Cadence. Then, we designed layout and modified according to design rule through Cadence.

We designed the metal width to be 30 μm and the coil radius to be 90 μm and the space between the adjacent metal lines to be 5 μm. In the overlaid coil, the receiver coil.

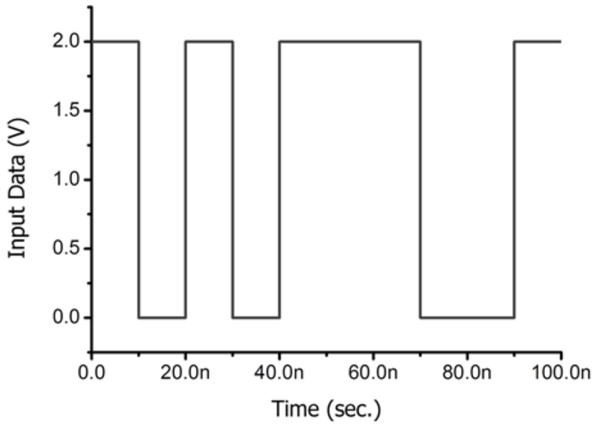


Fig. 8. Input data of transceiver for WCC

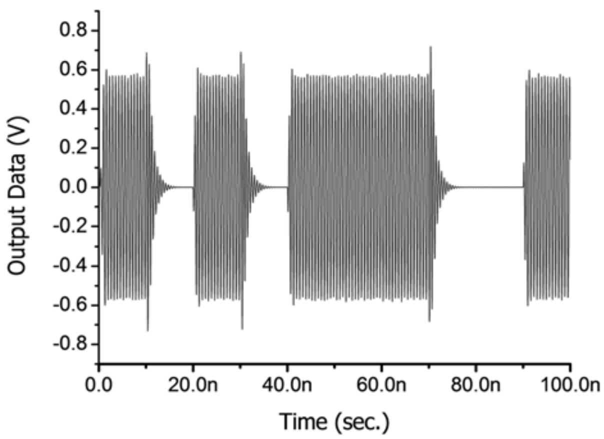


Fig. 9. Simulation results of receiver for WCC

## III. SIMULATION RESULTS

The proposed wireless data transfer system has been designed using CMOS process. Figure 8 shows the input data waveform entered cascade structure of transceiver part. The frequency of data input is 100 MHz and the peak-to-peak voltage of the input signal is 2 V. Figure 9 also shows the output voltage waveform of receiver coil. The peak-to-peak voltage of output signal is about 1.2 V and oscillation frequency is 1.75 GHz. When cheeked the duty difference between received signal and transmitter signal, unlike prior duty gap of conventional transmitter structure of WCC is 3ns, it has only difference of 0.08 ns. It decreased markedly. At this moment, transmission signal is delivered via the inductive coupling. Therefore, it was found that wireless transceiver system has power consumption about 40%. From the simulation results, the possibility of proposed wireless data transfer system was verified.

## IV. MEASUREMENT SETUP

To verify the feasibility of the proposed structure, we designed the CoB with the deigned IC of transceiver for the wireless chip-to-chip communication. Using the epoxy, we connect chip with PCB and avoid problems that may occur due to the exothermic by delivering the heat to PCB effectively. Additionally, we prevent the Cross-talk problems by connecting the GND of the PCB Substrate. After attaching the chip using epoxy, we attach the bypass capacitor on the outside in order to prevent the undesirable noise problem due to DC transmission.

After the completed chip for the measurement, we measure this chip having space between transceiver and receiver using the chip-to-chip devices. Input data is entered using the Function Generator. And Oscillation is confirmed by Spectrum Analyzer. Finally, we check the desired output waveform using the Oscillator.

## V. MEASUREMENT RESULTS

Figure 11 shows a photograph of the designed transmitter part of WCC. The WCC is fabricated using the 180-nm RF CMOS process, which provides six metal layers. The overall chip size including the testing pads is 1,040 × 540 $\mu m^2$. The supply voltage for the WCC is 2.5 V and the peak to peak voltage of input data is 2 V and offset voltage of data input is 1V. Also the frequency of data is 1MHz.

Figure 12 shows the measured waveform of receiver coil. As expected, it was able to identify transmission signal with little difference duty. Unlike the expected peak-to-peak voltage is 1.2V; the peak-to-peak voltage of transmission signal is 0.25V.

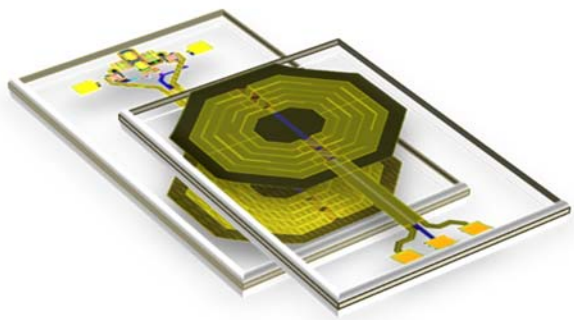

Fig. 10. Measurement method of WCC

Fig. 11. Chip Photograph of the fabricated transmitter part

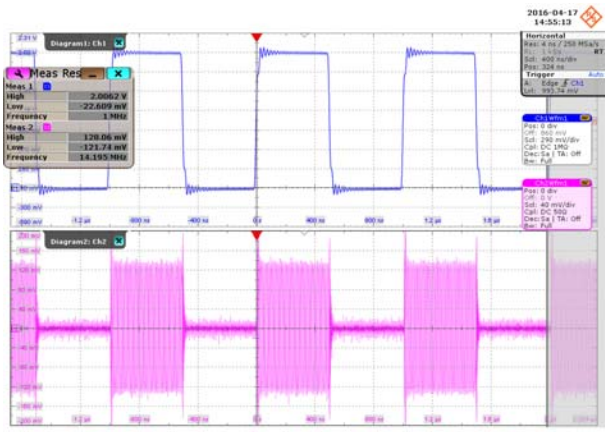

Fig. 12. Measured waveform of receiver coil

VI. CONCULSION

In this work, we propose a transceiver for wireless chip-to-chip communication method regarded as next-generation 3-D IC technology. The transmitter part is designed applying a conventional LC cross-coupled oscillator. To reduce the distortion of the signal, we input the data using the cascade structure. The signal transmission of the coil was confirmed by EM simulation, and chip was manufactured using this simulation data value. The frequency of input data is 100 MHz and the peak-to-peak voltage of the input signal is 2V. Figure 8 also shows the output voltage waveform of receiver coil. The peak-to-peak voltage of output signal is about 1.2V and oscillation frequency is 1.75GHz. The simulation result is shown the transmitter part is transmitting signal which has only difference of 0.08 ns. Also it was found that wireless transceiver system has power consumption about 40%. From the measured results, we successfully verify the feasibility of the proposed structure.

ACKNOWLEDGMENT

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