DC-DC buck converter using hopping technique and DTMOS Schmitt Trigger logic gates for EMC

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***Abstract* - A few circuits for Electromagnetic Compatibility (EMC) were designed through IDEC's last MPW (MS180-15030) process. One is DC-DC buck converter, and the other is Dynamic Threshold MOSFET (DTMOS) Schmitt Trigger (S. T.) logic gates.**

In this project, an EMI reduction technique is applied to the DC-DC converter. The frequency hopping technique is applied to reduce the power spectrum of the switching node of DC-DC converter which is the most dominant node generates EMI. The DC-DC converter with hopping frequency techniques is taped-out using 180nm CMOS process. The test results of the chip shows a significant improvement of the voltage spectrum at both output node and switching node of the DC-DC converter. Thus, the EMI generated by DC-DC converter is reduced by applying the frequency hopping technique.

Meanwhile, DTMOS S. T. logic gates are designed and fabricated using 180nm CMOS process. Especially, Deep N-well was used to get the separated NMOS body potential. These S. T. gates can be used for low power applications to increase noise immunity of the digital circuit. The proposed gates are verified with a simple example digital circuit.

I. INTRODUCTION

In any electronic system, the power supply part always takes the most importance role in maintaining the performance of the circuit. With the development of the electronic design skill, a system can contain a number of different chips in a chip. These kinds of chip contain many different dies which require a unique power supply voltage. Therefore, the DC-DC converter is widely used in the electronic systems.

With the increasing of the circuit density and of the operating frequency of the circuit, the electromagnetic interference (EMI) of devices becomes a serious problem [1]. The EMI in the power supply line is ways more serious. Therefore, in this project, the EMI generating problem of the DC-DC converter is considered.

The EMI is generated in proportion to the power spectrum of a node. In the reference paper [2], the frequency hopping techniques is applied to reduce the power spectrum at the output node of the DC-DC converter. In the operation of a DC-DC converter, the node that has the highest variation of current in and out is the switching node. Therefore, the dominant EMI generating source should be considered as the switching node.

In this project, the frequency hopping proposed in [2] is applied to the DC-DC buck converter. The switching node of the DC-DC converter chip is considered and analyzed in the measurement. The dominant EMI source is pointed out and the effectiveness of the frequency hopping technique on reducing EMI problem is concluded.

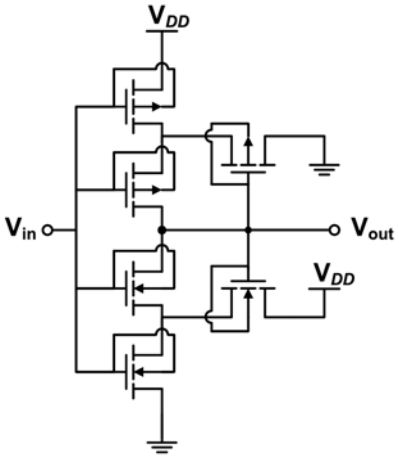

Fig. 1. Schematic of Conventional Schmitt trigger buffer.

With the DC-DC buck converter, DTMOS S. T. logic gates [3] were proposed. Recently, Internet of things (IoT) and wearable devices have attracted attention in the world. The main focus of this IoT era is low power and high reliability. This proposed S. T. logic gates can be an excellent solution to increase the noise immunity of digital circuit, because S. T. logic gates have a hysteresis characteristic. Especially, these proposed gates are suitable for low-power system. While Conventional S. T. buffer is using 8 transistors, this proposed S. T. buffer is only using 4 transistors. The traditional Schmitt trigger inverter design was shown in Figure 1. This design can implement hysteresis by using an extra current path that resists the signal transition out the output through the use of current

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feedback. Also, they are using total 8 transistors to implement Schmitt trigger buffer logic.

Through this project, real chip of DTMOS S. T. logic gates was fabricated and measured with an exact function. Some characteristics of S. T. logic gates will be shown as follows.

In this report, DC-DC buck converter using hopping technique and DTMOS Schmitt Trigger logic gates for EMC are designed and introduced. Experiments set-up and detail specification are described in Section II. Section III shows measurement result and discussion about result. Conclusion is presented in Section IV.

II. EXPERIMENTS

A. Analysis of EMI generating dominant.

A conventional DC-DC converter in Fig. 2. (a) is implemented and the power spectrum of switching node (V_{TMP} node) and output node (V_{out} node) is compared in Fig. 2. (b).

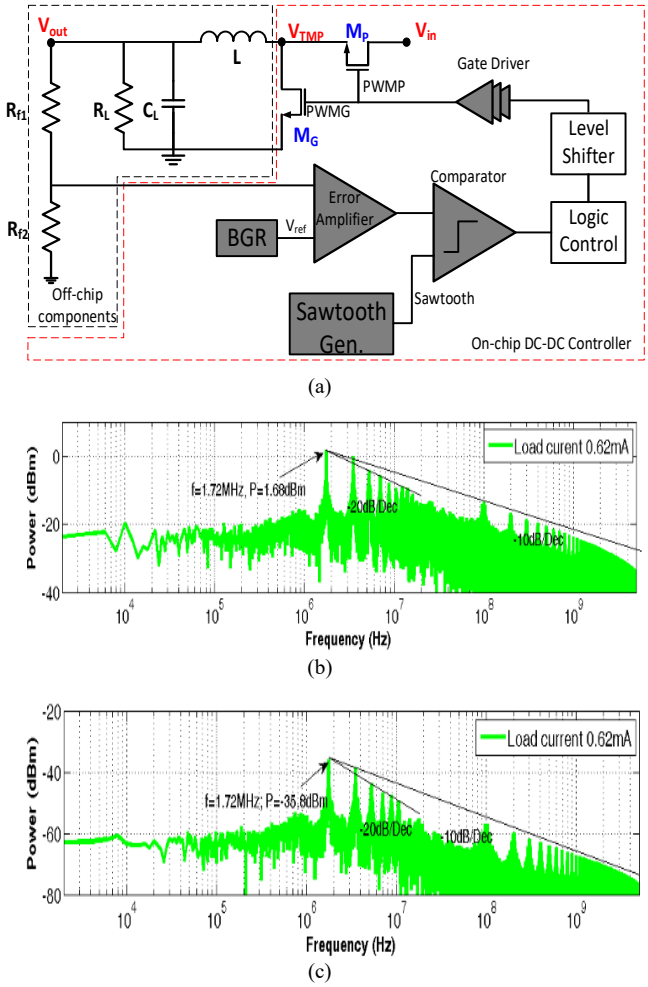


Fig. 2. Conventional DC-DC converter. (a) Conventional DC-DC converter schematic, (b) Switching node power spectrum, (c) Output power spectrum.

The power spectrums in Fig. 2 (b) and (c) show big gap between the switching node and output node power spectrum. The switching node has over 36 dB higher than the output node on power spectrum. Therefore, the dominant source for generating EMI is the switching node.

B. DC-DC converter with frequency hopping technique.

The hopping control block is added into the conventional DC-DC converter schematic to control the frequency of the saw-tooth generation. The saw-tooth frequency decides the center switching frequency of the DC-DC converter. By sweeping the switching frequency over 8 values, the power spectrum of the output node of DC-DC converter is expected to reduce by 18 dB theoretically.

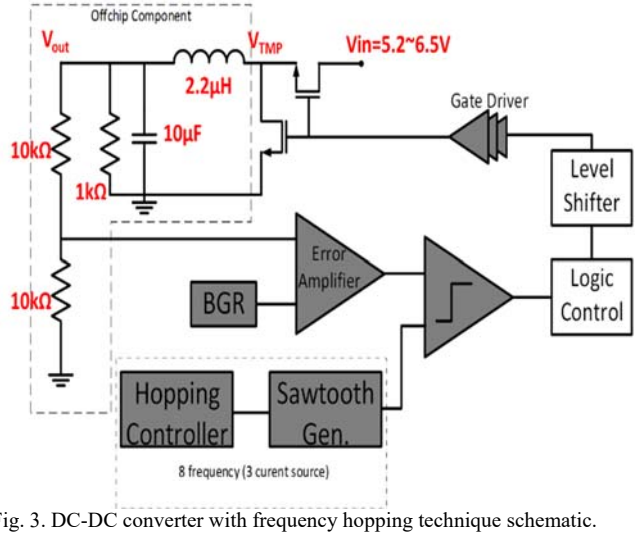


Fig. 3. DC-DC converter with frequency hopping technique schematic.

TABLE I.
DC-DC converter with frequency hopping technique specification

Parameter	Value
V_{ref}	0.85
f_{SWITCH}	1.2MHz~2.5MHz
V_{IN}	3.V~5V
V_{OUT}	0.85~2.8V
Output curent	Max 150mA
Output ripple	Max 200mA
Inductor	≥2.2 μH
Output capacitor	≥1 μF

The chip after taped-out is tested to confirm the operation before checking others performance. The operating waveform of the DC-DC converter with frequency hopping techniques is shown in Fig. 4. The hopping control clock shown in this test is 100 kHz. Within one clock cycle of hopping control, the switching frequency of the switching node is consistent. The switching frequency is changed randomly in the next hopping control clock cycle. In the test, the inductor and capacitor value is 2.2μH and 10 μF, respectively. The feedback resistor is shown in Fig. 3. The output voltage is expected to be 1.7 V. Our DC-DC converter design is well adapting the basic function operation.

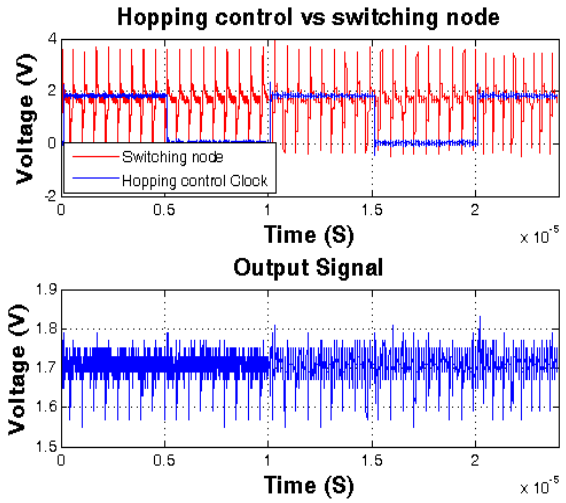


Fig. 4. DC-DC converter with frequency hopping techniques operation.

C. Schmitt Trigger Logic gates.

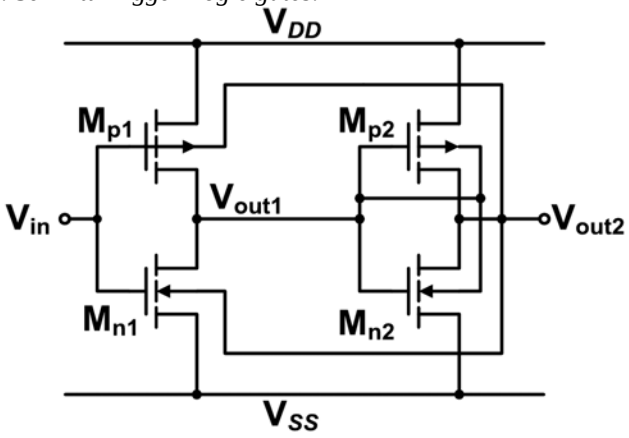


Fig. 5. Schematic of DTMOS Schmitt trigger buffer.

Figure 5 shows the DTMOS S. T. buffer [4]. This DTMOS S. T. buffer consists of two stages of CMOS inverters. They used only 4 transistors to implement Schmitt trigger buffer logic. The body bias of first stage inverter is controlled by the output of second stage inverter. DTMOS S. T. logic gates [3] were proposed and verified in simulation. Comparing data between conventional one and DTMOS Schmitt trigger is shown in table II. Layout Area, Hysteresis characteristic, Power consumption and delay were observed.

TABLE II.
Characteristics of a two Schmitt trigger buffer

Characteristic	Value	
	DTMOS	Conventional
Number of transistor	4	8 (6 + 2)
Layout Area	500 um^2	360 um^2
V_{LH}	0.333 V	0.3285 V
V_{HL}	0.273 V	0.2715 V
Hysteresis width	60 mV	57 mV
Switching Current	310.92 uA	1.277 mA
Delay	2.88 ns	1.73 ns

In common CMOS process, NMOS bodies are sharing their own body with p-substrate. So, it is difficult to control NMOS body potential. In this project, Deep N-well was applied in each NMOS device to control NMOS bodies separately. Layout of DTMOS Schmitt trigger buffer is shown in Figure 6.

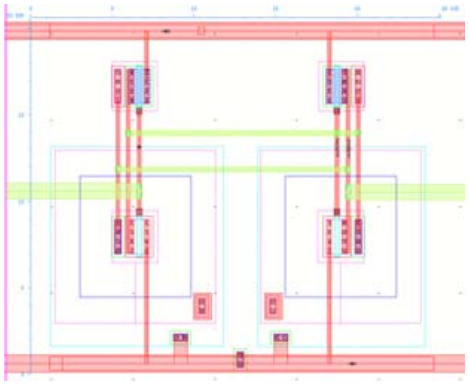


Fig. 6. Layout of DTMOS Schmitt trigger buffer.

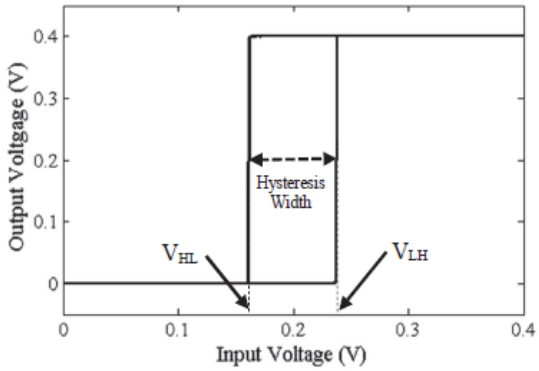
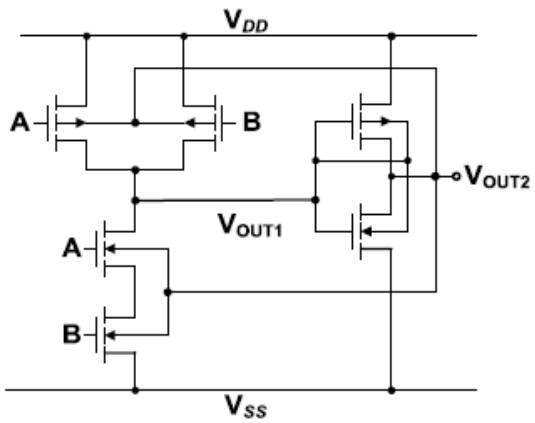
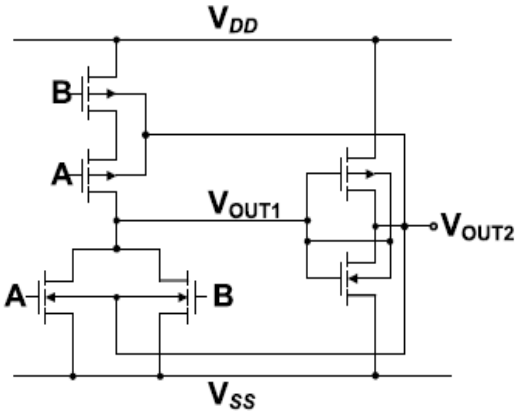


Fig. 7. Hysteresis characteristic of S. T. buffer.

Figure 7 shows hysteresis curve of S. T. buffer gate. This characteristic is produced by biasing body potential. The body potential of first stage is affected by output potential. For example, when the V_{in} is low, V_{out2} also will be low. This V_{out2} voltage is fed back to the body of the first stage. In this case, M_{n1} has zero substrate bias, M_{p1} has forward bias. As a result, threshold voltage for low to high transition V_{LH} is higher than $V_{DD}/2$. In contrast, threshold voltage for high to low transition (V_{HL}) is lower than half V_{DD}.



(a)



(b)

Fig. 8. Schematic of S. T. logic NAND (a) and NOR (b) gate.

Using the same DTMOS S. T. topology, we designed NAND gate and NOR gate. Figure 8 shows their schematics. They also have a hysteresis characteristic during low to high voltage transition.

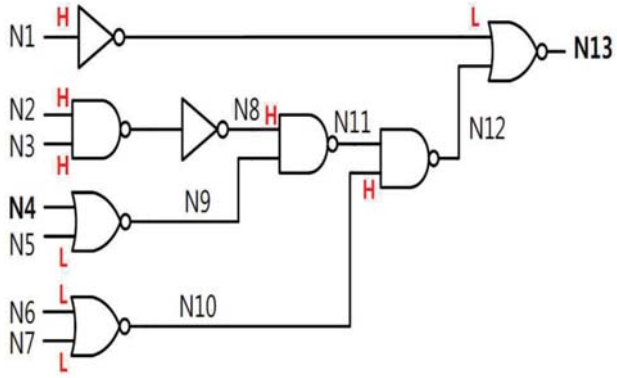


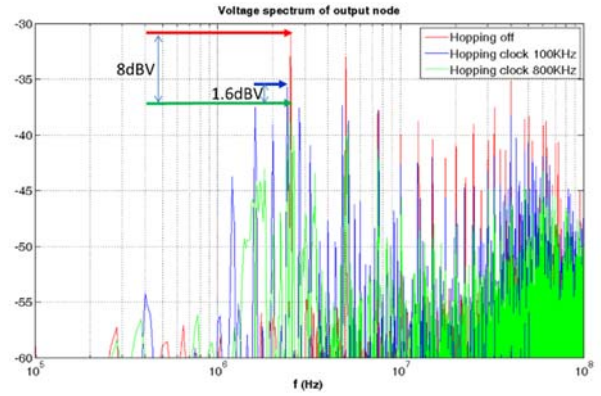
Fig. 9. Example circuit for noise immunity test.

To verify noise immunity in the circuit level, an example test circuit was designed like figure 9. Each of the gates consists of proposed S. T. logic gates. Originally, this circuit was designed for noise immunity test. However, in this time, only hysteresis characteristic was shown. We will focus on noise immunity enhancement using DTMOS S. T. logic gates in the next time. As shown in figure 9, N4 is a input port, noise will be injected with N4 input signal. N1-N3 ports were fixed to high, N5-N7 ports were fixed to low. N13 port will be changed following N4 input value. If some noise was injected into N4 input port, this noise can affect N13 output value. We can check noise immunity by monitoring just N13 output signal.

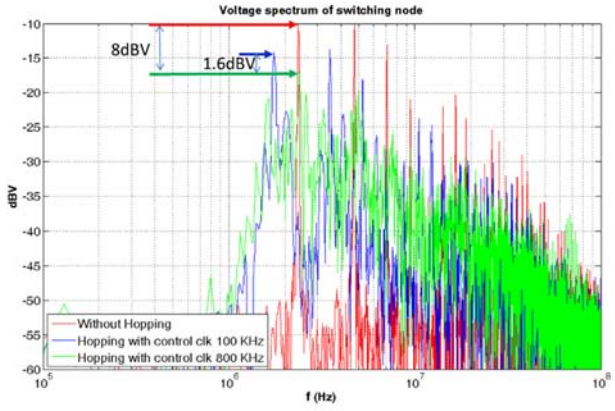
III. RESULTS AND DISCUSSION

A. Result of DC-DC converter.

The purpose of the proposed DC-DC converter is to reduce the EMI generating from the operation of the converter. The voltage spectrum of both switching node and output node is plotted and compared to those when frequency hopping is disabled. The comparison result is shown in Fig. 8.



(a)



(b)

Fig. 10. Voltage spectrum comparison. (a) Output node spectrum, (b) Switching node spectrum.

When the frequency hopping technique is enable, the volt age spectrum of both switching node and output node is sign ificantly reduced. The reduction amount of the spectrum dep ends on hopping control clock. During the experiment proce ss, the hopping clock frequency is optimized to find the valu e that maximizes the reduction amount. The hopping control clock at 800 KHz gives the high reduction amount around 8 dBV in both switching node and output node.

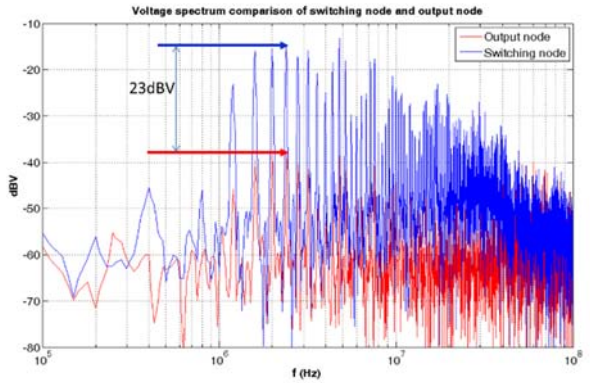


Fig. 11. Dominant EMI source spectrum comparison.

The voltage spectrum of switching node and output node is compared to conclude the dominant EMI generating source as shown in Fig. 11. The output voltage spectrum is smaller comparing to switching node. With the big gap of 23 dBV, the switching node can be concluded as the main

source that generates EMI in the DC-DC converter.

The performance comparing to the previous proposed design [2] is shown in Table. III.

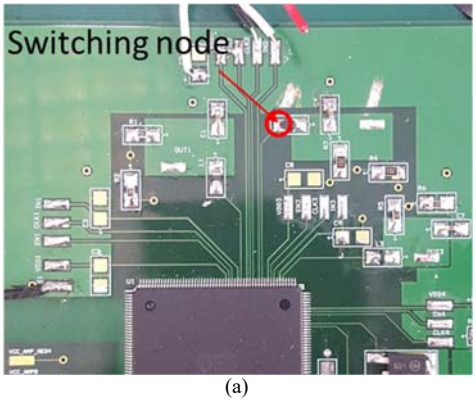
TABLE III.
Measurement and simulation result of Schmitt Trigger buffer gate

Parameter	Value	
	Previous[2]	Our
Input voltage	3.3-5.5V	3.0-5.5V
Output voltage	1.8V	1.8V
Output capacitor	10µF	2µF(min)
Output inductor	2µH	2µH
Load current	600mA	150mA
Switching frequency (single case)	2.2MHz	2MHz
Technology	0.35µm	0.18 µm
Active area	0.36mm^2	0.19mm^2
Frequency hopping control		
power spect. reduction (output)	13.2dB	8dB
power spect. reduction (sw)	--	8dB
EMI emission reduction	--	6.8dB

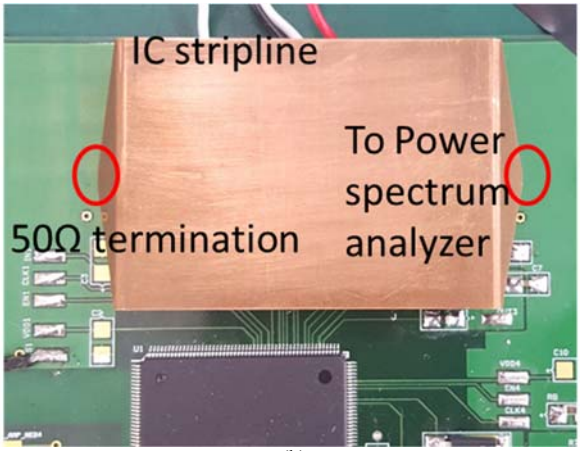
According to the comparison results, the reduction amount of power spectrum measured at output node in our design is less than previous. The reason is due to the unstable of the saw-tooth generator block. The random digital generator is also simple, therefore some designed frequencies is disable during the operation. Our design is a case study for analyzing the EMI reduction on DC-DC converter. Due to the conclusion that switching node is the main source of EMI generation, the reduction amount of power spectrum at switching node is compared when applying the frequency hopping techniques. The reduction amount of power spectrum at switching node when applying frequency hopping is around 8dB.

For analyzing the exact reduction amount of EMI emission from DC-DC converter. The IC-strip line method [5] is applied. The test setup for IC-strip line is shown in Figure 12.

The specification of IC-stripline follows the standard [6]. All the node of the DC-DC converter is corver bay IC-stripline, thus the EMI measured by IC-stripline is the total emission of all the node of DC-DC converter. The measurement result of EMI emission from DC-DC converter by using IC-stripline is shown in Figure 12.



(a)



(b)

Fig. 12. IC-stripline test setup. (a) DC-DC Converter PCB. (b) DC-DC converter PCB with IC-stripline.

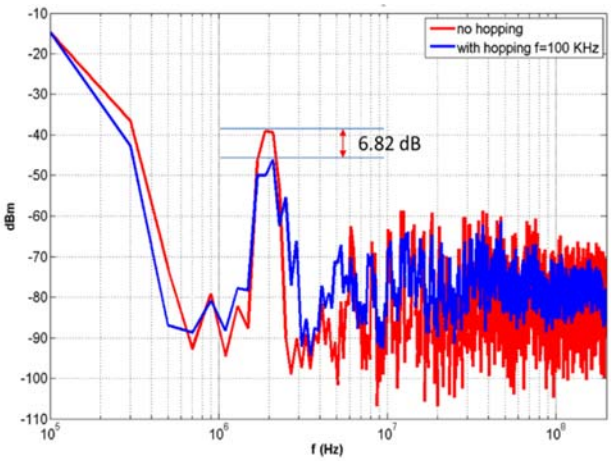


Fig. 13. EMI emission measurement result by IC-stripline.

The measurement result shown in Figure 13 proves the effectiveness of the frequency hopping on reduce the EMI emission from DC-DC converter. The reduction amount is 6.82dB and it can be further improved by optimizing the design in the future version.

B. Measurement Result of DTMOS S. T. logic gates.

Comparison of measurement result and simulation result are compared like below. Hysteresis curves are shown in the figure 14, and Detail parameters are shown in the table IV.

1) Schmitt Trigger Buffer gate

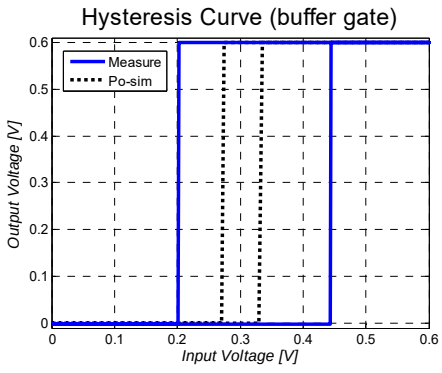


Fig. 14. Hysteresis curve of DTMOS S. T. buffer gate.

TABLE IV.
Measurement and simulation result of Schmitt Trigger buffer gate

Parameter	Value	
	Simulation	Measurement
Voltage Power	0.6V	
V_{LH}	0.333 V	0.443 V
V_{HL}	0.273 V	0.202 V
Hysteresis width	60 mV	241 mV
Offset voltage	0.303 V	0.322 V

Figure 14 shows hysteresis curve of DTMOS S. T. buffer gate. Blue line is for measurement result, and black dash line is for post lay out simulation result. We can see that measurement result offset is higher than half Vdd. We can also find out measurement result is wider than simulation result. It may be caused by process mismatch.

2) Schmitt Trigger Inverter gate

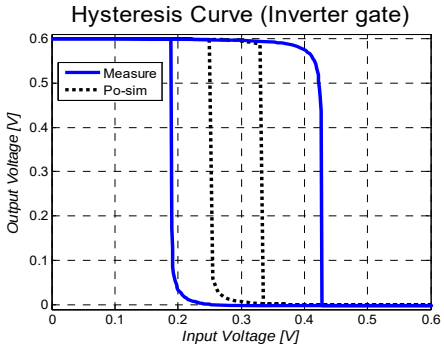


Fig. 15. Hysteresis curve of DTMOS S. T. inverter gate.

TABLE V.
Measurement and simulation result of Schmitt Trigger inverter gate

Parameter	Value	
	Simulation	Measurement
Voltage Power	0.6V	
V_{LH}	0.332 V	0.427 V
V_{HL}	0.253 V	0.189 V
Hysteresis width	79 mV	238 mV
Offset voltage	0.293 V	0.308 V

Figure 15 and Table V shows measurement and simulation result of S. T. inverter gate. Result is similar with buffer case. Inverter also has higher offset and wider hysteresis comparing simulation result.

3) Schmitt Trigger NAND gate

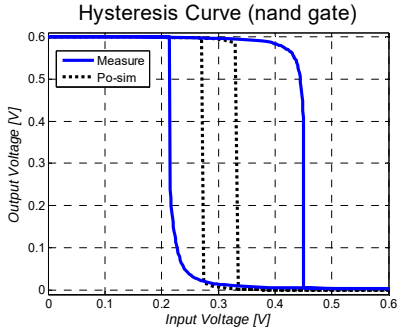


Fig. 16. Hysteresis curve of DTMOS S. T. nand gate.

TABLE IV.
Measurement and simulation result of Schmitt Trigger nand gate

Parameter	Value	
	Simulation	Measurement
Voltage Power	0.6V	
V_{LH}	0.332 V	0.450 V
V_{HL}	0.273 V	0.214 V
Hysteresis width	59 mV	236 mV
Offset voltage	0.302 V	0.332 V

To test NAND gate, One of input is fixed to one. And another input is sweep from low to high. Hysteresis curve of NAND is similar with inverter′s hysteresis curve.

4) Schmitt Trigger NOR gate

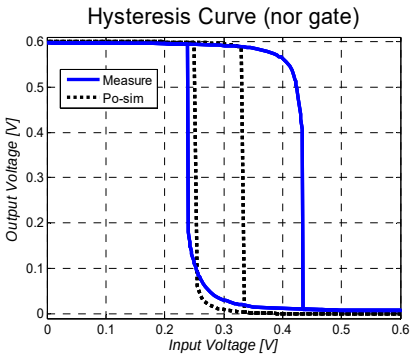


Fig. 17. Hysteresis curve of DTMOS S. T. nor gate.

TABLE VI.
Measurement and simulation result of Schmitt Trigger nor gate

Parameter	Value	
	Simulation	Measurement
Voltage Power	0.6V	
V_{LH}	0.332 V	0.434 V
V_{HL}	0.254 V	0.239 V
Hysteresis width	78 mV	195 mV
Offset voltage	0.293 V	0.336 V

Figure 17 and Table VI shows measurement and simulation result of S. T. nor gate. Test procedure is the same as before.

5) Schmitt Trigger gate test circuit

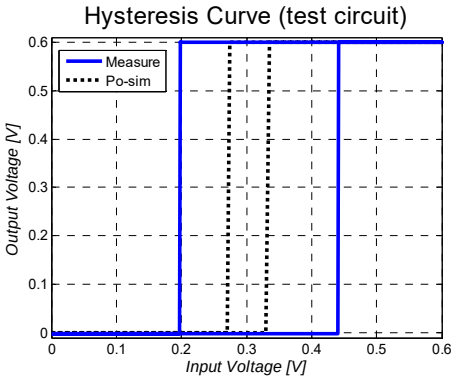


Fig. 18. Hysteresis curve of DTMOS S. T. test circuit.

TABLE VII.
Measurement and simulation result of test circuit

Parameter	Value	
	Simulation	Measurement
Voltage Power	0.6V	
V_{LH}	0.335 V	0.441 V
V_{HL}	0.273 V	0.197 V
Hysteresis width	62 mV	244 mV
Offset voltage	0.304 V	0.319 V

Almost DTMOS S. T. logic gates have enough hysteresis width. It means that these DTMOS S. T. logic gates have an enough noise margin. But, there is a little offset difference between simulation and measurement result.

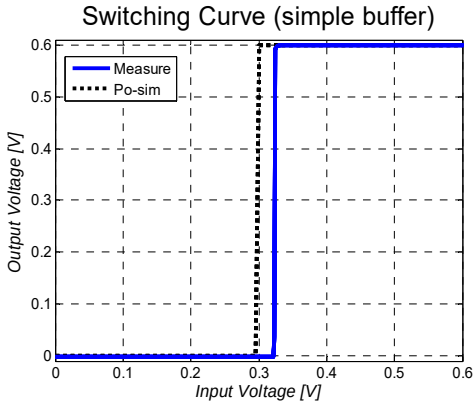


Fig. 19. Switching curve of simple CMOS buffer.

We can determine the cause of the problem through figure 19. Figure shows a switching curve of simple CMOS buffer. Simulation result is black dash line, and measurement result is blue line. As shown in figure 19, zero to vdd conversion point is higher than half vdd. It shows that PMOS transistor is stronger than NMOS transistor.

To verify our analysis, we modified simulation set-up. Original PMOS:NMOS ratio was 2u:2u. but in this time, we change this PMOS: NMOS ratio value to 4u:2u.

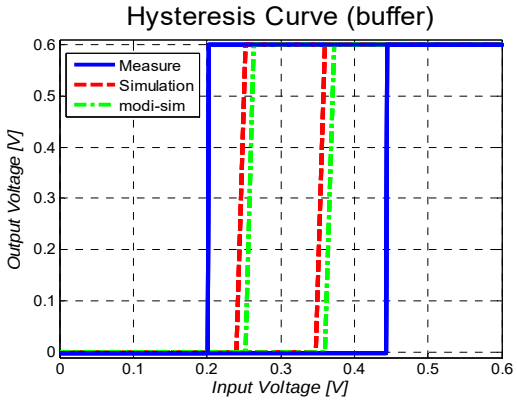


Fig. 20. Hysteresis comparison between measurement and simulation.

In Figure 20, we can see offset shifting by changing PMOS NMOS ratio. Green dash line is modified simulation result, and red dash line is original simulation result.

IV. CONCLUSIONS

In this project, the frequency hopping is applied to the DC-DC converter to reduce the EMI generating from the switching activities of the converter. The spectrum of all importance node of the DC-DC converter is analyzed to find the dominant source that generating EMI. Based on the voltage spectrum measured, the switching node has the highest magnitude which is 23 dBV higher than the output node. The switching node is concluded as the main EMI source of the DC-DC converter.

By applying the frequency hopping technique, the spectrum of both switching and output node is reduced. The control frequency of the frequency hopping technique has affect the spectrum reduction amount. The optimize frequency is found at 800 KHz during the experiment process, and the maximum 8 dBV reduction on spectrum is archived by applying the hopping frequency technique.

In this IoT era, most devices are getting smaller and smaller. Chip size also scaled down. In this situation, signal reliability and noise immunity can be a very important issue. This paper introduces the DTMOS S. T. logic gates which can improve noise immunity having hysteresis width.

Using 0.18um process, these S. T. logic gates are fabricated and they have over 200mV hysteresis width under 0.6V VDD environment.

Further measurement can be done on verifying the circuit level noise immunity enhancement using example circuit. And, Delay and Power consumption will be measured later. Then, the feature of DTMOS S. T. logic gates can be more clearly.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. NRF-2014R1A2A2A01006595). This work was supported by the IC Design Education Center (IDEC).

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