Design of Dual Mode DC-DC Buck Converter Using Segmented Output Stage

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***Abstract* - This paper presents a dual mode DC-DC buck converter using a segmented output stage. It operates in the SFM (switching frequency modulation) mode under light load and the PWM (pulse width modulation) mode under heavy load to enhance power efficiency over wide range loads. Also an output stage is segmented under light load in order to decrease switching power dissipation. The proposed circuit has been designed in a 0.35 μm CMOS process. Simulation results show that the circuit receives an input voltage of 2.9 V~4.2 V and generates an output voltage of 1.75 V~2.0 V. Also, the circuit has a maximum efficiency of 93.8% over the load current range of 10 mA~200 mA.**

I. INTRODUCTION

As the use of battery operated portable devices is rapidly increasing, it is required to develop highly power efficient PMICs (power management ICs) for long battery life in order to realize multiple functions and variable output voltages in the portable devices [1-2].

Among these PMICs, DC-DC converters are widely used in portable devices because they provide high efficiency. Recently, as DC-DC converters are required to have high efficiency, low area, and various output voltages, many researches have been actively conducted [3-14].

In general, operation modes of mobile devices change from standby mode with light load to communication mode with heavy load. However, such mobile devices have long usage time in the standby mode, and it is very important to improve the efficiency of the DC-DC converter under light load [8-14].

DC-DC converters are classified as PWM (pulse width modulation) mode and PFM (pulse frequency modulation) mode according to a switching control method [3-7]. In the conventional DC-DC converters, the PWM mode is mainly used, but there is a problem that power efficiency is low due to a lot of power consumption due to excessive switching operations under light load. To overcome this low power efficiency under light load, some approaches have been proposed using the PFM mode which controls on or off state of power switching transistors by changing switching frequency with constant duty ratio [8-9]. Also, in order to provide higher efficiency over a wide load range, some dual-mode approaches have been proposed combining the PFM or the SFM (switching frequency modulation) mode under light load and the PWM mode under heavy load [10-12].

In general, a DC-DC converter uses power switching transistors with large ratio of W/L to facilitate driving a large load current. However, the large sized transistors result in a lot of switching loss under light load. In order to achieve high power efficiency under light load, some approaches have been proposed which vary the width of the power transistor depending on load current [13-14]. However, additional complex circuits, such as some digital blocks or ADCs are needed to implement the load adaptive width scaling scheme.

In this paper, we design a PWM/SFM dual-mode DC-DC buck converter using a segmented output stage. The converter operates in the SFM mode under light load and the PWM mode under heavy load using a small PWM/SFM controller which generates switching signals of power switching transistor, and an output stage is segmented using a simple comparator to enhance power efficiency under light load.

In Section II, a design of a dual mode DC-DC buck converter using a segmented output stage is presented. Implementation results are described in Section III. And finally, conclusions are made in Section IV.

II. DESIGN OF DUAL MODE DC-DC BUCK CONVERTER USING SEGMENTED OUTPUT STAGE

In this section, we introduce a design of a PWM/SFM dual mode DC-DC buck converter using a segmented output stage. The DC-DC buck converter operates in dual mode, i.e. the SFM mode [9] under light load and the PWM mode under heavy load. And the buck converter has a segmented output to improve its power efficiency under light load.

Fig. 1 is a block diagram of a dual mode DC-DC buck converter using a segmented output stage. The circuit consists of a PWM/SFM controller which generates the switching signals of power switching transistors, segmented gate drivers to control power switching transistors according

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to load current, and an error amplifier for comparing the feedback voltage V_F with the reference voltage $V_{ref,E}$ to change output voltages, based on a power circuit block with power transistors and LC filter.

The converter operates using a current-mode control that keeps the output voltage constant by detecting the output voltage and the inductor current. The converter detects the output voltage of the error amplifier and changes the frequency of VCO (voltage controlled oscillator) in the PWM/SFM controller.

Switching transistors are driven using a set clock signal V_{setclk} and a reset clock signal $V_{resetclk}$. The set clock signal V_{setclk} for controlling power switching transistor is generated using the VCO with frequency proportional to the load current until load current reaches at the given current $I_{Load,C}$. The reset clock signal $V_{resetclk}$ is generated by detecting the inductor peak current to determine the duty ratio of switching signal.

When a load current is at light load with less than a given load current $I_{Load,C}$, the frequency of the set clock signal increases as the load current increases, which operates in the SFM mode.

On the other hand, when load current is at heavy load with more than a given load current $I_{Load,C}$, the frequency of the set clock signal is constant, but the reset clock signal is generated in time away from the set clock signal and duty ratio D increases as the load current increases, which operates in the PWM mode.

A segmented output stage circuit is included to reduce switching loss due to excessive switching operations at light load. When the load current is less than a given value, only gate driver1 is turned on and switching transistor operates with scaled-down size to reduce the switching loss.

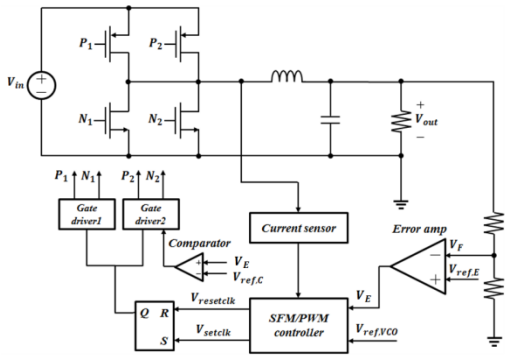

Fig. 1. Block diagram of a dual-mode DC-DC buck converter using a segmented output stage.

A. A PWM/SFM controller

A PWM/SFM controller makes DC-DC converter operate in the SFM mode under light load and the PWM mode under heavy load, according to load current. Fig. 2 shows a proposed PWM/SFM controller circuit. Unlike conventional dual mode circuits, we introduce a PWM/SFM mode controller using VCO.

The VCO receives the error voltage V_E and generates a set clock signal V_{setclk}. Because the error voltage is proportional to load current, the frequency of V_{setclk} increases up to a given frequency of VCO as the load current increases. Also, the ramp voltage V_{Ramp} is generated using current source I_{osc}, capacitor C_{osc} and transistor M_1 and is combined with inductor current to generates a reset clock signal $V_{resetclk}$.

Fig. 3 shows some waveforms of PWM/SFM controller according to load current. When the load current is less than $I_{Load,C}$, the frequency of V_{setclk} increases as the load current increases. In the contrary, when the load current is more than $I_{Load,C}$, the frequency of V_{setclk} is constant. And as the load current increases, the time difference between the clock signal of V_{setclk} and the clock signal of $V_{resetclk}$ increases and the duty ratio D of the switching signal is larger.

Compared with the conventional PWM/PFM dual mode, because our PWM/SFM dual mode doesn't need a separate mode controllers, it can be implemented in small circuit.

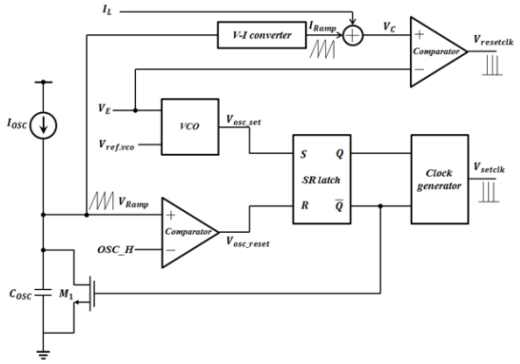

Fig. 2. A PWM/SFM controller.

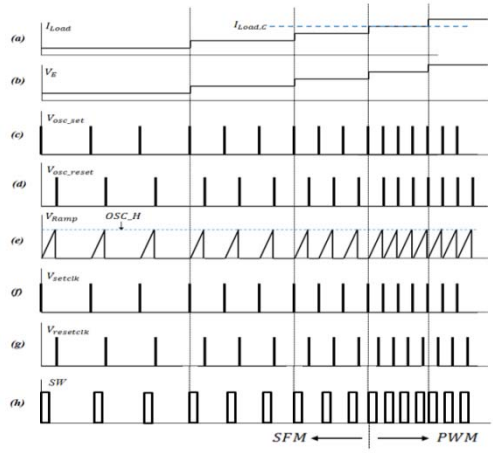

Fig. 3. Waveforms of PWM/SFM controller.
(a) the load current I_{Load}, (b) the error voltage V_E,
(c) the oscillation set clock V_{osc_set},
(d) the oscillation reset clock V_{osc_reset}, (e) the ramp voltage V_{Ramp},
(f) the set clock V_{setclk}, (g) the reset clock $V_{resetclk}$,
(h) the switching pulse SW

B. A segmented output stage

A segmented output stage is used to improve power efficiency of light load. Fig. 4 shows a segmented output stage circuit. The segmented output stage circuit consists of a single comparator, two segmented gate drivers, and two segmented switching transistors. The output of a comparator is applied to the enable signal of the segmented gate driver(2) to segment switching transistors. When load current is at

light load with less than a reference load current, the switching transistor SW_{P2} and SW_{N2} are turned off to reduce the size of the switching transistor and then switching loss can be reduced.

Compared with conventional methods using some digital blocks and an ADC, our circuit is simply implemented in a small circuit using a simple comparator.

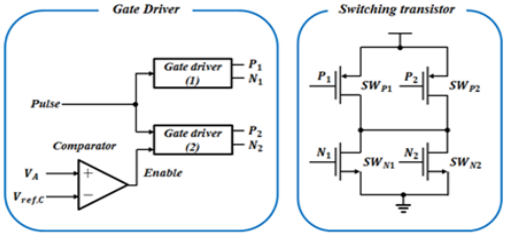

Fig. 4. Segmented output stage circuit.

Fig. 5 shows some waveforms of the segmented output stage depending on load currents. In the case of light load, only SW_1 is turned on to reduce the size of the switching transistor. On the contrary, for heavy load both SW_1 and SW_2 are turned on.

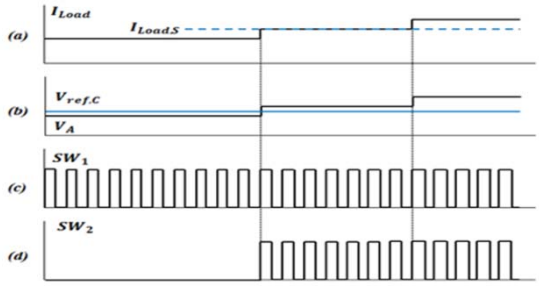

Fig. 5. Waveforms of segmented output stage
(a) the load current I_{Load}, (b) the reference voltage $V_{ref,C}$ and the error voltage V_A, (c) the switching transistor SW_1, (d) the switching transistor SW_2

III. IMPLEMENTATION RESULTS

The proposed dual mode buck converter has been implemented in a 0.35 μm CMOS process. TABLE I shows performance results with design specifications. Fig. 6 shows the layout of the chip. The area of core chip is 1.18 μm × 1.38 μm. Switching transistors, a bandgap reference, VCO and gate drivers are designed.

TABLE I. Performance results

Item	Specification	Simulation
V_{in}	2.9 V ~ 4.2 V	2.9 V ~ 4.2 V
V_{out}	1.75 V ~ 2.0 V	1.75 V ~ 2.0 V
Ripple voltage	2 mV	1.6 mV
I_{MAX}	200 mA	200 mA
Line regulation	< 1 %/V	0.3 mV (0.017%)
Load regulation	< 1 %/V	1.7 mV (0.097%)
Line transient	< 50 μs	22.9 μs
Load transient	< 50 μs	25.4 μs
Efficiency	> 80 %	78 % ~ 93.8 %
Frequency	0.8 MHz ~ 1.5 MHz	0.8 MHz ~ 1.5 MHz

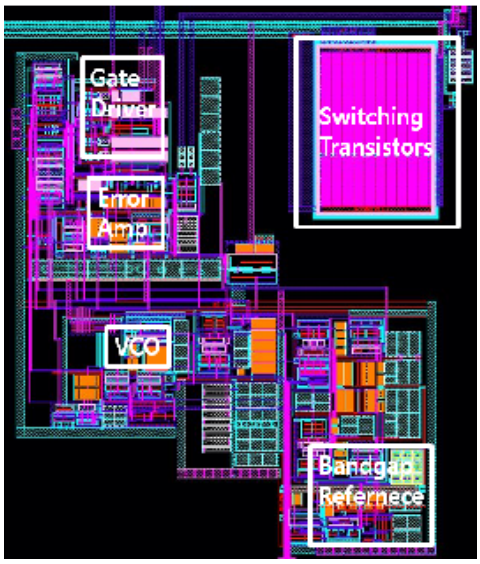

Fig. 6. Layout.

A. Output voltage characteristics

Fig. 7 and TABLE II show output voltage characteristics for input voltage of 3.3V. The output voltage varies from 1.75 V to 2 V with ripple of 1.6 mV by a control input OVC.

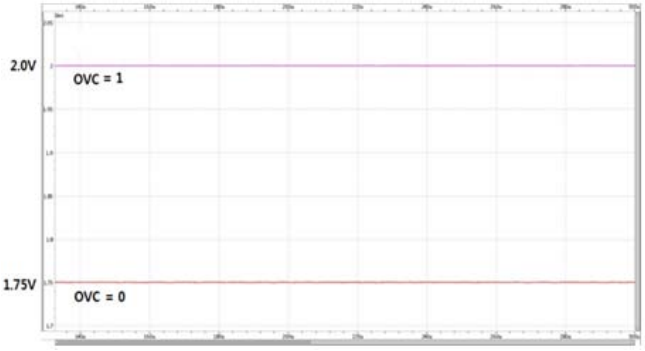

Fig. 7. Output voltage characteristics.

TABLE II. Output voltages according to OVC.

V_{in}	I_{Load}	OVC	Reference voltage
3.3	10	0	1.75
3.3	10	1	2.0
Ripple voltage			1.6 mV

B. Regulation and transient response characteristics

Fig. 8 and TABLE III show the transient reponses. When the input voltage changes from 2.9 V to 4.2 V under load current of 100 mA, output voltage has variation of 0.3 mV. And when the load current changes from 10 mA to 200 mA at the input voltage of 3.3 V, the variation of the output voltage is 1.7 mV as shown in Fig. 9 and TABLE IV.

Fig. 10 and Fig. 11 show the characteristics of a line transient and a load transient, respectively. When the input voltage changes from 3.3 V to 3.8 V with 5 ms period and a 10 μs slope under load current of 100 mA, the transient response is 22.9 μs with overshoot of 1.14 mV. And when the load current varies from 10 mA to 100 mA with a slope of 10 μs for 3.3 V input voltage, load transient is 25.4 μs with the overshoot of 5.01 mV.

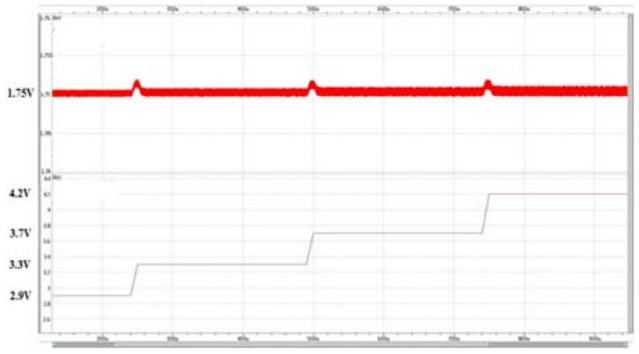

Fig. 8. Line regulation characteristics.

TABLE III.
Output voltages according to input voltages.

V_{in} [V]	Load current [mA]	V_{out} [V]
2.9	100	1.7502
3.3	100	1.7503
3.7	100	1.7504
4.2	100	1.7505
Output voltage variation		0.3 mV
Output voltage variation rate		0.017 %

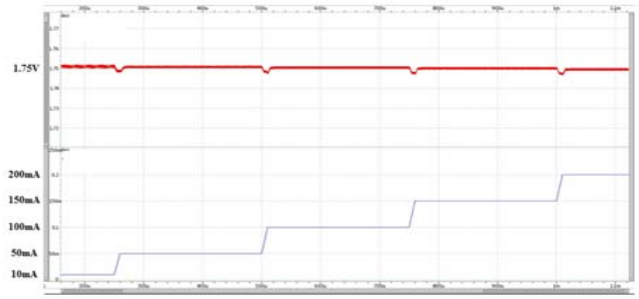

Fig. 9. Load regulation characteristics.

TABLE IV.
Output voltage according to load current.

V_{in} [V]	Load current [mA]	V_{out} [V]
3.3	10	1.7508
3.3	50	1.7506
3.3	100	1.7503
3.3	150	1.7499
3.3	200	1.7491
Output voltage variation		1.7 mV
Output voltage variation rate		0.097 %

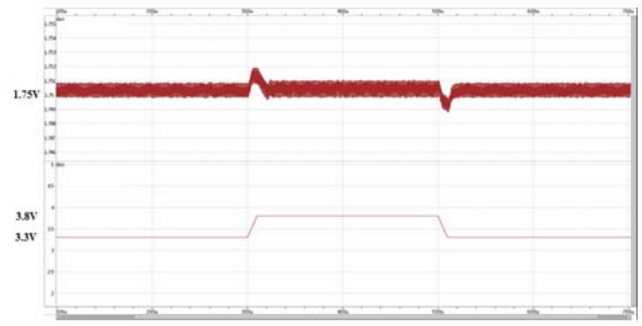

Fig. 10. Line transient characteristics.

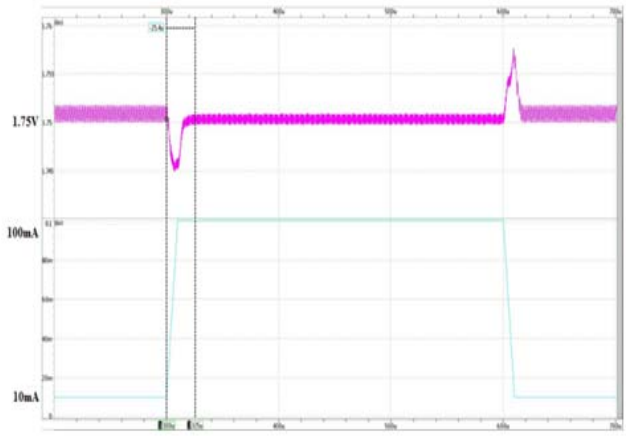

Fig. 11. Load transient characteristics.

C. Power efficiency

Fig. 12 shows simulation results of power efficiency of the buck converter with the input voltage of 3.3 V and the output voltage of 1.75 V. Our method (a) (dual mode + segmented output stage) has the power efficiency of 78%~93% under the load current of 10 mA~50 mA, which is 3% higher than the method (b) (only PWM mode + segmented output stage). And our power efficiency is 7% higher than the method (c) (PWM mode only) under the load current of 100 mA. Consequently, our proposed controller with dual mode and segmented output stage has higher power efficiency, compared to the converter using a single PWM method or without segmented output stage.

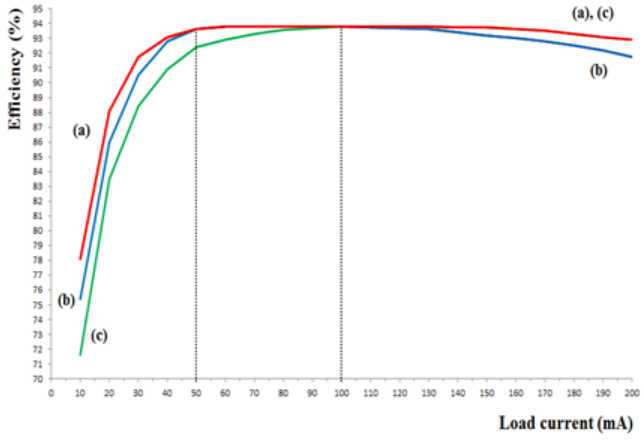

Fig. 12. Power efficiency.
(a) our proposed method (dual mode + segmented output stage),
(b) only PWM mode + segmented output stage, (c) PWM mode only

D. Comparison

TAVLE V shows the comparison of the electrical characteristics for this work and the previous researches [12-14]. The simulation results show that the power efficiency of the proposed buck converter is higher than [13] (PFM mode + segmented output stage) and [14] (PWM mode + segmented output stage) and is lower than [12] (PWM/PFM dual mode). However, this work is simpler and smaller in size than [12] due to a simple PWM/SFM controller.

TABLE V.
Comparison of electrical characteristics of DC-DC converter.

	[12]	[13]	[14]	This work Simul.
Design process	0.35 μm CMOS	-	0.13 μm CMOS	0.35 μm CMOS
Converter type	Buck	Buck	Buck	Buck
Mode	PWM/PFM	PFM	PWM	PWM/SFM
Segmented output stage	x	○	○	○
Input voltage [V]	2.7~5	5	3.3	2.9~4.2
Output voltage [V]	1~1.8	1.8	1.2	1.75~2.0
Output current [mA]	3~400	10~2000	1~1000	10~200
External capacitor [μF]	10	40	-	10
External inductor [μH]	10	2.2	-	4.7
Switching frequency [MHz]	0.1~0.6	1	2	0.8~1.5
Circuit size [μm]	1.89 × 1.89	-	1.15 × 1.20	1.18 × 1.38
Power efficiency [%]	85~95	61~89	20~89	78~93.8

IV. CONCLUSIONS

In this paper, a dual mode DC-DC buck converter using a segmented output stage has been designed. Dual mode is implemented by PWM/SFM controller using a VCO and a segmented output stage is designed with a simple comparator.

Simulation results using a 0.35 μm CMOS process show that the output voltage is regulated to 1.75 V~2.0 V with small ripple 1.6 mV for input voltage of 2.9 V~4.2 V. And the power efficiency is 78%~93% for the load current of 10 mA ~ 50 mA, which is 3%~7% higher than the previous methods using only PWM mode or unsegmented output stage.

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