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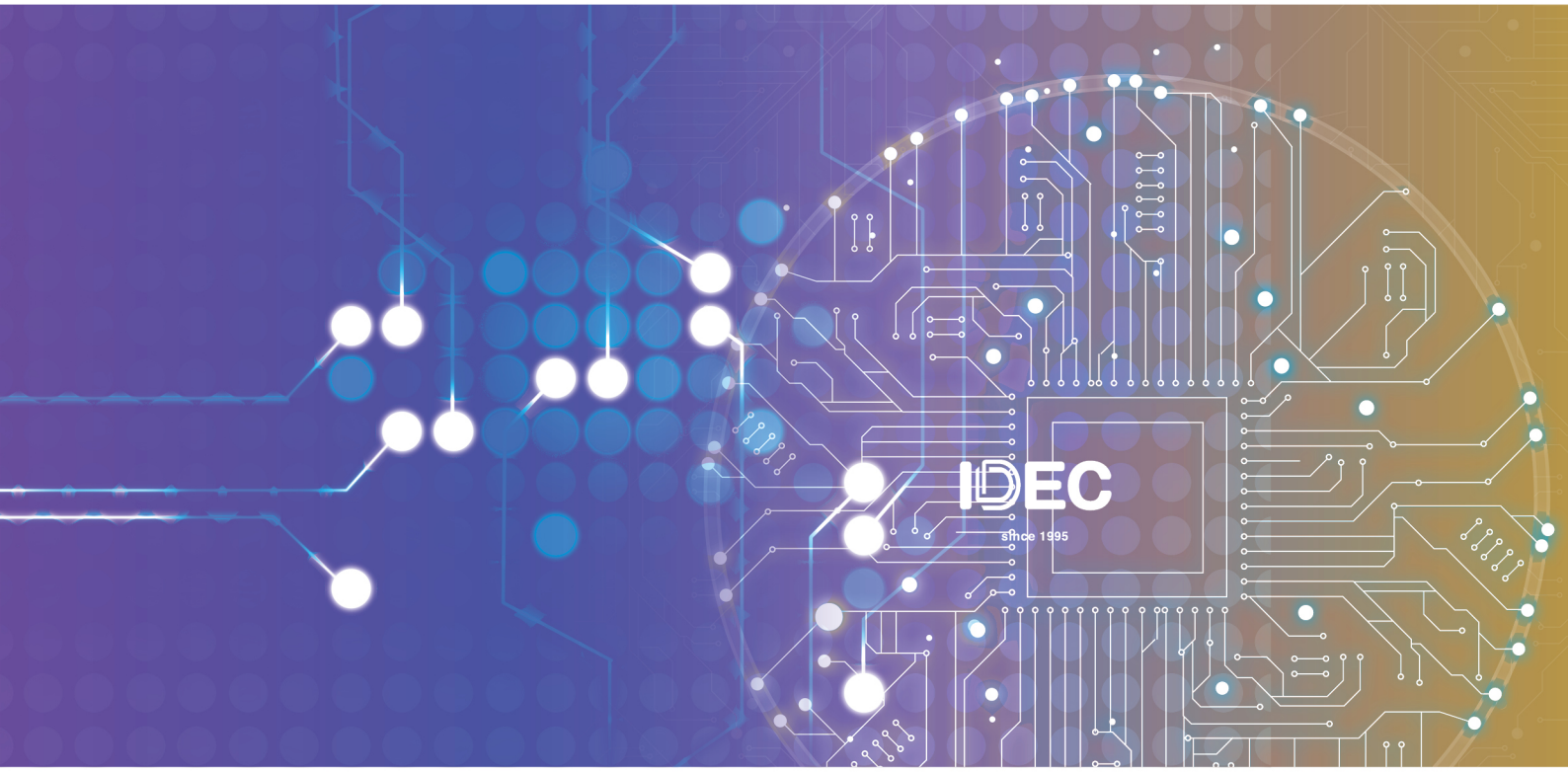

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Editorial Assistant

Kyung Ok Lee
(IC Design Education Center)
291 Daehak-ro, Yuseong-gu, Daejeon,
34141, Republic of Korea
Tel : 82-42-350-8533
Fax : 82-42-350-8540
E-mail : kyungoklee@idec.or.kr

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A 10.3125 Gb/s Deserializer for IEEE 10G-EPON Standard

Won June Hwang, Yun Sik Choi, Bo Yun Jung, and Kwang Hyun Baek
School of Electrical and Electronics Engineering, Chung-Ang University
E-mail : kbaek@cau.ac.kr

***Abstract* - The throughput requirement of high-speed interface such as wireline I/O and memory I/O has been increased even if the power budget for the interface circuits has been maintained and decreased. This paper, true single-phase clock logic and half-rate architecture to implement the 16-to-1 10.3125 GB/s deserializer is used to minimize the power consumption with remaining high-speed operation. The design method for essential block such as demultiplexer, clock data recovery circuit, continuous time linear equalizer, decision feedback equalizer and lock detector is also described in paper. The designed deserializer is fabricated through 65nm CMOS process and dissipate about 200mW is satisfied with IEEE standard. The developed deserializer has BER 10^{-12} with PRBS 2^9-1.**

***Keywords*—Deserializer, Ethernet, High speed interface**

I. INTRODUCTION

As data traffic for services such as 5G, high-resolution video streaming, and IoT is rapidly developing, the demand for high-speed interface is rising sharply. A high-speed interface circuit must overcome several challenges including high speed operation, equalization techniques, and low power consumption. The developed 1:16 10.3125Gb/s deserializer which converts high-speed serial data to parallel data is for 10G-EPON IEEE standard. As shown in Fig. 1, the deserializer consists of equalizer to compensate for distorted data, 1:16 demultiplexer, clock and data recovery circuit (CDR). In the 10.3125Gb/s deserializer, the key blocks are CDR and equalizer. The CDR aligns the clock to the center of the data and recovers the clock by using the input data. The developed CDR is continuous type of CDR because the data packet in Ethernet system is continuously transmitted. In order to minimize the malfunction of CDR, in this paper, the new architecture of Bang-Bang phase detector (BBPD) is proposed. Also, the lock detector based on a counter for the exact loop selection between frequency detection loop and phase detection loop in CDR is implemented. The developed lock detector is able to change the resolution, which results in making the flexibility of the frequency of data. Because the CDR recovers the clock by the information of the data, the slope information of data is critical. However, due to channel loss, the data is distorted, which causes to disappear the slope information of data. In order to prevent this problem, the equalizer is necessary. In developed deserializer, two types of the equalizer are implemented. One is continuous-time linear equalizer (CTLE) that compensates for the lag between pre-cursor and post-cursor of the distorted data. Because the operation of CTLE is like the amplifier operating at the specific frequency, the CTLE could amplify the noise at the specific frequency. This characteristic of CTLE may distort the data. Because of this reason, the decision-feedback equalizer (DFE) that compensates only for post-cursor of the distorted data is also developed. Because the DFE is optimized for post-cursor of the distorted data, it is usually employed for the channel that is severe in terms of reflection. Therefore, the CTLE and DFE are developed for 10G-EPON deserializer.

In order to design low power deserializer with high-speed operation, half-rate architecture and true single-phase clock (TSPC) logic are employed. Thanks to the above mentioned techniques, a 10.3125 Gb/s 16-to-1 deserializer for IEEE 10G-EPON has been successfully designed in this paper. Each parts are described in following sections and the performance results and specifications are summarized. The conclusion is drawn in section IV.

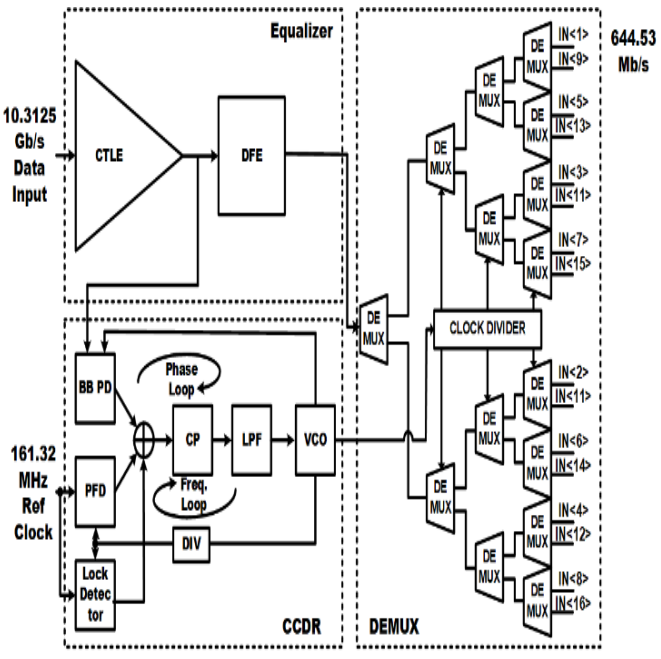

Fig. 1. Block diagram of the developed deserializer

a. Corresponding author; kbaek@cau.ac.kr

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II. IMPLEMENTATION

A. 1 to 16 Demultiplexer (DEMUX)

The demultiplexer circuit converts the serial data to parallel data. The block diagram of the 2-to1 demultiplexer is presented in Fig. 2. The input data is aligned by rising and falling edge of clock at first. In order to align the order of the data, the additional latch is employed at the line of D1. Through this operation, the data packet is consequently separated. In demultiplexer, because the data is separated by the clock having the same data rate, the rising and falling time of clock has to be identical. Conversely, if the duty of the clock is different, commonly additional jitters are caused. The clock of latch should stay above 0.8UI in order for the latch to have the gain to increase or remain the amplitude of output swing. If not, the time to simultaneously turn input switched on the increase, which leads to reduce the time spent to increase the output amplitude. In other words, the turn-off time of input switches is decreased. Because of these reasons, the clock distribution and slope in demultiplexer are essential factors. The block diagram and layout of the developed demultiplexer are shown in Fig. 3. The input data rate is 10.3125Gb/s serial data and the output data rate is 644.53Mb/s parallel data. The structure of the developed demultiplexer is third-type in order to have an identical clock delay [1]. By locating clock driver at the center of the 1:16 demultiplexer, the clock can have the almost same clock delay.

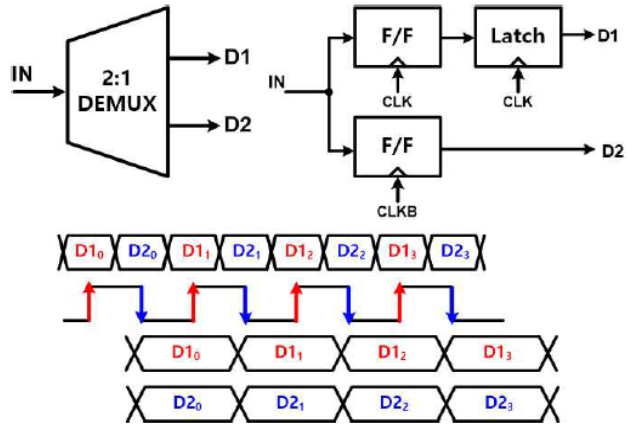

Fig. 2. Block diagram and timing diagram of demultiplexer

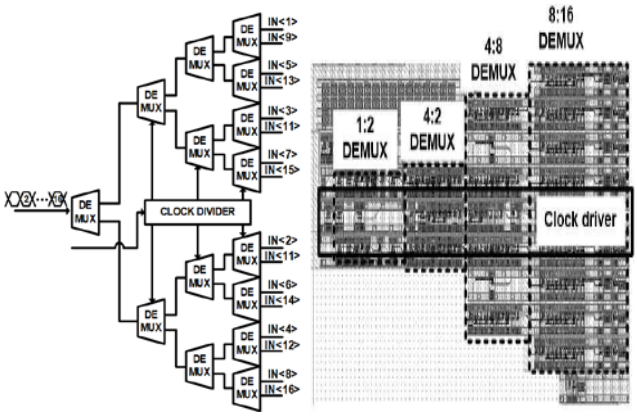

Fig. 3. Block diagram and layout of the developed demultiplexer

B. Clock and Data Recovery Circuit

The deserializer is only able to obtain the data from the serializer due to the problem caused by the skew between data and clock. Because of this reason, a circuit is needed to recover the clock by utilizing the received data. It is referred as to Clock and Data Recovery Circuit (CDR). The CDR's major function is to align the rising edge of the clock to the center of the data. The operation flow of CDR is as follows: Firstly, the frequency of the required clock is set in frequency locked loop by the reference clock. Then, the frequency of the clock is evaluated by the lock detector. If the result is correct, the phase loop operates in order to align the rising edge of the clock to the center of the data with the frequency locked loop off.

As aforementioned, the CDR can detect a transition of data and the difference between the received data and recovered clock by using frequency loop in CDR. Through this operation, the timing circuit in demultiplexer is able to have the set-up time which is about the half of the T_{data} period, making the timing circuit robust when it operates at high frequency domain. In order to find the ideal sample point, the phase detector is indispensable. For this reason, a binary phase detector (BBPD) is employed. The BBPD compares the phase of the input data with the phase of clock by using four flip-flops and two XOR gates. Fig. 5 shows the gain of BBPD is ideally infinite [2]. The BBPD can be

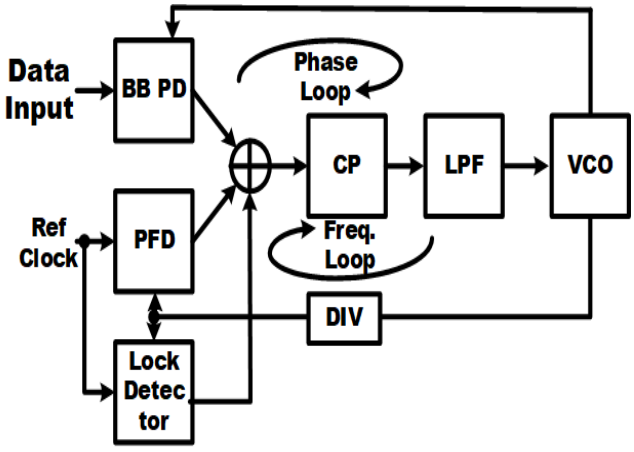

Fig. 4. Block diagram of clock and data recovery circuit

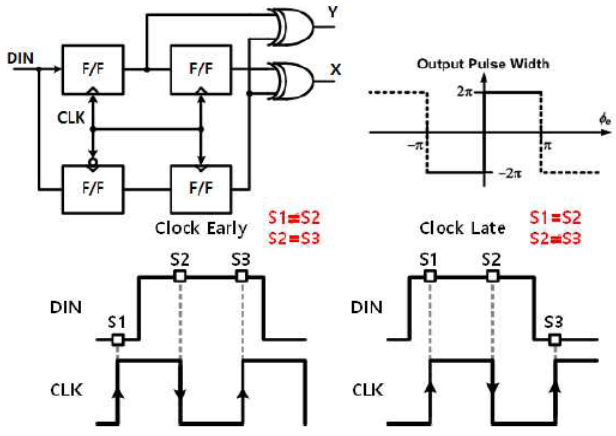

Fig. 5. Block diagram of bang-bang phase detector

implemented with two XOR gates and two timing circuits. If the clock arrives earlier than the data, the BBPD provides the information to delay the clock with the charge-pump. On the contrary, if the clock arrives later than the data, the BBPD provides the information which enables clock to reach faster. In order to distinguish whether the clock arrives early or late, the BBPD uses three sampled data by using the consecutive edge of the clock. As shown in Fig. 5, if the data sampled by the first clock edge is different from the others, the clock is located early. Conversely, if the consecutive sampled data of the first and second clock edge is the same and is different from the last one, the clock is late. However, the BBPD causes several problems in high-speed operation. The rising and falling edge of S1 and S3 are different from that of S2 due to the unequal output load of the timing circuits. Also, the clock skew delays the propagation of S1, S2, and S3, which provokes the malfunction of XOR gates. Therefore, the errors occur as shown in Fig. 6. The simulation verifies this phenomenon. If the load of S1 and S3 are smaller than 3.5 times compared with the load of S2, the average sum of up signal is equal to that of down signal, which causes the clock not to be in the center of the data. In this paper, in order to overcome this problem, the BBPD with re-aligned flip-flops is proposed. Fig. 7 shows the proposed BBPD that connects with four flip-flops at the output node of the

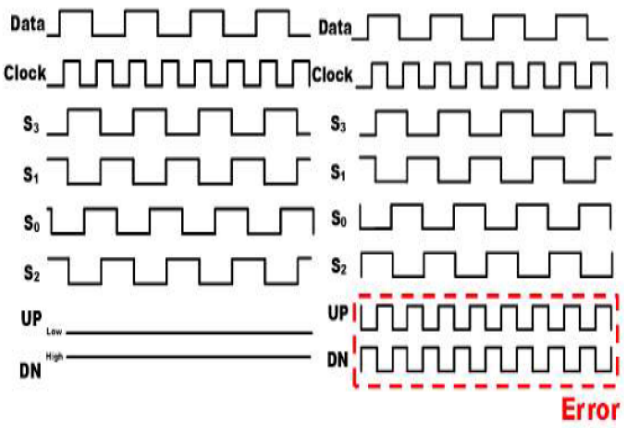

Fig. 6. Error of the conventional bang-bang phase detector

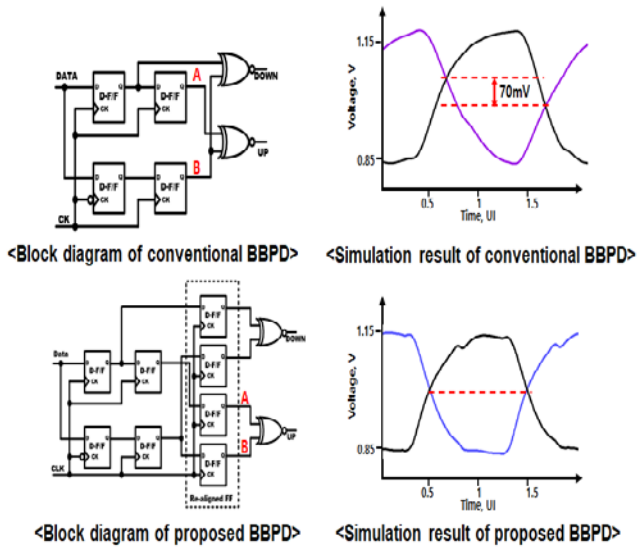

Fig. 7. Comparison between conventional and the proposed BBPD

convention BBPD. Since the loads of the final flip-flops are equal and the rising and falling time are identical, it leads to reduce the burden of the XOR gates. At the last timing circuit stage, the data is realigned with the same clock. As shown in Fig. 7, when the conventional BBPD is utilized for a 10.3125Gb/s system, the amplitude difference of midpoint of data is about 70mV. However, if the proposed BBPD is adopted for the same system, the difference of the midpoint of data is almost zero, which allows to effectively increase the bandwidth of XOR gates.

C. Lock Detector (LD)

The lock detector (LD) whose key role is to switch the frequency loop to the phase loop has an important role in CDR. If a LD malfunctions when it evaluates the frequency, the BBPD cannot align the clock to the center of the data. As shown in Fig. 8, a phase-based LD is able to compare reference clock with a divided clock of VCO in terms of phase. The output of LD is low as soon as the CDR is turned on. Afterwards, the phase-based LD continuously compares the delayed-divided clock. If the rising edge of the delayed-divided clock is located at the gap between reference and delayed reference clock, the frequency is locked. As a result, the output of LD is expected to be high. However, two types of problems may occur in terms of frequency and phase. In practice, the difference between the reference and delayed frequency occurs.

Because of this reason, the phase difference is accumulated by the difference of frequency, which causes that lock state becomes off even if the frequency loop is done. Another one is the difference in terms of phase. Even though the frequency of reference and the divided is the same, the phase offset may occur due to the mismatch of the charge pump and unexpected spur by the power supply. In

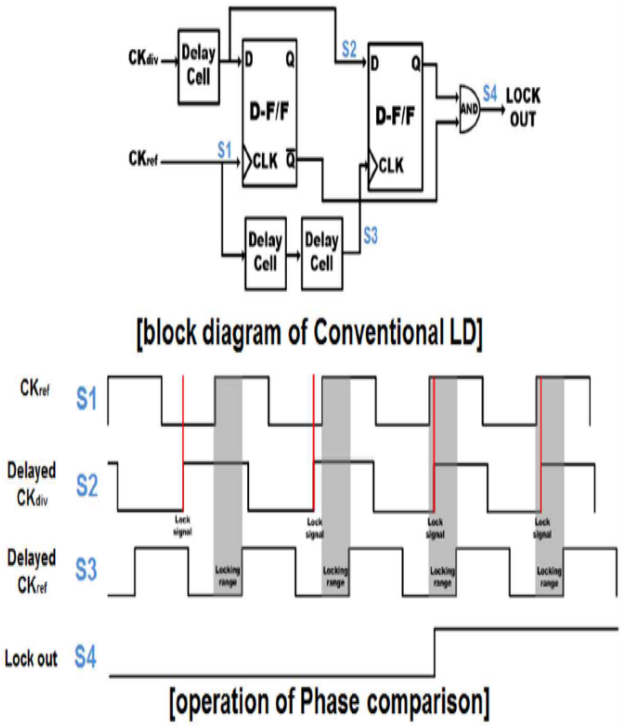

Fig. 8. Block diagram and operation of phase-based lock detector

the case of this phenomenon, the output of the lock detector is always low. Simply, in order to overcome these problems, it is easy for delay cells to be controlled. However, the optimized delay cannot be found due to the variations of PVT. Consequently, the method of phase-based LD is unstable due to using the phase difference. Because of these problems, in this paper, the LD based on the synchronous digital counter by the clock is used. Also, the method of the employed is based on the frequency difference. As shown in Fig. 9, the counter-based LD consists of N-bit counters, the timing circuits for aligning reference and divided clock, the resolution control circuit, and the lock decision circuit. The basic principle of the counter-based LD compares the number of the counter for reference clock with the number of the counter for divided clock. If the number is the same within the specified time, this state is called lock. Fig. 10 shows the timing diagram of the operation for the counter-based LD. As aforementioned, if the number of counters for the divided clock is 2^n-K and it is located within the range from 2^n-(K-1) to 2^n-(K+1) of locking for reference clock counter, this state is lock. And then the reset is operated in order to prevent to accumulate the phase error.

Fig. 11 shows the N-bit asynchronous counters in the LD. Because this is asynchronous counter, the layout of reference and divided clock line should be careful. By using the interested count number, the LD makes one pulse and lock window.

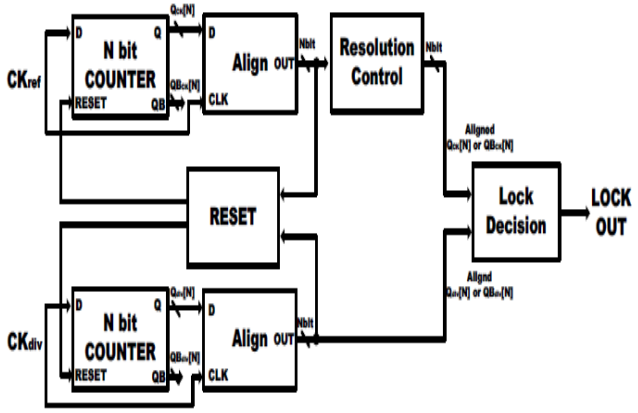

Fig. 9. Block diagram of the proposed lock detector

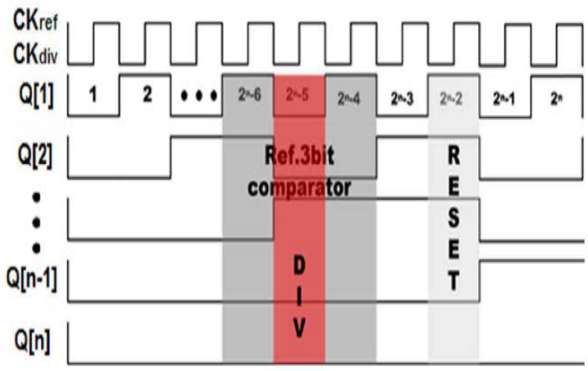

Fig. 10. Operation method of the counter-based lock detector

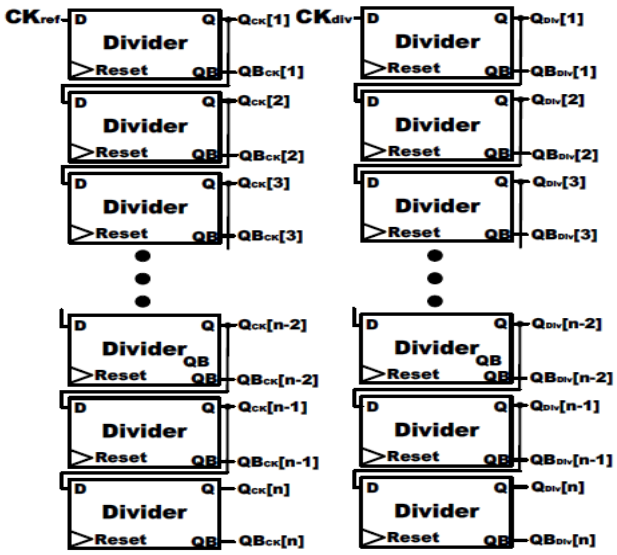

Fig. 11. N-bit counter having reset function in the counter-based LD

D. Continuous Time Linear Equalizer

The CTLE that acts as the high-pass filter and boosts the gain at the interested frequency can compensate for channel loss. The CTLE is able to eliminate pre-cursor and post-cursor ISI. Generally, CTLEs have both active and passive types. The passive CTLE made of resistor and capacitor is presented in Fig 12 [3][4]. On the contrary, the active CTLE includes an amplifier with high-pass characteristics, meaning that the gain is decreased in the active CTLE at low-frequency.

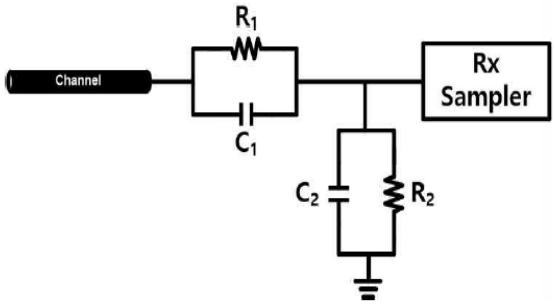

Fig. 12. Block diagram of passive continuous time linear equalizer

Because the passive equalizer has poles and zeros, the peaking gain is commonly generated after the zero in the passive equalizer. Since the passive equalizer consists of passive components, the gain at high-frequency is produced by degrading the gain at low-frequency. The value of gain and frequency for the peaking are determined by modifying the value of resistor and capacitor. The passive equalizer does not require additional power and has great linearity. On the other hands, larger space is needed compared to other equalizers, and the passive equalizer is not able to make the additional gain at Nyquist frequency. Because of this reason, in order to overcome the disadvantages of the passive equalizer, the active equalizer is presented. Fig. 13 shows a schematic of the active CTLE [5]. The active CTLE is composed of the input pair transistors, current sources,

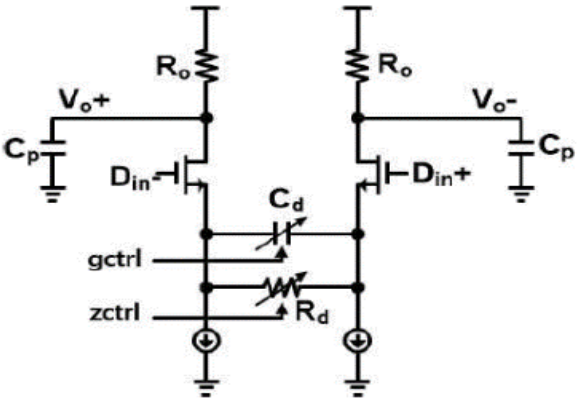

Fig. 13. Schematic and transfer function of active continuous time linear equalizer

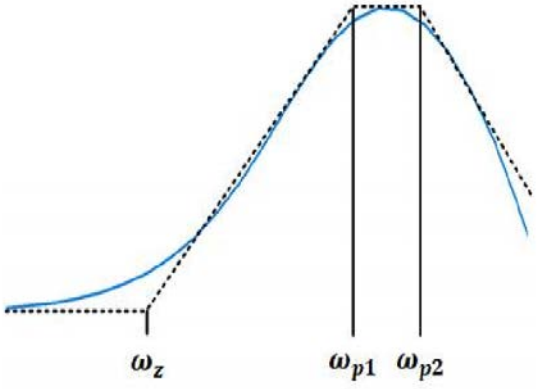

Fig. 14. Frequency response of active continuous time linear equalizer

output resistors, degeneration resistor to improve the bandwidth, and degeneration capacitor. The resistor and capacitor connected with the source of the input transistors determine the location of zeros and poles to make the peaking gain at the interested frequency. The transfer function of the active CTLE can be formulated as follows:

$$H(s) = \frac{g_m}{C_P} \frac{s+\frac{1}{R_d C_d}}{(s+\frac{1+\frac{g_m R_d}{2}}{R_d C_d})(s+\frac{1}{R_O C_P})} \quad (1)$$

$$\omega_z = \frac{1}{R_d C_d} \ , \omega_{p1} = \frac{1+\frac{g_m R_d}{2}}{R_d C_d} \ , \omega_{p2} = \frac{1}{R_O C_P} \quad (2)$$

The equation consists of one zero and two poles. The zero and pole at relatively low frequency are generated by degeneration resistor and capacitor. The last pole is dependent upon load capacitance. By using the Equation (1) and (2), the peaking gain at the interested frequency can be obtained.

$$Gain_{DC} = \frac{g_m R_O}{1+\frac{g_m R_d}{2}} \quad (3)$$

$$Gain_{Peaking} = g_m R_O \quad (4)$$

$$Peaking = \frac{Gain_{DC}}{Gain_{Peaking}} = \frac{\omega_{p1}}{\omega_z} = 1 + \frac{g_m R_d}{2} \quad (5)$$

As shown in Equation (3), (4), and (5), the frequency response of active CTLE for peaking gain is determined by zero and first pole. By the second pole, the interested frequency is finally decided. In order to design active CTLE, there are two factors to consider: First one is the amplitude of the received data should be within the input range of the active CTLE because the active CTLE is also an amplifier. Second one is that the current of the active CTLE is determined by the output load.

In the developed 10.3125Gb/s deserializer, the active CTLE is employed instead of the passive CTLE due to the area and the peaking gain. The block diagram of the developed active CTLE that consists of 3-stage active CTLE and bias circuits for 10.3125Gb/s deserializer is shown in Fig. 15. The received data is distorted by channel loss. The designed active CTLE recovers the data that can be recognized. Then, the output of the designed active CTLE would be connected with DEMUX, DFE, and CDR. The gctrl means the peaking gain control and zctrl means the location of zero control. In order to compensate for the channel loss by FR4 PCB line, coaxial cable, and the inductance of the package, in the filter cell, the resistor and the capacitor made by transistors are added. Therefore, the peaking gain and frequency is simply adjusted by the gate voltage of Rd and Cd. In order to prevent the variation of the common-mode voltage at the output, this feedback was necessary. Because this is replica circuit for the active CTLE, components should be matched with the transistors of the active CTLE. VTT was required for common-mode voltage. By using the feedback, the current of the filter cell was changed by the variation of Bias CS voltage in order to maintain the VTT voltage. In the developed active CTLE, the amplitude of the data is 400mV and VTT is 1V. The amount of current in the filter cell is about 350mA. Fig. 16 represents the simulation result indicating the peaking gain and frequency according to the variation of the gate voltage of gctrl and zctrl. As above mentioned, the simulation results verify that the peaking gain is changed according to the variation of the degeneration resistor and the peaking frequency is determined by the value of degeneration

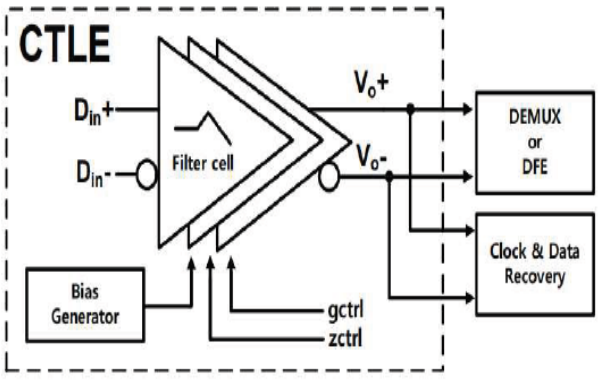

Fig. 15. Block diagram of active Continuous Time Linear Equalizer

capacitor. Fig. 17 shows the compensated frequency response at 10.3125Gb/s. The used insertion channel loss is -16dB at 10.3125Gb/s. At the frequency, the peaking gain of the active CTLE is 9.28 dB. As a result, the channel response becomes uniformed to the interested frequency. The eye-diagram having 260.1mV amplitude and about 0.86UI width is shown in Fig. 18.

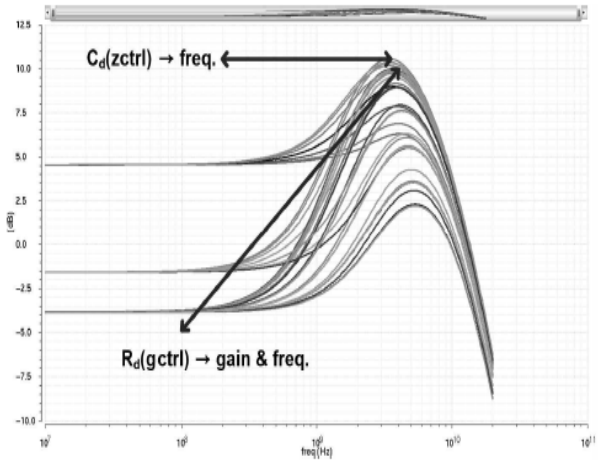

Fig. 16. Simulation results of peaking gain and frequency by control

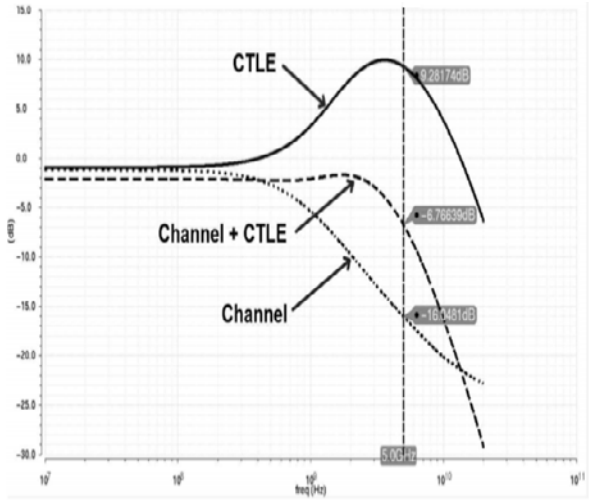

Fig. 17. Simulation results of the active CTLE with channel

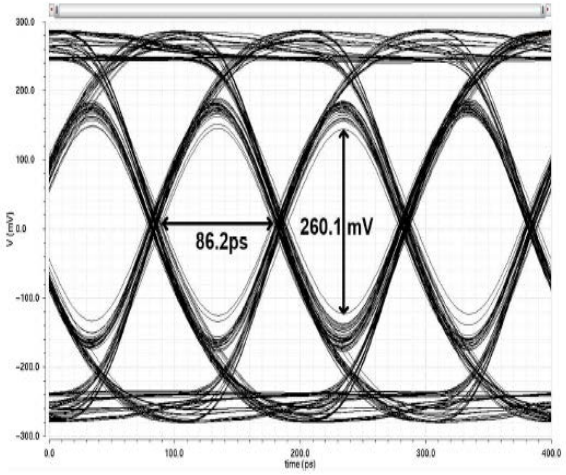

Fig. 18. Simulation results of the active CTLE with channel

E. Decision Feedback Equalizer

As aforementioned, the active CTLE can compensate for pre-cursor and post-cursor ISI with the characteristic of high-pass filter. Because of this reason, the noise could be generated, which results in making the ringing effect. The DFE can eliminate this type of ringing effect by removing the post-cursor ISI [6]-[10]. Therefore, DFE is located after CTLE. Fig. 19 shows the block diagram of the conventional DFE that is composed of decision slicer (flip-flop), 1-UI delay cells and the summer. The operation flow of the conventional DFE as follows: First of all, the initial data z_k is determined by the decision slicer. And then, d_k called the determined data is delayed with 1-UI. The more the number of the delay cell increases, the more the taps to weight W_k to the delayed cell also increases. The taps for weight have to be considered by the characteristics of the channel. Finally, the weighed data that is reflected by the channel response is summed or subtracted with the received data.

As shown in Fig. 20, the DFE is able to remove post-cursor ISI with the weighted delayed data. The advantage of the DFE is that the noise and crosstalk related to high frequency post-cursor ISI can be eliminated without amplifying the noise. On the other hands, the conventional DFE is not able to eliminate pre-cursor ISI, which could result in recovering the clock by using the received data due to the slow transition of the data. Also, because the conventional DFE has the feedback structure, there is a critical timing path.

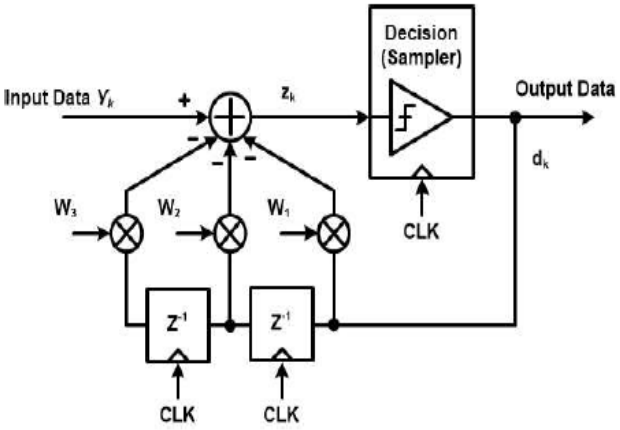

Fig. 19. Block diagram of the conventional decision feedback equalizer

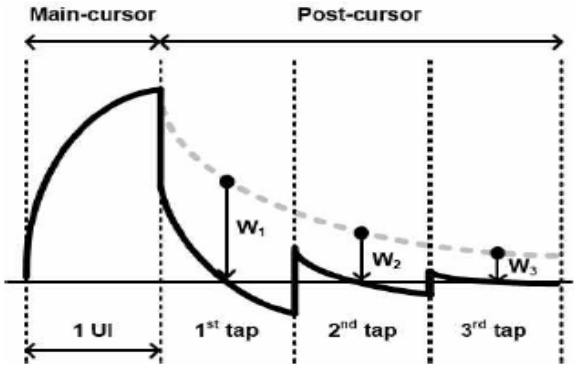

Fig. 20. The basic operation of the conventional decision feedback equalizer

F. Half-Rate Architecture and True Single-Phase Clock Logic

At the frequency beyond 10 Gb/s, the full-rate architecture dissipates significant power, because the power consumption of digital logic is proportional to the square of the frequency. On the other hand, a half-rate architecture can reduce a lot of power by using twice the slower clock. The current mode logic is generally used in high-speed circuit design due to its high operating frequency. But, unlike CMOS logic, static currents are constantly flowing, which consumes significant power. At 10 Gb/s, TSPC dissipates only 1/10 of power than CML in 65 nm process [11].

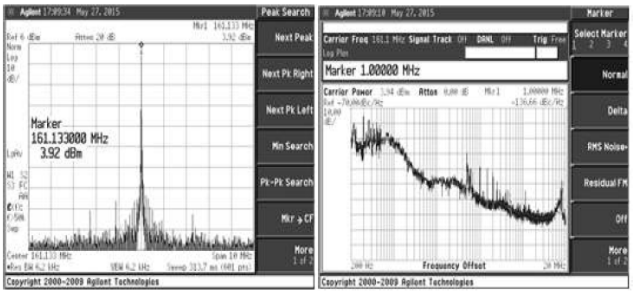

Fig. 21. Spectrum and phase noise of CDR

Fig. 22. Test board of the developed deserializer

III. MEASUREMENTS AND DISCUSSION

The developed 10.3125Gb/s deserializer for 10G-EPON is fabricated through 65nm CMOS process. The results of the designed deserializer are as follows: The deserializer occupies area of 1.96mm^2. The power consumption of the developed deserializer with CTLE is 380mW including I/O buffers. The input pattern provided by the PARBERT equipment and reference clock is applied to the developed deserializer. The extracted data patterns are compared with the input data patterns by using MATLAB codes. In order to evaluate the data patterns, the recovered clock that is able to be the standard to operate is first evaluated as shown in Fig. 21. As a result, the phase noise of the deserializer is -107dB/c at 1MHz offset. The developed deserializer is evaluated with 2^{31}-1 data pattern. The result of the evaluation is passed without the error. In the test boar as shown in Fig. 22, the developed deserializer is evaluated by using the optical module and IXIA. The output of the deserializer transmits to the external serializer. And then, the IXIA evaluates the transmitted data of the serializer. As a result, among the transmitted data 3,840,000 bytes, the 3,792,000 bytes is accepted. The accepted data rate is about 98.75%.

TABLE I
PERFORMANCE SUMMARY

Specification	16:1 Desrializer
Technology	65nm CMOS
Input data rate	10Gb/s
Reference clock	156.25MHz
Equalizer	CTLE / DFE
Supply voltage	1.2 V
Power consumption	200mW
Area	1.4mm X 1.4mm

IV. CONCLUSION

The deserializer for 10G-EPON standard is rendered through 65nm CMOS. The deserializer for 10G-EPON with CTLE and DFE is implemented. In order to evaluate deserializer, the PRBS 2^{31}-1 patterns were put in the designed deserializer by using the PARBERT. The deserializer is evaluated by MATLAB without error. Also, it is evaluated with optical modules and IXIA integrated the Ethernet data packet. As a result, it achieves the 98% of data reliability rate.

ACKNOWLEDGMENT

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Won june Hwang received the B.S. and M.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2011 and 2014, respectively. He currently is working toward the Ph. D. degree in electrical and electronics engineering. His research interests include PMIC (Power Management IC) with buck-boost DC-DC converter and PLL in zigbee system.

Yun Sik Choi received the B.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2017, where he is currently working toward the M.S. degree in electrical and electronics engineering. His research interests include high speed SerDes circuits and low-noise Phase-Locked Loop

Bo Yun Jung received the B.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2016, where she is currently working toward the M.S. degree in electrical and electronics engineering. Her research interests include high-speed digital-to-analog converter (DAC).

Kwang Hyun Baek (S’97–M’02–SM’10) received the B.S. and M.S. degrees from Korea University, Seoul, Korea, in 1990 and 1998, respectively. He received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC), IL, USA, in 2002. From 2000 to 2006, he was with the Department of High-Speed Mixed-Signal ICs as a senior scientist at Rockwell Scientific Company, formerly Rockwell Science Center (RSC), Thousand Oaks, CA, USA. At RSC, he was involved in development of high-speed data converters (ADC/DAC) and direct digital frequency synthesizers (DDFS). He was also with Samsung Electronics from 1990 to 1996. Since 2006 he has been with the School of Electrical and Electronics Engineering, Chung-Ang University (CAU), Seoul, Korea, where he is a faculty member. His research interests include high-performance analog and digital circuits such as low-power ADCs, high-speed DACs, hybrid frequency synthesizers (PLLs, DDFSs), high-speed interface circuits (CDRs, SerDes), PMIC, and near threshold-voltage (NTV) circuits.

A 1.2V 30 MS/s SAR ADC with Foreground Capacitor Calibration

Hyun Gyu Ju[1], Se Won Lee and Min Jae Lee[a]
School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology
E-mail: [1]hgju@gist.ac.kr

***Abstract* – In this paper, a successive approximation register (SAR) ADC with foreground capacitor calibration is presented. In order to overcome the drawback of SAR architecture with low-power consumption, several techniques are adopted such as high-speed latch, three-stage comparator, reference-less architecture, custom metal-oxide-metal (MOM) capacitor, and foreground capacitor calibration. The design methodology and measurement procedure is presented in detail. The prototype ADC is fabricated in a 65 nm CMOS process, and it achieves signal-to-noise and distortion ratio (SNDR) over 60 dB at sampling frequency of 30 MS/s under 1.2 V supply voltage. The power consumption is 1.1 mW, and the chip area of the core ADC is 0.045 mm^2.**

***Keywords*—Capacitor mismatch, foreground calibration, successive approximation register (SAR) ADC**

I. INTRODUCTION

Low-power techniques are an important factor to extend devices' battery life in the rapidly growing portable device market. Thus, a successive approximation register (SAR) ADC has been widely adopted in recent years due to its straightforward operation principle, with low power consumption compared to other architectures. However, it is difficult to improve sampling frequency, because of increased bit-decision cycles as the resolution of an ADC and limitation of DAC settling, which are determined by transistor turn-on resistance and capacitance. Therefore, a SAR ADC is commonly used in relatively low speed fields, such as bio-medical, sensor, EEG and EMG [1, 2].

As the semiconductor process progresses, the size of the MOS transistor has gradually reduced, which enables to raise the operating frequency of the SAR ADC to a higher frequency band. This is because of the resistance of the MOS transistor in the linear region being diminished, as technology scales down. The SAR ADCs enlarge the operating frequency band to several tens of MS/s, such as wireless section, and aims to reach several hundreds of MS/s using multi bit-per-cycle or any other techniques [3-5].

a. Corresponding author; minjae@gist.ac.kr

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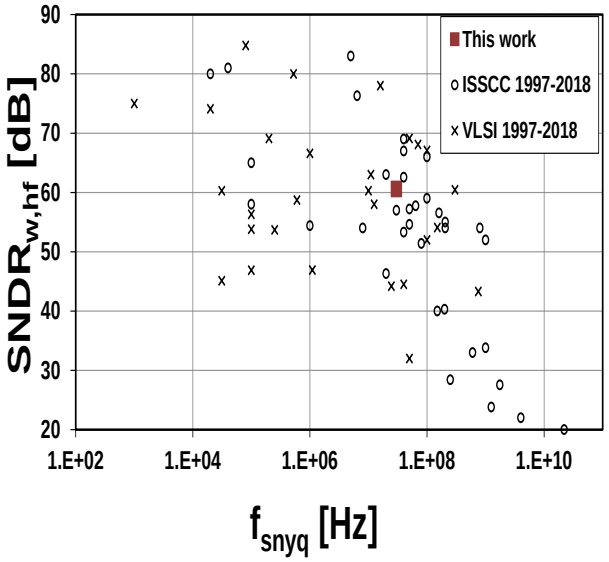


Fig. 1. A survey of SAR ADCs in terms of sampling frequency and SNDR

In contrast to the improvement in operating speed of SAR ADC, resolution performance such as SNDR has not been dramatically improved with the developing process. This is due to the fact that the reference level to convert the input signal depends on capacitor matching in SAR ADC. As the size of the metal is scaled down, the capacitor mismatch makes it difficult to guarantee high linearity.

Fig. 1 shows published SAR ADCs in terms of sampling speed and SNDR [6]. Based on the architectural disadvantages of SAR ADC, the SNDR performance and sampling frequency tend to be inversely proportional to each other. Nevertheless, methods to overcome these drawbacks have been intensively studied, as compared to other ADCs, owing to the low power architecture. Likewise, this paper describes a high-speed latch and three-stage comparator to increase the sampling frequency and introduces custom capacitor layout and capacitor mismatch calibration to improve SNDR performance. In addition, the overall design methodology is discussed.

This paper is organized as follows. The design of SAR ADC is described in section II. Section III shows the foreground capacitors mismatch calibration technique. The measurement and discussion are presented in section IV. Finally, the conclusion is drawn in section V.

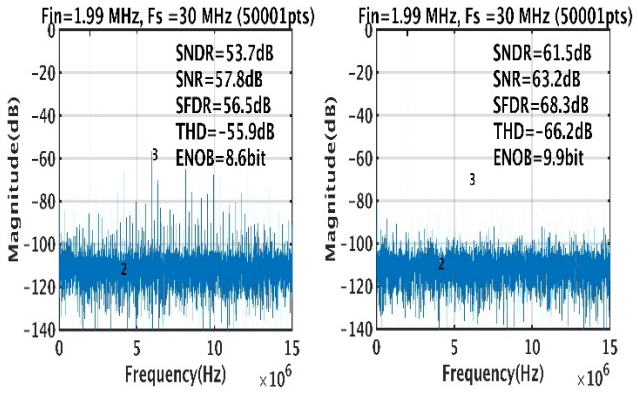
II. DESIGN METHODOLOGY OF SAR ADC

A. Modeling of SAR ADC

The modeling of the SAR ADC was performed using the MATLAB tool to determine the various design parameters such as total sampling capacitor, noise contribution for each ADC blocks, consideration of redundancy capacitors and so on.

```
------------------------------------------------------------------
---------------------- SAR CAPDAC ------------------------------
------------------------------------------------------------------
------------------------------------------------------------------
order     ideal_CW       CDAC_vip (fF)      CDAC_vin (fF)
------------------------------------------------------------------
 1(dum)      1             0.404934           0.390162
 2           1             0.468483           0.327797
 3           2             0.764891           0.818590
 4           4             1.605176           1.778557
 5           8             3.428516           3.112384
 6           8             3.265917           2.919589
 7          16             6.281568           6.273926
 8          32            12.538605          12.955526
 9          64            25.218985          26.078855
 10        128            51.016508          51.547936
 11        128            50.523988          52.636548
 12        256           102.254667         103.489483
 13        512           205.302992         204.240355
 14       1024           408.286525         406.992378
------------------------------------------------------------------
 Total                    871.3618           873.5621
 Cp                       440.0000           440.0000
------------------------------------------------------------------
 Cs                       1311.3618          1313.5621
------------------------------------------------------------------
------------------------------------------------------------------
---------------------- SAR Parameters --------------------------
------------------------------------------------------------------
Input signal swing (Diff pp) = 1.60 ( Vref = 1.2 )
------------------------------------------------------------------
1LSB step (Resolution)   = 194.7516 (uV)
------------------------------------------------------------------
Quantization Noise          = 56.22 (uV)
Comp Noise(Diff)            = 180.00 (uV)
KT/Cs Noise(Diff)           = 39.71 (uV)
Reference Noise(Diff)       = 75.32 (uV)
Amp Noise(Diff)             = 50.00 (uV)
------------------------------------------------------------------
```

(a)



(b) (c)

Fig. 2. Modeling of SAR ADC; (a) parameters (b) output spectrum before capacitor calibration (c) output spectrum after capacitor calibration for upper 4 MSB capacitors

Fig. 2 (a) shows the modeling results of the designed SAR ADC. It has 12-bit resolution and a total of 14 conversion cycles with two redundancy cycles. The total sampling capacitor is 1.3 pF to consider KT/C noise, and the unit size of custom capacitor is determined as 0.4 fF considering a practical layout. Our target performance of the SAR ADC shown is over 60 dB of signal-to-noise and distortion ratio (SNDR) after capacitor mismatch calibration. Before the capacitor mismatch calibration, the SNDR of the SAR ADC achieves about 54 dB due to the effect of capacitor mismatch as shown in Fig. 2 (b). After capacitor mismatch calibration for upper 4 MSB capacitors, the SNDR of SAR ADC is improved to 61 dB as shown in Fig. 2 (c). The amount of noise is set to have a smaller effect than capacitor mismatch. The detailed foreground capacitor mismatch calibration method is discussed in section III.

B. Bootstrap

In the designed SAR ADC, top-plate sampling is used to reduce the MSB sampling capacitor. Therefore, channel charge injection from a sampling MOS transistor is a major factor in performance degradation for ADC with high linearity. In order to alleviate channel charge injection, Fig. 3 shows the bootstrap circuit which keeps the gate-source voltage of the MOS transistor constant for any input level. When the clock is low, the sampling transistor is turned off and the capacitor is charged to VDD. When the clock is high, one side of the capacitor is connected to the input and the other side is connected to the gate of the sampling MOS transistor. As a result, the gate-source voltage is continuously kept at VDD by the capacitor. The body of the PMOS that controls the boosted voltage is connected to the boosted voltage side, not to VDD, because the boosted voltage is always greater than VDD. In our bootstrap circuits, a triple well MOS transistor is used to disconnect from supply noise caused mainly by the digital circuit.

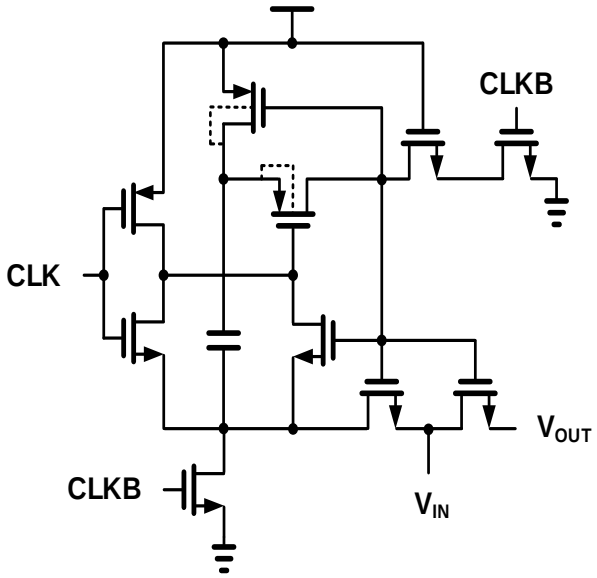


Fig. 3. The schematic of a bootstrap circuit to reduce channel charge injection of sampling switch

C. Comparator

Fig. 4 represents the dynamic comparator circuit of the designed SAR ADC [7]. In order to achieve a large gain at low supply voltage, we chose a three-stage architecture with 3-stacked transistors. The detailed operation method is as follows. When the clock is low, the first stage output of comparator is reset to VDD by M4 and M5. The final output stage is also reset to VDD by the reset switch M16, M17, M18 and M19. When the clock is high, the first output node rises to VDD with the time difference as the input levels. The second stage class-AB amplifiers amplify the each first outputs. Then, the cross-coupled inverters in the third stage quickly regenerate comparator outputs using positive feedback. In the designed comparator, the switch size should be determined appropriately, because the small size of the reset switch causes dynamic offset of the comparator, and the excessive size of reset switch causes the parasitic capacitor to slow down regeneration and consume more power. The regeneration core consists of M10-M13 should be small in size to achieve fast regeneration time. Moreover, input transistors M1 and M2 are large enough to reduce input referred noise and comparator static and dynamic offset from transistor mismatch. The detailed transistor sizes of comparator are summarized in Table I. From the modeling, the noise amount of comparator is set to about 180 μV_{rms}. Due to the limitation of increasing size of the input transistors, MOS capacitors are added on the first stage output to lower the noise level.

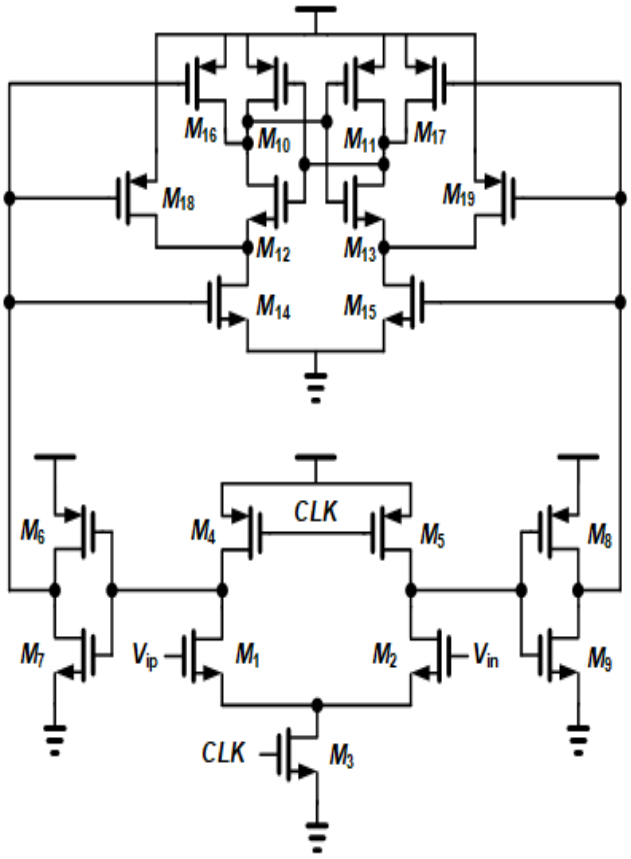


Fig. 4. Schematic of three-stage dynamic comparator

TABLE I
Transistor Parameters of Comparator

Transistor	Transistor Size W/L [um/um]
M1,M2	43.2/0.065
M3	6.48/0.065
M4, M5	8.64/0.065
M6, M8	7.28/0.065
M7, M9	4.32/0.065
M10, M11	1.44/0.065
M12, M13	0.72/0.065
M14, M15	1.44/0.065
M16, M17	0.72/0.065
M18, M19	1.44/0.065

D. Reference-less architecture

A reference buffer is used in many ADCs to provide a small output impedance for fast reference voltage settling. However, the reference buffer consumes static current to generate small output impedance and may even consume more power than the SAR ADC. In our design, we did not use the reference buffer for low power operation. As a penalty for this, the sampling frequency of SAR ADC is limited to reference voltage settling. Originally, the sampling frequency is possibly up to 40 MS/s except for reference voltage settling.

E. SAR Logic

Conventional digital logic of a SAR ADC consists of two flip-flop arrays. The first array provides a conversion sequence and consists of a shift register. Thus, the information of the current cycle is sequentially shifted every time when comparator is operated, and the size of shift register is determined by the total conversion cycles. The second flip-flop array is to catch and hold a comparator output. From the first flip-flop array conversion sequence, the comparator outputs are stored in each flip-flop in the second array and drive capacitor DAC to generate the next reference level. This logic configuration is very simple and can be implemented with low-power. However, the propagation delay of clock to output delay of flip-flop is the largest bottleneck in the SAR ADC to achieving high speed operation. Therefore, a custom SAR logic is adopted to catch data rapidly as shown Fig. 5 [8]. From the first flip-flop array, the enable signal (EN) is to be sequentially high. When EN is high, the data input D_{IN} is passed through transmission gates. Then, the logical data is propagated through three inverters. When the current conversion cycle ends, the enable signal is low. The input transmission gate separates stored conversion data from comparator output $D_{IN,}$ and the transmission gate in the output buffer activates the internal

latch. Lastly, the SAR logic is reset when SAR conversions are completed, the NMOS reset switch forces the input of output buffer to be low, and PMOS reset switch sets floating node to high level.

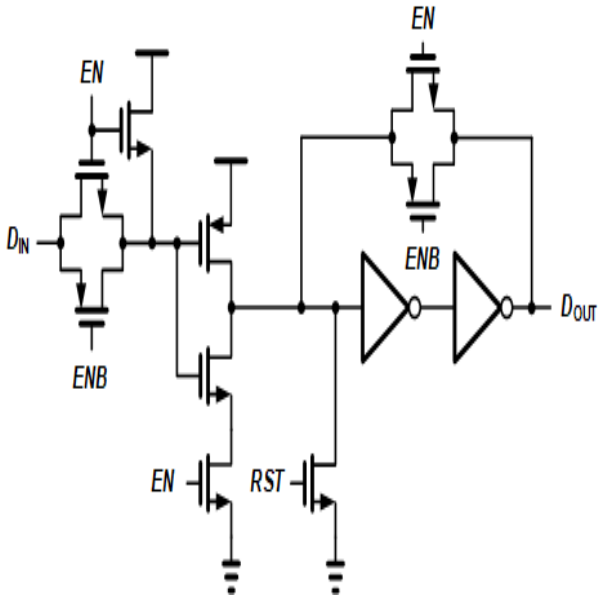


Fig. 5. Schematic of high speed data latch

Fig. 6 shows the custom MOM capacitor layout. Metal 5 and 6 layer are used to reduce parasitic capacitor from substrate. The unit capacitance of CDAC is 0.4 fF and unit capacitance for mismatch calibration is 0.125 fF, which is 4 times smaller than unit capacitance of CDAC for fine tuning.

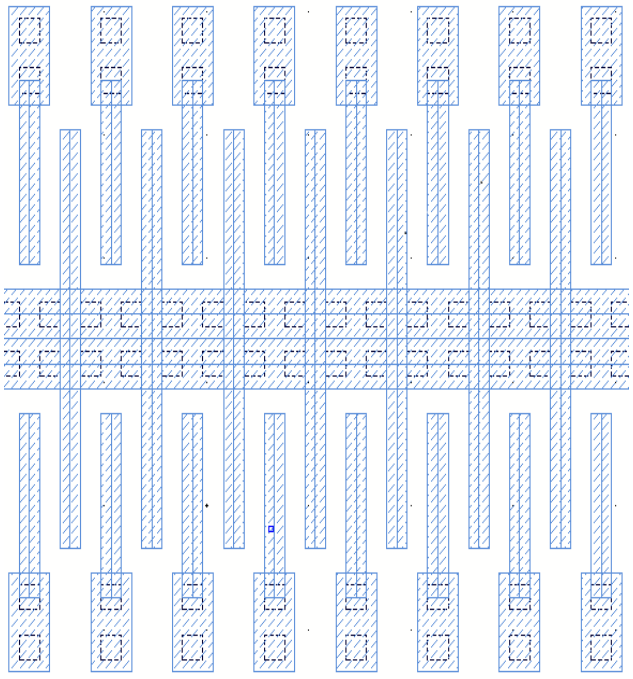


Fig. 6. Custom capacitor layout using stacked metal 5 and 6

III. FOREGROUND CAPACITOR MISMATCH CALIBRATION

As CMOS devices become smaller due to process evolution, the SAR ADC has the advantage of operation speed and low power implementation. However, the capacitor mismatch, which determines the linearity of SAR ADC, is becoming worse. For most SAR ADCs with high resolution, the minimum capacitor value is limited by capacitor matching rather than KT/C noise. Likewise, in this design, the small unit capacitor is used for fast operation speed, and the capacitor matching issue is resolved through calibration. Among two calibration methods, called foreground and background calibration, we adopt the former because the error from capacitor mismatch appears deterministically. We calibrate the top four capacitors with the largest matching error among the 14 capacitors including the two redundancy capacitors.

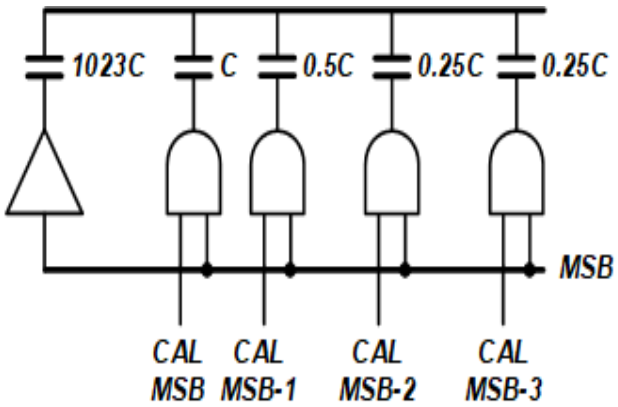
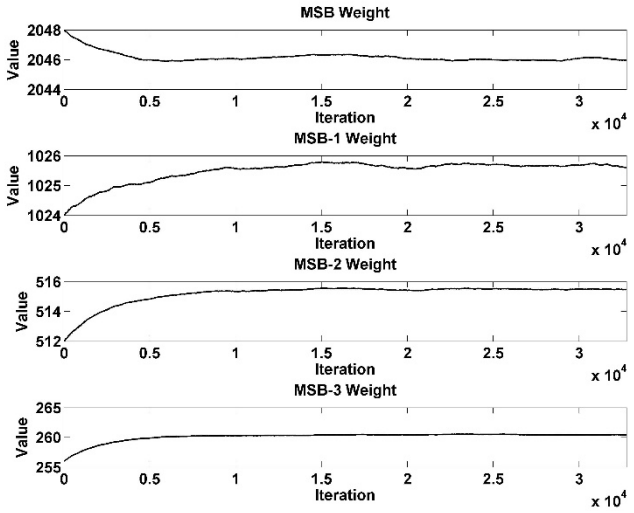


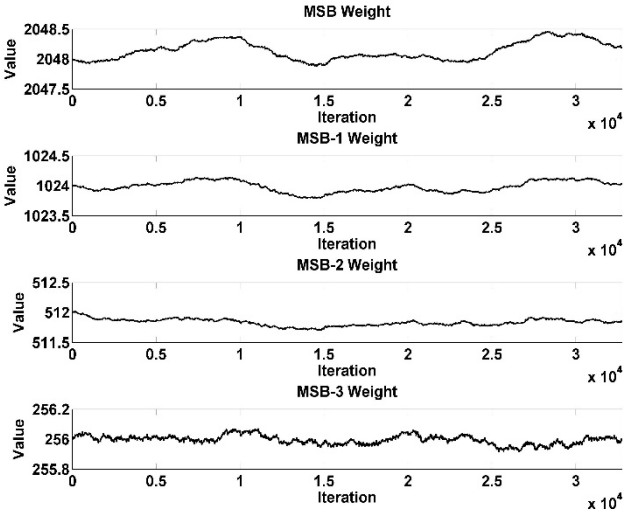
Fig. 7. Custom capacitor layout using stacked metal 5 and 6

Fig. 7 shows the MSB capacitor with mismatch calibration capacitors. Originally, the MSB capacitor is composed of a total of 1024C. The MSB capacitor is reduced to 1023C and total size of 2 unit capacitor with 1/4 of resolution is used to adjust the size of the MSB capacitor. The NAND gates drive each calibration capacitors, and calibration data codes CAL MSB from decoder determine the mismatch capacitor activation.

In the foreground calibration, the loot-mean-square (LMS) algorithm is used to obtain the error information. Fig. 8 (a) shows the calculation of the weights with the lowest error using the LMS for the weight of upper 4 MSB. Although we use approximately 215 measured output samples, it can be seen that the LMS algorithm can be utilized with approximately 10,000 output samples. Before calibration, four MSB weights with minimum error deviate from the binary weight due to capacitor mismatch. This error information is the source for adjusting the capacitor. For example, as the MSB-3 capacitor requires about 260 weight, the MSB-3 capacitor should be increased. Thereby, the capacitor mismatch calibration is performed in sequence from the lower capacitor to upper capacitor. After calibration, the capacitors are calibrated to achieve minimum error and hence, obtaining binary weight as shown in Fig. 8 (b).

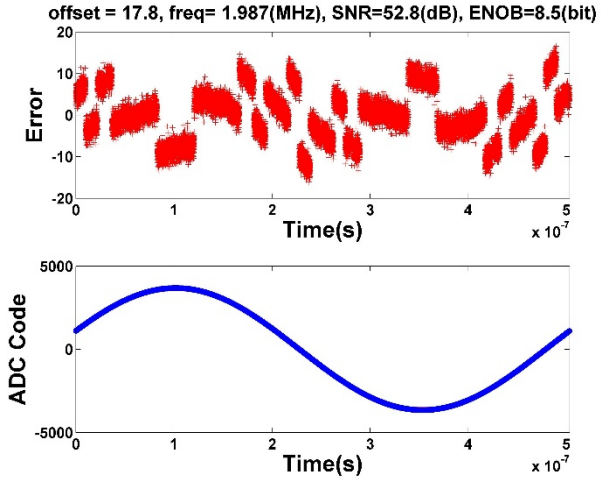


(a)

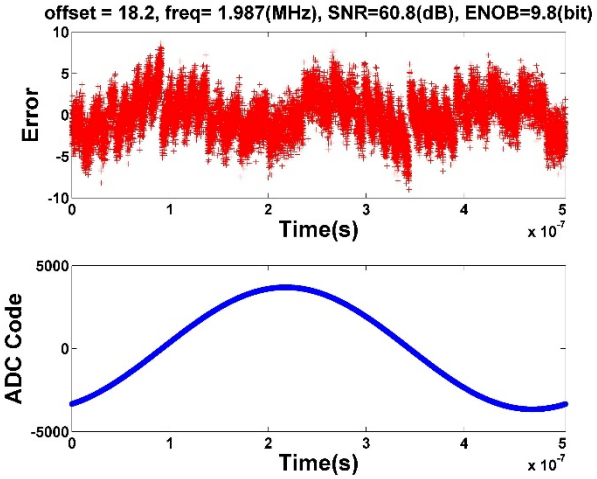


(b)

Fig. 8. The required weights for the 4 MSB through LMS algorithm; (a) before calibration (b) after calibration



(a)



(b)

Fig. 9. Sine wave curve fitting of measured outputs; (a) before capacitor mismatch calibration (b) after capacitor mismatch calibration

IV. RESULTS AND DISCUSSIONS

The prototype ADC is fabricated in 65 nm CMOS process with a sampling frequency of 30MS/s consuming 1.1 mW under 1.2 V supply. Fig. 11 shows the measurement board of prototype SAR ADC. Digital IO and LDO is implemented by using switches and external chips. In addition, the SPI controller, logic analyzer, and signal generator for testing ADC utilize instruments. Fig. 12 shows die photograph of the prototype ADC. The core ADC occupies 150-um height and 300-um width. Fig. 13 shows the measured output spectrum of prototype ADC. With 1.9 MHz input frequency, a measured spurious free dynamic range (SFDR) and SNDR are 66.1 dB and 60.8 dB, respectively. With near Nyquist frequency, the prototype ADC achieves SFDR of 75.2 dB and SNDR of 60.6 dB. The calculated figure of merit (FoM) is 41 fJ/conv.-step. Fig. 13 shows the DNL and INL to show the static performance. The measured minimum and maximum DNL are -1 LSB and 4.6 LSB, respectively, and measured minimum and maximum INL are -6.2 LSB and 5.6 LSB, respectively, owing to a capacitor calibration. The overall performance of the prototype ADC is summarized in Table II and compare to [5, 9, 10].

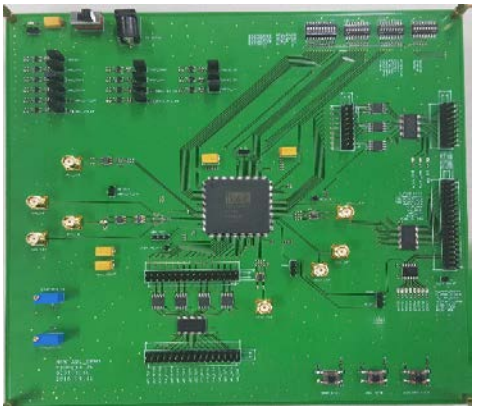


Fig. 11. Test Board to measure prototype SAR ADC

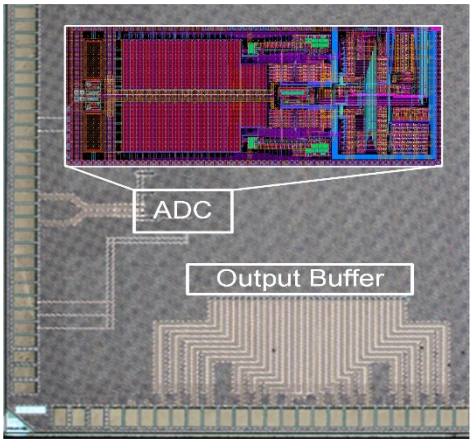
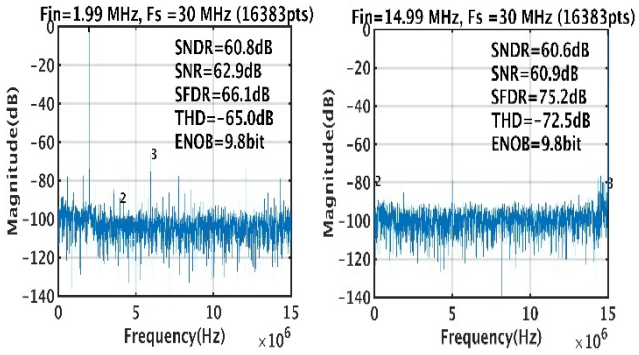
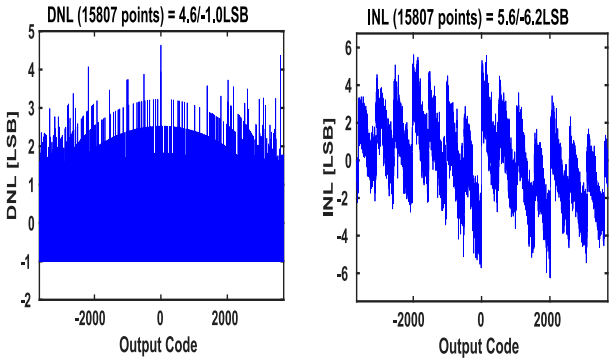


Fig. 12. Die photograph



(a) (b)

Fig. 13. Measured output spectrum at; (a) 1.9 MHz input (b) 14.9 MHz input



(a) (b)

Fig. 14. Static performance of the prototype ADC; (a) DNL (b) INL

TABLE II
Performance Summary and Comparison

	[5]	[9]	[10]	This work
Technology (nm)	130	130	90	65
Resolution (bit)	10	12	9	12
Sampling Rate (MS/s)	50	45	40	30
Supply Voltage (V)	1.2	1.2	1	1.2
Area (mm^2)	0.052	0.059	0.09	0.045
ENOB (bit)	9.2	10.8	8.2	9.8
Power (mW)	0.826	3.02	0.82	1.1
FoM (fJ/conv.-step)	29	36.3	54	41.1

V. CONCLUSION

A design methodology for high speed and linear SAR ADC with low power consumption is presented. The design considerations are introduced in the order of modeling of SAR ADC, bootstrap, three stage comparator, reference-less architecture, SAR logic and custom capacitor. In addition, the foreground capacitor calibration method is described to resolve the matching issue of reduced total sampling capacitor due to the high speed implementation. Thanks to the capacitor mismatch calibration, the prototype ADC achieves over SNDR of 60 dB under 30 MS/s sampling frequency with 1.1 mW power consumption, yielding 41.1 fJ/conversion-step.

ACKNOWLEDGMENT

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Hyun Gyu Ju received the B.S. degree in control and measurement engineering from Hanbat National University, Daejeon, South Korea, in 2013, and the M.S. degree from School of Electrical Engineering and Computer Science from Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2015, where he is currently working toward the Ph.D. degree at GIST. His research interests include high speed data converter and mixed-signal integrated circuits.

Se Won Lee was born in Busan, Korea, in 1991. He received his B.S. degree in Electronics Engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2017. He is currently working toward Ph.D. degree in School of Electrical Engineering and Computer Science from Gwangju Institute of Science and Technology, Gwangju, Korea. His research interests include mixed signal IC design, especially, high speed A/D converters.

Min Jae Lee received the B.S. and M.S. degrees from Seoul University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2008, all in electrical engineering.

In 2000, he was a Consultant with GCT Semiconductor Inc., and Silicon Image Inc., Sunnyvale, CA, USA, designing analog circuits for wireless communications and digital signal processing blocks for gigabit Ethernet. He joined Silicon Image Inc., in 2001, developing Serial ATA products. In 2008, he joined Agilent Technologies, Santa Clara, CA, USA, where he was involved in the development of next-generation high-speed ADCs and DACs. Since 2012, he has been with the School of Electrical Engineering and Computer Science, Gwangju, South Korea, where he is currently an Associate Professor.

Dr. Lee was a recipient of the 2007 Best Student Paper Award at the VLSI Circuits Symposium in Kyoto, Japan. He received the 2015 Distinguished Lecture Award from the Gwangju Institute of Science and Technology.

A low noise Hall Effect Sensor Readout Circuit

Yu Seong Kim[1] and Seong Ik Cho[a]
Department of Electrical Engineering, Chonbuk National University
E-mail: [1]yoosung5514@jbnu.ac.kr

***Abstract* – In this paper, the structure, operation principles, and characteristics of the hall sensor using semiconductors are discussed through the hall sensor design. The CMOS hall sensor is composed of a CMOS hall plate and Readout Integrated Circuit (ROIC) which processes the signal of the hall plate. For this sensor, a detailed ROIC design is required due to the small output signal of the hall plate. The ROIC consists of the part related to current spinning with chopping and Instrumentation Amplifier (IA). In this circuit, the offset and 1/f noise of the magnetic signal are separated by the current spinning frequency of 100 kHz and the noise of amplifier is removed by chopping. The IA has high input impedance, low offset and large Common Mode Rejection Ratio (CMRR). Also, the de-chopping is placed inside the IA which can be designed with op amp that has low slew rate and narrow bandwidth. The designed ROIC has the difference 43dB gain between noise gain and signal gain. The signal gain is 64dB. The proposed hall sensor operates as a switch at 0~20mT magnetic field in 10 kHz with 1mA bias current. It has been integrated in a standard 0.18um CMOS technology.**

***Keywords*—Hall effect sensor, Magnetic sensor, ROIC**

I. INTRODUCTION

The interest in magnetic sensors has significantly increased in recent years because of its attractive and applicable advantages in various ways. The magnetic sensor that converts magnetic field into electrical signal is widely used in various fields. Magnetic sensors are frequently applied not only for automotive industry and compass applications but also in a large variety of biomedical systems. The Hall Effect is a typical phenomenon that is occurred in magnetic sensors. Hall Effect magnetic sensor is the base of highly developed and important industrial activities. It is commonly used as a key element in contact-less sensors for linear position, angular position, velocity, rotation, electrical current, and so on [1]. The basic principle of the Hall Effect is shown in Fig. 1.

When the magnetic field is placed perpendicular to the conductor where a current is passed, the voltage is generated, perpendicular to both the current and the magnetic field. This effect is known as Hall effect, and the generated voltage is called Hall voltage. Therefore, the hall voltage of a hall plate may be regarded as a signal carrying information. If we know the material properties, device geometry and biasing conditions, the hall voltage can give us information about the magnetic induction B [2]. The Hall plate that senses magnetic field is produced by bipolar or CMOS process [3]. The CMOS Hall plate is small size and low cost but it has low sensitivity and offset on process variation. Therefore, effective hall plate and low noise readout circuit are required [4]. The cross shape of hall plate effectively reduces offset of hall plate, and the combination of chopping and current spinning technique can reduce offset and 1/f noise [5]. Generally, hall effect sensors are composed of the hall plate to generate hall voltage and ROIC [6]. The integrated hall sensor block diagram is shown in the Fig. 2.

In this paper, a hall sensor is designed to have readout circuit applying current spinning and chopping technique. In the section A and B of chapter II, the cross shape hall plate structure with high sensitivity is described and the hall plate equivalent circuit for signal processing circuit design is modeled. In section C, the signal processing circuit is designed with the proposed hall plate and the principles of the combination of chopping and current spinning technique for low noise, as well as IA designs are illustrated. Since the operation error occurs in the ROIC due to the bandwidth limitation of the IA, the designed model has a de-chopping

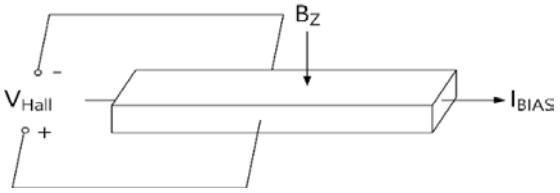

Fig. 1. The basic principle of the Hall Effect

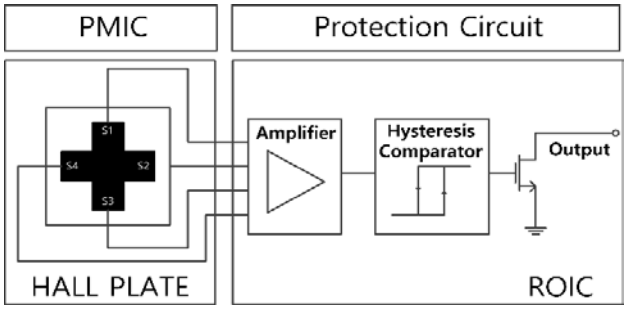

Fig. 2. The integrated Hall sensor block diagram

a. Corresponding Author; sicho@jbnu.ac.kr

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structure in the middle of the measurement amplifier to solve this error. The simulation of the designed Hall sensor is presented in Section D. Related results and discussion of the manufactured Hall sensor test are shown in Chapter III. Finally, the conclusion is drawn in chapter IV.

II. MAIN SUBJECT

A. Hall plates

Hall sensor has two different modes and it is called 'Current mode' when current is outputted and 'Voltage mode' when voltage is outputted. In voltage mode, current or voltage can be received by the bias input. These are referred to as 'Current-related voltage mode' and 'Voltage-related voltage mode', respectively. One of the most important characteristic is magnetic sensitivity and the equations to calculate absolute sensitivity S_A for each mode are shown as eq. (1-a) and eq. (1-b).

$$\text{Voltage-related } S_A = \frac{V_{Hall}}{B} \text{ [V/T]} \tag{1-a}$$

$$\text{Current-related } S_A = \frac{I_{Hall}}{B} \text{ [A/T]} \tag{1-b}$$

V_{Hall} and I_{Hall} mean Hall voltage and Hall current respectively. Relative magnetic sensitivity depending on the operating mode of the sensor is shown in TABLE I [7].

TABLE I
Sensitivity of Hall magnetic sensors in voltage-mode and current-mode condition

Mode	Sensitivity	Unit
Current-Biased Voltage-Mode	$S_A = \frac{S_{Hall}}{I_{bias} \times B}$	[V/AT]
Voltage-Biased Voltage-Mode	$S_A = \frac{S_{Hall}}{V_{bias} \times B}$	[V/VT= T]
Current-Mode	$S_A = \frac{I_{Hall}}{I_{bias} \times B}$	[A/AT=T]

Hall plates are classified into three types according to the shape of the sample. First type is when its length L is infinite, second type is when it is a rectangle, and the third is the cross shape device. Three types of hall plates are shown in Fig. 3.

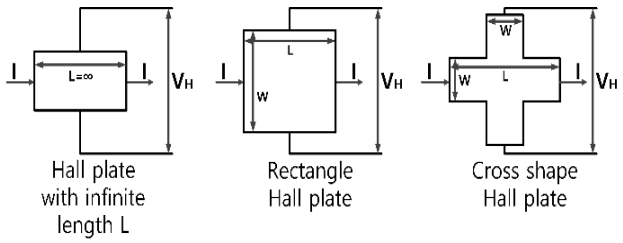

Fig. 3. Types of hall plates

In the case of a Hall plate with infinite length L, the Hall voltage is eq. (2).

$$V_{Hall} = \frac{1}{qnt} I_{Bias} B \tag{2}$$

Where q denotes the magnitude of the electron charge, n is the carrier concentration in the plate and t is the plate thickness. However, the Hall voltage of rectangle Hall plate and cross shape Hall plate is eq. (3).

$$V_{Hall} = \frac{G}{qnt} I_{Bias} B \tag{3}$$

G denotes the geometrical correction factor of Hall voltage. For an ideal Hall sensor with a very long rectangular shape, G=1. In case of the cross shape Hall plate, G can be formulated as eq. (4) and the value of G is less than 1(G<1) meaning that Hall voltage is smaller than the ideal case.

$$G = 1 - 5.0267 \frac{\theta_H}{\tan(\theta_H)} e^{-\frac{\pi W + 2L}{2\ W}} \tag{4}$$

The cross shaped Hall plate is a geometry with low offset noise and high sensitivity [8]. CMOS Hall plate is composed of N-well active region, P+ layer and N+ contacts. P+ layer covers the surface of active area to decrease the flicker noise and N+ contacts use to reduce contact resistances. The cross shaped Hall plate cross section is shown in Fig. 4.

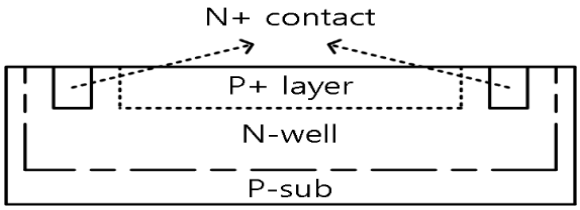

Fig. 4. The cross shaped Hall plate cross section

The cross shaped Hall plate has been modeled in using the Verilog-A language as shown in Fig. 5. in order to easily simulate [7].

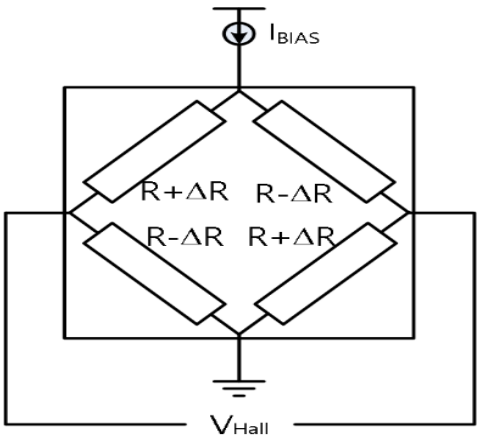

Fig. 5. Bridge circuit model of Hall plate using Verilog-A

B. Hall plate optimal size tracking

G in eq. (4) is proportional to length and inversely proportional to width. The longer the length, the more Hall plate is identical to the ideal shape of very long rectangle. So, this equation (G) converge to 1 and it is shown as a graph in Fig. 6.

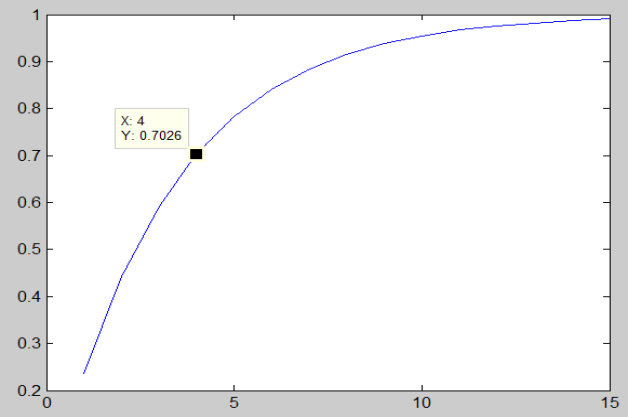

Fig. 6. Geometry correction factor according to length

The relation between the voltage related voltage mode and the current related voltage mode is formulated in eq. (5) [9].

$$S_V = \frac{S_I}{R_S N_S} \cong \frac{G}{2\frac{L}{W}+\frac{2}{3}}\mu_H \quad (5)$$

This equation is shown as a graph in Fig. 7.

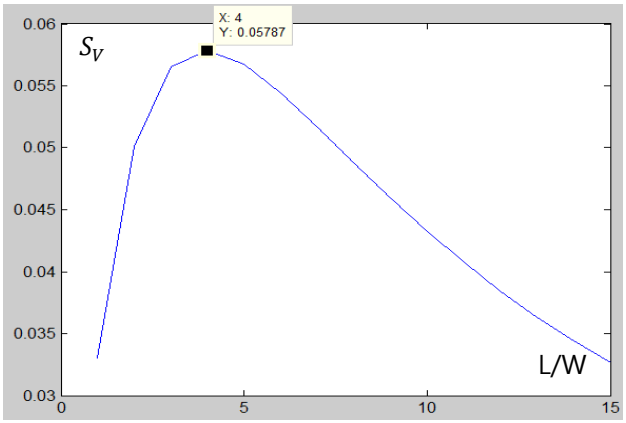

Fig. 7. Voltage related efficiency per width over length ratio of the sensor's arms.

As shown in Fig. 7., when the ratio of L/W is 0.4, the value of the sensitivity reaches its maximum. Therefore, the cross shape Hall plate width and length are designed as 10um and 4um respectively. Sheet resistance is shown in eq. (6). This value is given in the process and is 940 ohms.

$$R_S = \frac{1}{q\mu N t} \quad (6)$$

C. Readout circuit

According to materials, the electron mobility varies, and silicon's electron mobility is relatively low. It leads to low sensitivity of Hall plate and low output signal of Hall plate. In addition, due to the asymmetry of the process variables, offset and 1/f noise occur in the output signal. Therefore, noise must be suppressed. The combination of chopping and current spinning technique allows to dramatically reduce noises of Hall plate. The detailed noise reduction principle using chopping and current spinning technique is visualized in Fig. 8.

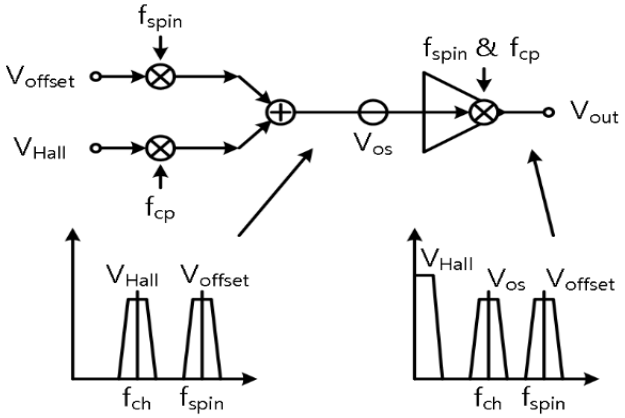

Fig. 8. The noise reduction principle using chopping and current spinning technique

The magnetic signal and the noise of Hall plate are divided by current switching frequency. The magnetic signal is moved to the chopping frequency and the noise is moved to the DC frequency band. The magnetic signal and the noise are divided through that the magnetic signal is moved to the DC frequency band by the de-chopping.

The Hall plate is a resistive sensor which has high output impedance. The resistive sensor also requires fully different amplifiers due to its different output. More specifically, low noise amplifier is needed because the output signal of the Hall plate is very low and has unnecessary noise. Using the fully differential amplifier as close loop is not suitable to amplify the plate signal because the input impedance is low. Therefore, instrumentation amplifier is chosen to amplify signal of Hall plate because it has high input impedance, low offset and large CMRR. However, since IA does not have wide bandwidth, putting de-chopping after normal IA is problematic due to the amplified swing range of the input signal. The amplified swing range of the input signal appears as chopping ripple. The principle of chopping ripple is shown in Fig. 9 [10].

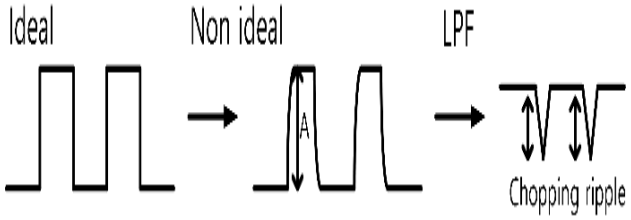

Fig. 9. The principle of chopping ripple

The amplified signal signifies that the amount of change dV of the signal becomes large. When amplifying dV is increased by the gain of instrumentation amplifier. So, the more current needs by eq. (7).

$$C\frac{dV}{dt} = I \tag{7}$$

Thus, chopping of the amplified signal has large chopping ripple. High slew rate and wide bandwidth are required to reduce the chopping ripple. The designed Hall sensor has de-chopping inside the IA. It decreases the necessary slew rate and bandwidth to reduce the chopping ripple than conventional IA. The structure of De-chopping is illustrated in Fig. 10.

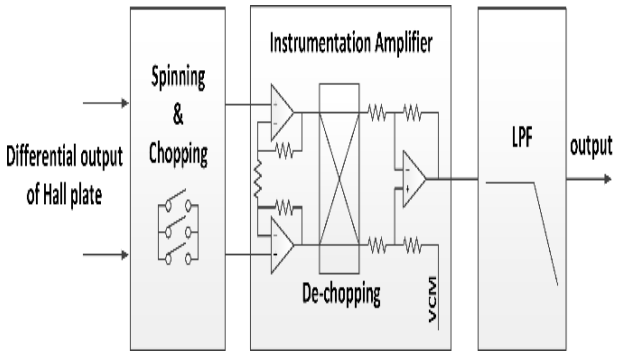

Fig. 10. De-chopping inside the instrumentation amplifier

In this circuit, the offset and 1/f noise of the magnetic signal are separated by the current spinning frequency of 100kHz and the noise of amplifier is removed by chopping of 200kHz.

D. Simulation

Fig. 11. illustrates the top block diagram of designed Hall sensor. The hall sensor is composed of the Hall plate, ROIC and PMIC. The designed Hall sensor uses LDO for stable supply voltage. The clock pulse for chopping and switching operation is supplied using the clock generation. The 400kHz frequency generated from the clock is divided for the current spinning frequency of 100kHz.
The magnetic field of 0~20mT is supplied at 10kHz for simulation. Fig. 12. shows the output of the Hall plate behind the current spinning and chopping. This means that the magnetic signals and the noise are separated. However, it has small signal that exist in large noise.

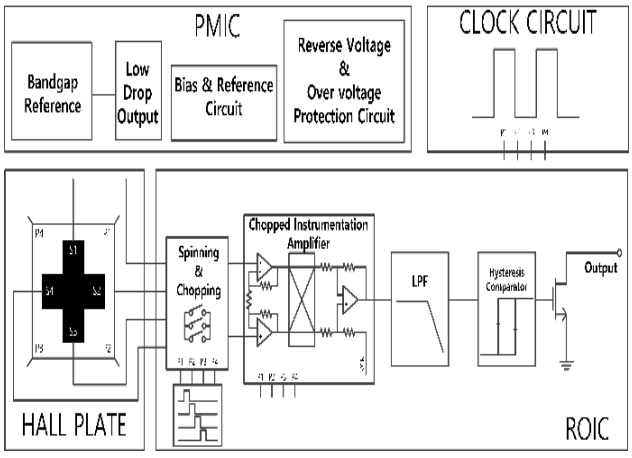

Fig. 11. The top block diagram of the designed Hall sensor

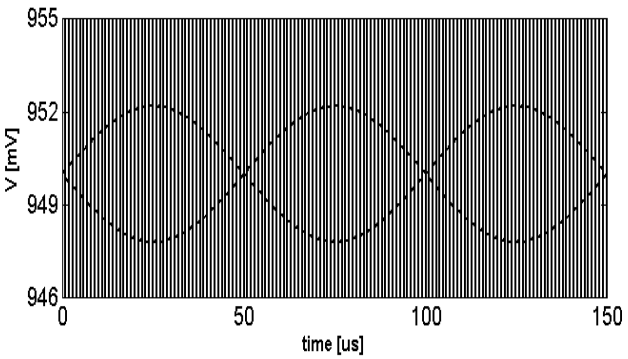

Fig. 12. The output of the Hall plate behind the current spinning and chopping

This output is amplified and demodulated through the proposed IA. The LPF filter is used for reduces chopping ripple behind the amplify stage. Fig. 13. shows the gain and bandwidth of the ROIC that have 64dB and 61kHz respectively. Reduced noise could be verified by the result that difference between the noise gain and signal gain is 43dB. It is shown in Fig. 14.

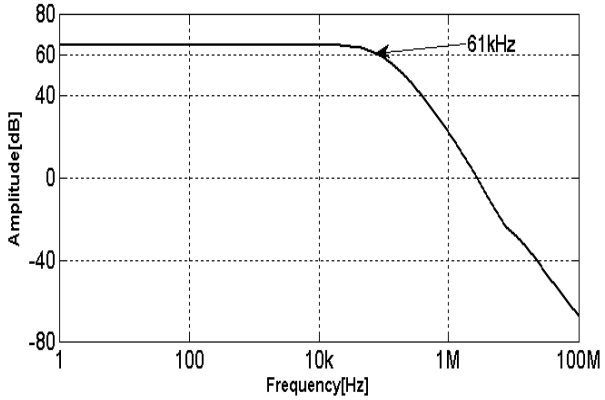

Fig. 13. The gain and bandwidth of the ROIC

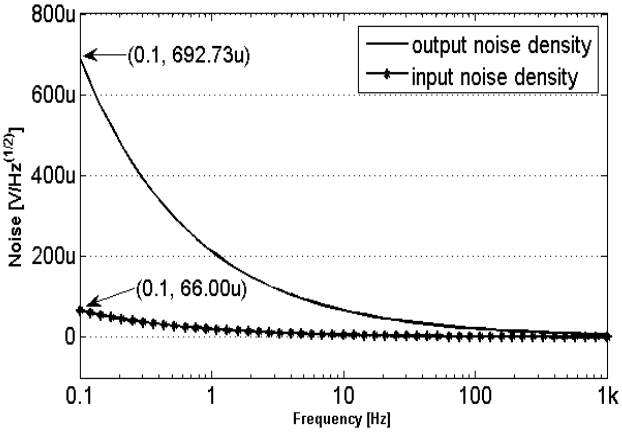

Fig. 14. Difference between the noise gain and signal gain

The comparator is used to switch signal after LPF filter. The output behind the comparator is shown in Fig. 15. It shows switch operation based on magnetic signal.

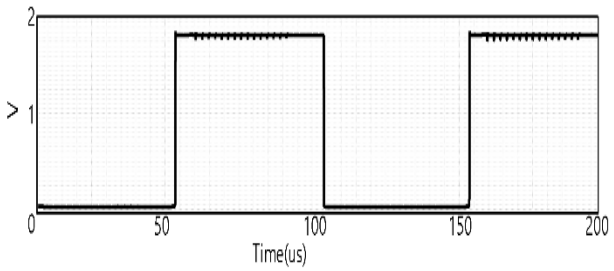

Fig. 15. The switch operation based on magnetic signal

III. RESULTS AND DISCUSSION

The test conditions are shown in TABLE II. The supply voltage is 3.3V and CM voltage is 0.9V. The current spinning frequency is 100kHz and the clock frequency for chopping is 200kHz. 1mA current applied to the sensor, and the magnetic field is applied through the 10Hz rotational motion of Neodymium magnet with 200mT. The experimental environment is configured as shown in Fig. 18. Supply voltage and CM voltage are applied using power supply. The output is measured using an oscilloscope.

TABLE II
The test conditions

Specification	Value
Process [um]	0.18
Supply voltage [V]	3.3
CM voltage [V]	0.9
Current spinning frequency [Hz]	100
Clock frequency [Hz]	200
Bias current [mA]	1
Magnetic field frequency [Hz]	10

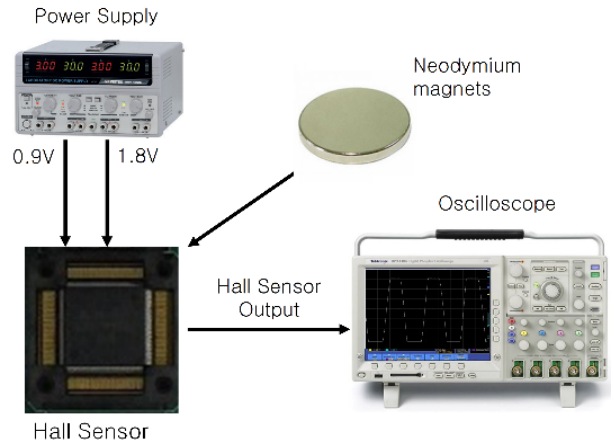

Fig. 18. Environment of the Hall sensor test

Fig. 19 shows the Hall sensor output in response to a magnetic field. It can be confirmed that the output is outputted according to the distance of the magnetic field based on the CM voltage of 0.9V. This output signal can be used to output a switching signal as shown in Fig. 20. using a comparator.

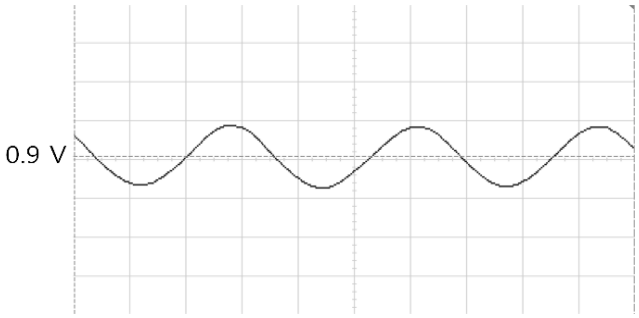

Fig. 19. Output of the Hall sensor

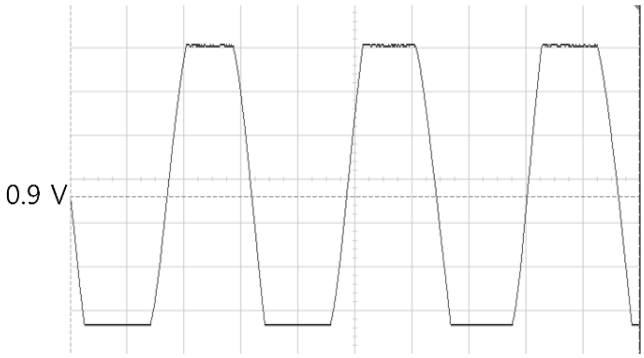

Fig. 20. Hall sensor as switch

IV. CONCLUSIONS

In this paper, the low noise ROIC for CMOS Hall sensor is designed. The CMOS Hall plate has been modeled using the Verilog-A language for simulation. The IA is used to amplify the modeled signal. Current spinning with chopping technique is used for low noise. When de-chopping is performed at the last amplifying stage, there is a problem that the chopping noise is increased by amplified swing range as gain of last amplifier. To solve that, the designed Hall sensor in this paper has de-chopping inside the IA, The required slew rate and bandwidth of the op amp are decreased to reduce the chopping ripple. The designed Hall sensor has 100kHz switching frequency. It operates as a switch at 0~20mT magnetic field in 10Hz with 1mA bias current. The difference between the noise gain and signal gain is 43dB. Further research about the offset reduction of the last amplifier in the proposed ROIC needs to be conducted.

ACKNOWLEDGMENT

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Yuseng Kim received the B.S. degree in major of semiconductor science & technology from Chonbuk University, Jeonju, Korea, in 2017. His research interest includes low voltage analog semiconductor integrated circuit design.

Seong Ik Cho received the Ph. D degree in electrical engineering from Chonbuk University, Jeonju, Korea, in 1994. His main interest is low voltage analog semiconductor integrated circuit design.

A Low Phase Noise Integer-N Frequency Synthesizer for 2.4GHz ZigBee Application

Sung Wook Yoon[1], Chang Yeol Kim, Yang Ji Jeon and Il Ku Nam[a]
Department of Electrical Engineering, Pusan National University
E-mail: [1]tjddnr1100@naver.com

Abstract **- A low phase noise and low power consumption integer-N frequency synthesizer for ZigBee application (IEEE 802.15.4) in the frequency range of 2.39-2.51GHz with channel spacing of 5MHz is designed through Samsung CMOS 65nm process. The phase noise and low power consumption are important factors for phase locked loop (PLL) design considering RF transceiver performance. The phase noise characteristics of proposed frequency synthesizer can be improved by dividing the large tuning range into a sub-band range with a small gain of VCO. Phase noise can be reduced by choosing the appropriate code value assigned to the desired channel using AFC (auto frequency calibration). Also, AFC's power consumption could be decreased in coarse tuning mode. It consumes 14 mW during the coarse tuning mode and 11 mW during the fine tuning mode at 1.2V supply, respectively. It occupies an area of 1.73 mm × 1.73 mm including PADs. The simulated phase noise characteristic of the frequency synthesizer is -125dBc/Hz at 1 MHz offset from the carrier.**

***Keywords*— Auto frequency calibration, Frequency synthesizer, Low phase noise, Low power consumption**

I. INTRODUCTION

The explosive growth of the telecommunications industry has continuously promoted to increase demand for fully integrated RF transceiver with low cost and low power consumption. Among the various radio communication standards, the need for low data rates and low power software focused on sensor network applications led to the development of the ZigBee standard [1].

Frequency synthesizers are most widely used in a variety of systems such as wired and wireless communication system as well as CPU [2]. Phase noise is an important factor for RF transceiver performance, compared to other factors to considerer for frequency synthesizer design. Low power consumption is also a significant specification for RF transceiver.

This paper presents a 2.4 GHz frequency synthesizer with low phase noise and low power consumption for ZigBee applications. The paper is organized as follows. Section II presents the proposed synthesizer architecture. In Section III, the PLL building blocks are described. The simulated results are shown in Section IV and conclusions are drawn in Section V.

a. Corresponding author; nik@pusan.ac.kr

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II. PROPOSED SYNTHESIZER ARCHITECTURE

Fig.1 shows the block diagram of the proposed RF frequency synthesizer for ZigBee applications. It is composed of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), a programmable swallow divider, and an AFC based on digital counters. As shown in Fig. 2 (a), the VCO gain (K_{vco}) should exceed certain amount in order to obtain broadband frequencies in a VCO with single varactor. Therefore, since the output frequency f_o of a VCO with a large K_{vco} abruptly varies within a wide tuning range, the substantial gain of the VCO can significantly degrade the phase noise performance of the phase-locked loop (PLL) [3]. As shown in Fig.2 (b), the phase noise can be reduced by dividing the large tuning range into a sub-band range with a small K_{vco}. The proposed frequency synthesizer can perform low phase noise by choosing the code value assigned to the desired channel using AFC. It is called coarse tuning mode.

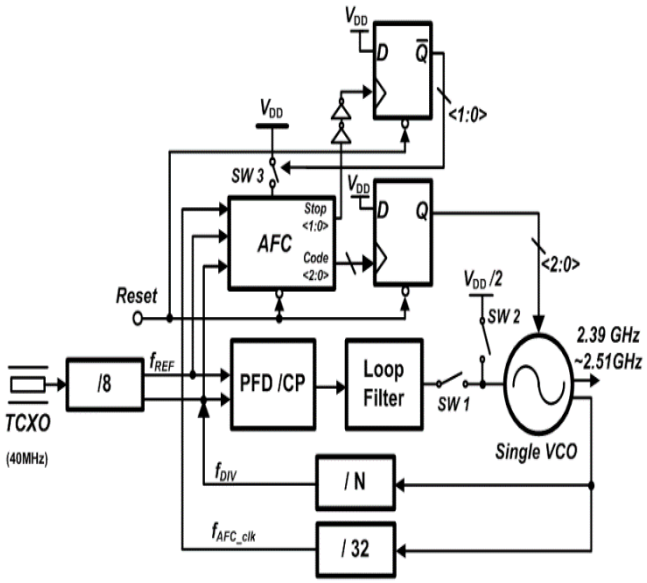
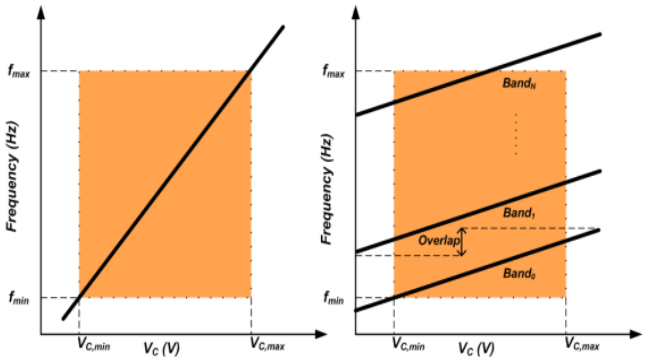


Fig. 1. Block diagram of the frequency synthesizer

Within the selected tuning range, the PLL synthesizes the selected output frequency by synchronizing the output frequency with the reference frequency generated from TCXO. It is called fine tuning mode. After coarse tuning mode, AFC is powered down to low power consumption. Then, the switch SW1 is closed and the SW2 is opened to form a PLL. Although the AFC is powered down, the value of the capacitance code is held by the D flip-flop triggered by the output of codes of the AFC.



(a) (b)

Fig. 2 (a) Single tuning curve, (b) tuning range divided into sub-bands for a wideband VCO operation.

III SYNTHESIZER BUILDING BLOCK

A. AFC

Fig.3 shows the proposed block diagram of the AFC which consists of two counters, a comparator, and a state machine. The flow of proposed AFC operation is as follows. First, two counters (counter1 and counter 2) count the rising clock edge of the reference frequency (f_{REF}) and the divider output frequency (f_{DIV}), respectively. The counter1 and counter2 counts 64 rising clock edges of f_{REF} and f_{DIV}, respectively. The outputs of two counters trigger D flip-flops to produce high logic signals for H_{REF} and H_{DIV}.

If the time difference between H_{REF} and H_{DIV} is larger than three times of the AFC's rising clock edge, the comparator generates an UP signal as shown in Fig.4 (a). The state machine that receives the UP signal from the comparator sequentially generates 3-bit code outputs from 000 to 111. In the opposite case, a DOWN signal is generated from the comparator and input to the state machine.

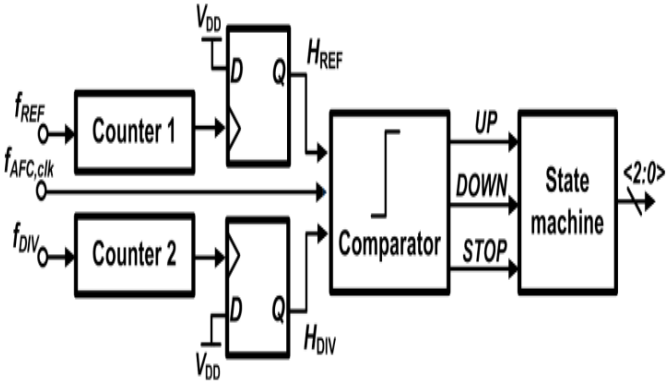
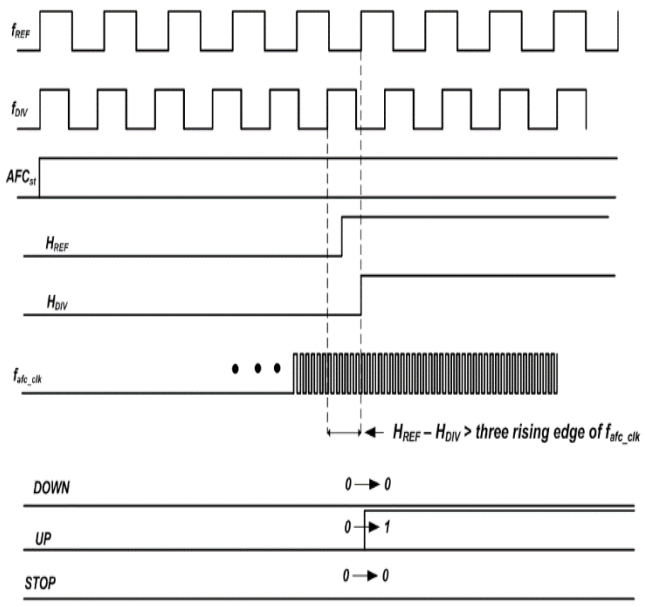


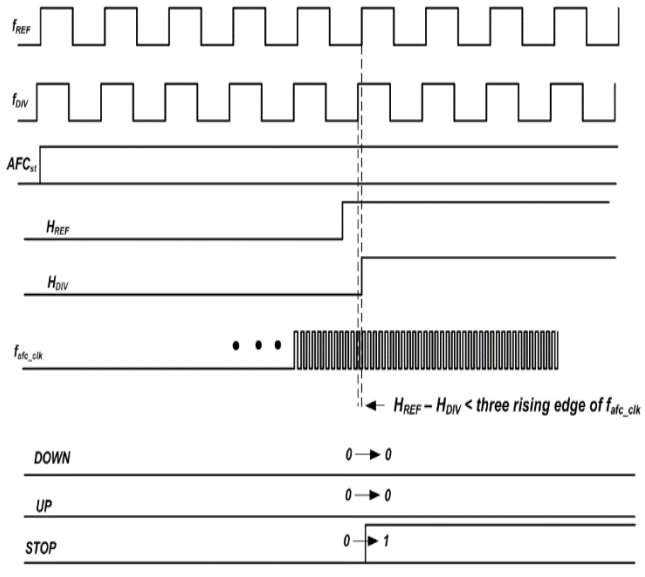
Fig. 3. Block diagram of AFC

In case that the time difference between H_{REF} and H_{DIV} is smaller than three times of the AFC's rising clock edge, the STOP signal is produced as shown in Fig.4 (b). Therefore, AFC is turned off until the RESET signal is input.

In coarse tuning mode, even though the output of the counter1 and counter2 is compared at all rising edges of f_{REF} and f_{DIV}, it can take considerable time to detect the frequency difference due to the initial phase error of f_{REF} and f_{DIV}. Therefore, the coarse tuning time depends on the initial phase relationship.



(a)



(b)

Fig. 4. Timing diagram of AFC operation: (a) when the time difference between H_{REF} and H_{DIV} is larger than three times of the AFC's rising clock edge, (b) when the time difference between H_{REF} and H_{DIV} is smaller than three times of the AFC's rising clock edge.

The flow chart for the digital calibration technique is shown in Fig.5. If the selected channel is out of tuning range, AFC is activated. Then, the switch SW1 is opened and the PLL loop is cut off. The switch SW2 is connected to V_{DD} /2. The time difference between the H_{REF} and H_{DIV} is compared to the clock of AFC to determine whether the output of the comparator is up or down. When the comparator generates STOP signal, the switch SW1 is closed and the switch SW2 is opened again, and the PLL loop is activated for fine tuning.

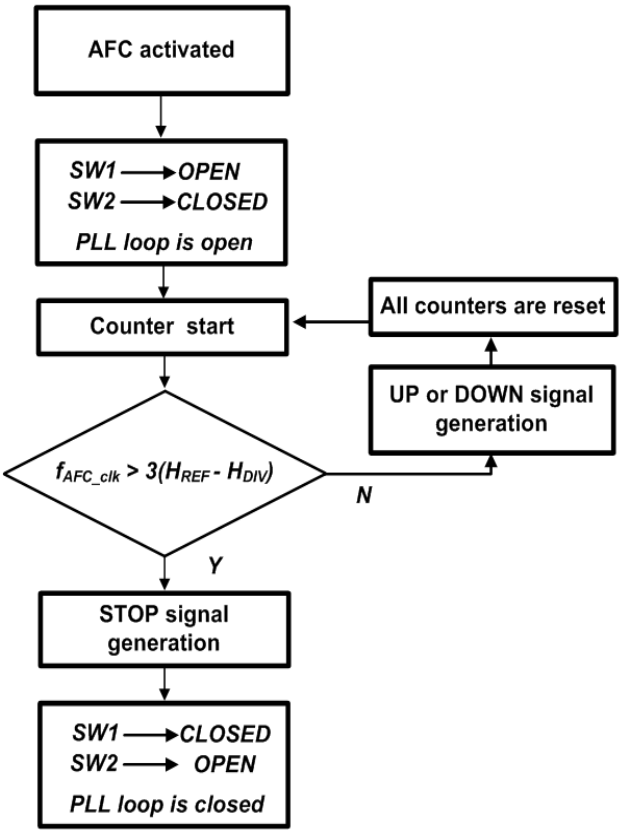
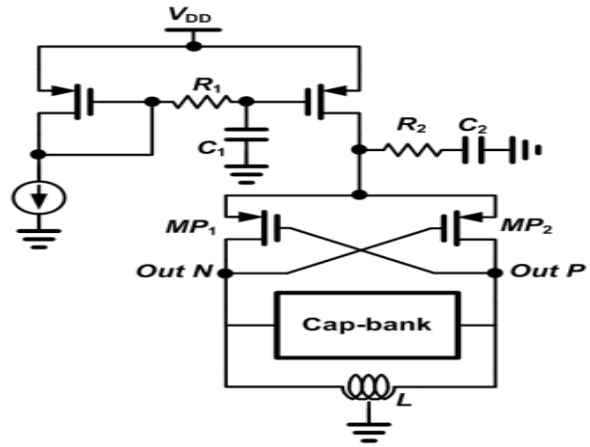


Fig. 5. Flow chart for the auto frequency calibration

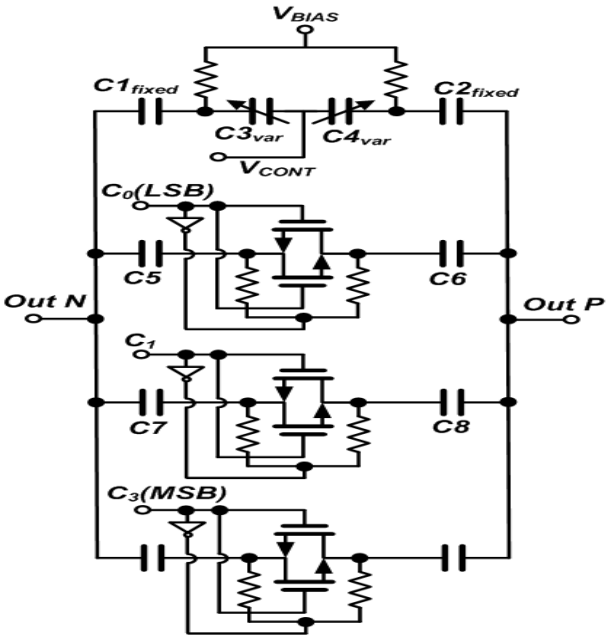
B. VCO

The simplified schematic of the VCO with frequency range from 2.39 to 2.51GHz is shown in Fig.6 (a). The designed VCO has 8 sub-tuning bands with low K_{VCO} of 33MHz. In order to reduce the phase noise caused from flicker noise, the VCO has cross-coupled pMOS transistor pairs. Since the pMOS transistor has small flicker noise compared to nMOS one, the VCO can have relatively low phase noise.

On the other hand, the noise from current source degrades the phase noise performance of a VCO [5]. It can be solved with low-pass filter composed of R_1 and C_1. Also, in order to reduce second-order harmonics of the oscillation frequency f_O, the low-pass filter composed of R_2 and C_2 is used as shown in Fig. 6 (a). Fig.6 (b) shows switchable capacitor-bank that is coarsely controlled by a 3-bit control signal. The VCO operates at the lowest frequency when the capacitor bank has maximum capacitance.



(a)



(b)

Fig. 6. (a) Schematic of VCO, (b) Capacitor-bank schematic

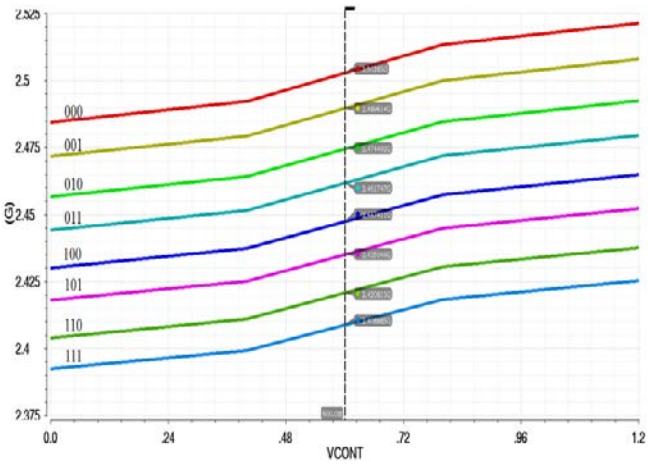


Fig. 7. Simulated tuning characteristics of the VCO

C. Gain-boosting Charge Pump

A conventional CMOS charge pump (CP) circuit has the current mismatch problem because the CMOS CP has up and down switch made of pMOS and nMOS, respectively. The mismatch between up and down current in a conventional CMOS CP causes several problems in phase-locked loop system, such as reference spurs [6]-[10]. The unbalanced charge pump has the static phase error which generates the fixed pattern jitter or degrades performance of PLL. In order to minimize current mismatch between up and down current, the gain boosting topology is adopted [11]. Fig.8 shows the simplified schematic of the designed charge pump. As shown in Fig.9, the current mismatch between up and down operation is under 5% without additional power consumption.

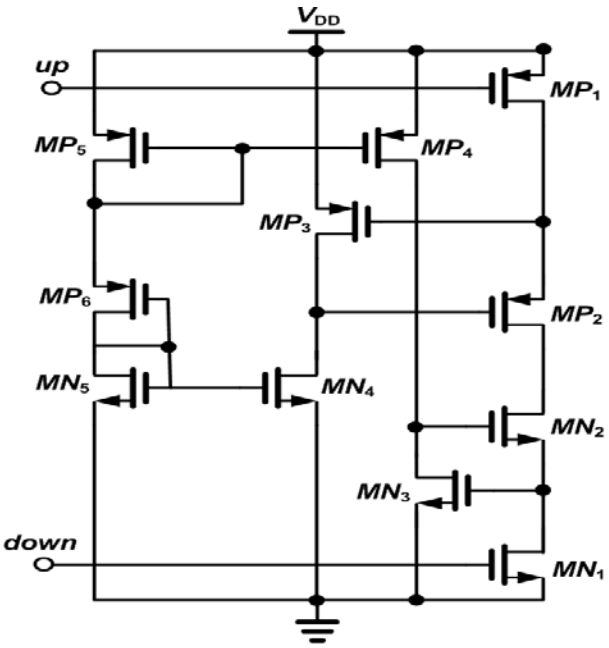


Fig. 8. Schematic of the charge pump

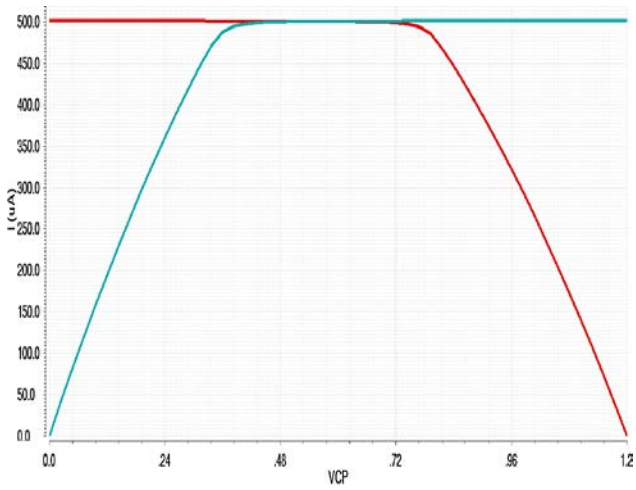


Fig. 9. Up and down output current of the charge pump using gain-boosting topology

IV. SIMULATION RESULTS

A. Transient response

The VCO control voltage is shown in Fig. 10. In the coarse tuning mode, the control voltage of VCO is connected to $V_{DD}/2$ and AFC begins to find the value of the capacitor-bank code for sub-band tuning range selection. After AFC operation is completed, the fine tuning mode is started.

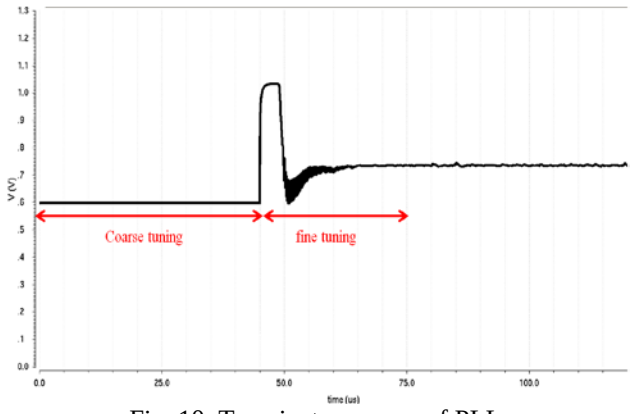


Fig. 10. Transient response of PLL

B. Phase noise simulation

The overall PLL phase noise performance is characterized by the noise contributions from all PLL circuits. Fig. 11 shows the linear phase–domain model of a PLL with additive noise source. θ_{ref} represents the noise source that appears at the reference input to the PFD. The noise source includes the noise from the crystal oscillator, crystal buffer, and reference divider. $\theta_{divider}$ shows the noise from the divider. θ_{VCO} and θ_{pfd} express the phase noise of the VCO and PFD, respectively. θ_{vcntr} represents the noise at the VCO control voltage by the loop filter. Fig. 12 shows the phase noise of the noise sources extracted from each block.

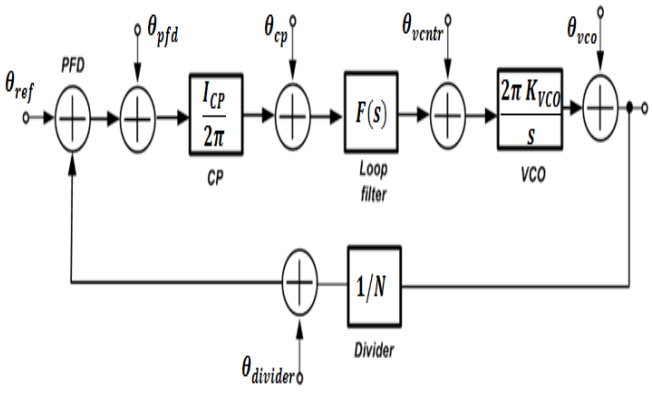
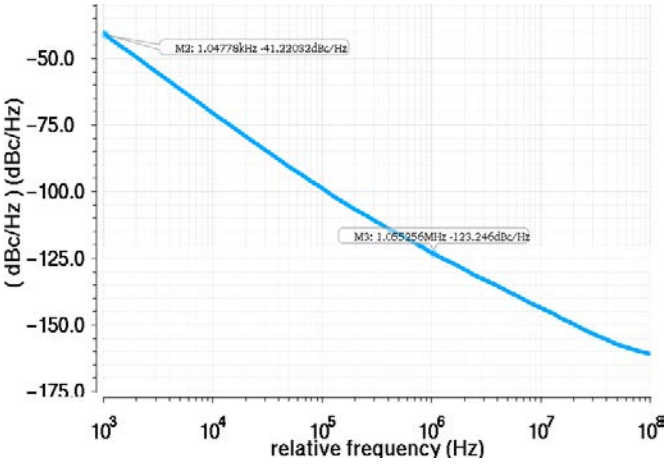


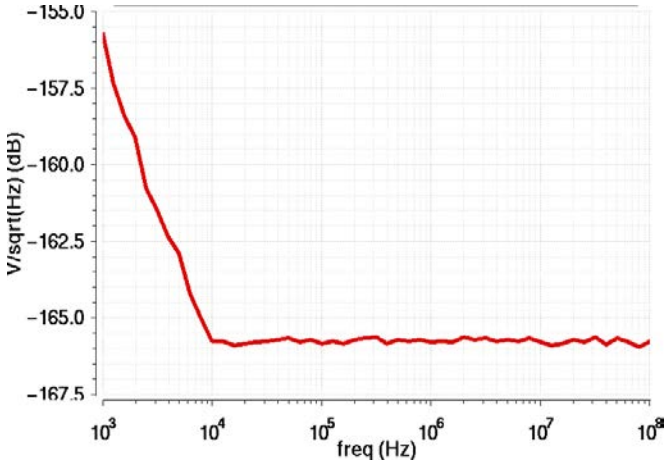
Fig. 11. Equivalent circuit model to simulate PLL phase noise

The phase noise of a VCO in a PLL is shaped by a PLL noise transfer function. A phase noise of a free running VCO is simply called VCO phase noise, while the phase noise of the VCO in a locked PLL is called PLL output phase noise.

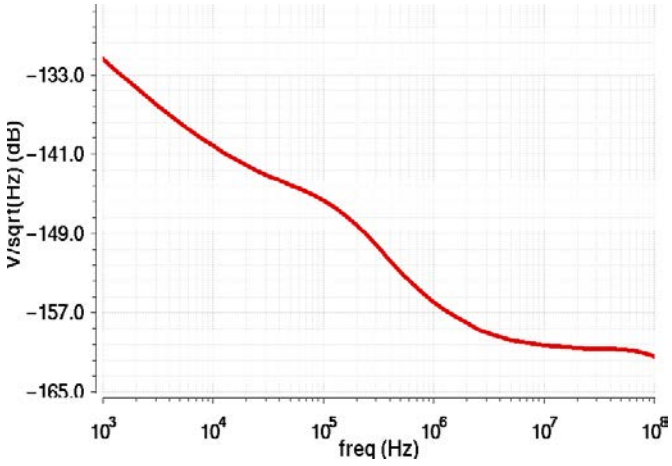
The total simulated phase noise results are presented in Fig.13. The simulated phase noise of fine tuning loop is -125 dBc/Hz at 1 MHz offset from the carrier. The phase noise of a crystal oscillator has an impact on the closed-in phase noise at 10 kHz of the PLL while VCO noise shapes phase noise of a PLL at 400 kHz offset. The phase noise of a PFD and CP increases in-band phase noise floor.



(a)



(b)



(c)

Fig. 12. (a) Phase noise of the VCO, (b) Phase noise of the TCXO, (c) Phase noise of the PFD and CP.

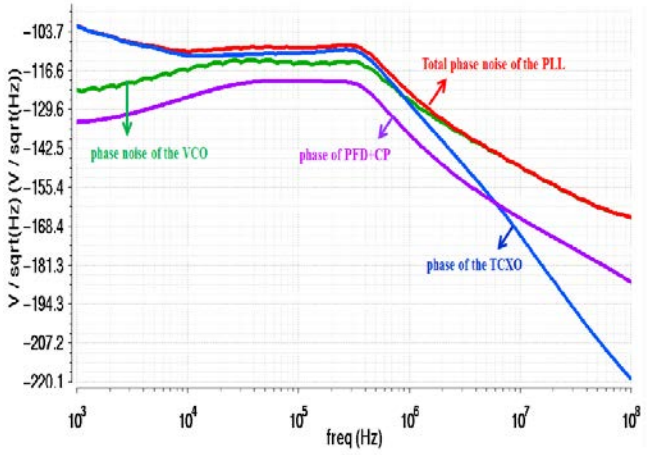


Fig. 13. Simulated total output phase noise of the frequency synthesizer.

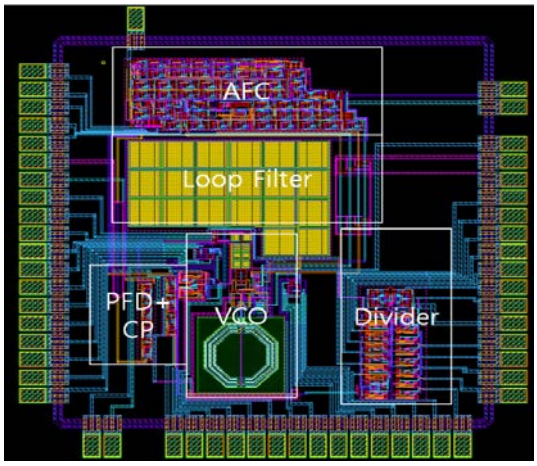


Fig. 14. Layout diagram of the frequency synthesizer

V. CONCLUSIONS

A low phase noise 2.4 GHz CMOS RF frequency synthesizer for ZigBee communication system is presented. By using a coarse tuning loop, the frequency synthesizer achieves improved phase noise performance. Since the designed synthesizer is capable of covering target frequency tuning range and a low K_{vco} of 33MHz, it is suitable for ZigBee applications.

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Sung Wook Yoon received the B.S. degree in electrical engineering from the Pusan National University, Pusan, Korea, in 2016.
His main interests are RF system circuits for wireless communications, especially RF/Analog/Millimeter wave Integrated circuit.

Chang Yeol Kim received the B.S. degree in electrical engineering from the Pusan National University, Pusan, Korea, in 2016.
His main interests are RF system circuits for wireless communications, especially RF/Analog/Millimeter wave Integrated circuit.

Yang Ji Jeon received the B.S. degree in electrical engineering from the Pukyong National University, Pusan, Korea, in 2017.
His main interests are RF system circuits for wireless communications, especially RF/Analog/Millimeter wave Integrated circuit.

Il Ku Nam received the B.S. degree in EE from Yonsei University, Korea, in 1999, and the M.S. and Ph.D. degrees in EECS from the KAIST, Korea, in 2001 and 2005, respectively. From 2005 to 2007, he was a Senior Engineer with Samsung Electronics, Gyeonggi, Korea, where he was involved in the development of mobile digital TV tuner IC. In 2007, he joined the School of Electrical Engineering, Pusan National University, Busan, Korea, and is now a Professor.

A Wideband Bi-Directional Gain Amplifier with Asymmetric Cell using Cascade Gain Boosting in 65nm CMOS Process

Van Viet Nguyen, Hyo Hyun Nam[1], Jung Dong Park[a]
Division of Electronics and Electrical Engineering, Dongguk University, Seoul
E-mail: [1]kahn0217@dongguk.edu

Abstract **- A bidirectional distributed gain amplifier (BDGA) with asymmetric cell combined with a cascade gain boosting structure is presented in this paper. Conventional DA designs generally have the gain limitation because of the additive gain mechanism, whereas the proposed structure can benefit significantly from the multiplicative gain mechanism due to the cascade of two BDGAs. Moreover, the unit gain cells are intentionally designed to be asymmetrical with the common source (CS) configuration at output stages to improve the output power of the circuit. The proposed circuit architecture is fabricated in a standard 65 nm CMOS. The measurement results show the gain of 10.5 dB, and the 3-dB bandwidth from 5.8 - 17.6 GHz. The measured output P_{1dB} is 6.8 dBm along with 9.3 dBm of the saturated output power at 10 GHz. The circuit draws a current of 75 mA from a 1.2 V supply and occupies 1.1 x 0.6 mm^2 of chip area.**

***Keywords*— Asymmetric cell, Bidirectional distributed CMOS, Gain amplifier, Gain boosting stage.**

I. INTRODUCTION

With the rapid progress of CMOS technology, which has been applied variously not only in defense industry but also commercial sectors such as automotive radar and high-speed communication, the active phased array technology has reached its maturity phase [1,2]. The transmit/receive module (TRM) plays the most critical role and has a significant impact on the entire cost and weight of active phased array systems. As a result, constant efforts have been putting into the research of new topologies for T/R module to reduce its cost, weight, power consumption, die area and simultaneously to increase its robustness and function [3]. Because the design of an active phased array front-end system requires thousands or even ten thousand of building elements, cutting down the cost per single TRM gives a substantial contribution to cost reduction of the phased array system especially in many low-cost applications [4]. Moreover, advances in digital signal processing have enabled digital beam forming mechanism in phased array system to integrate with amplitude and phase setting section. Digitally controlled phase shifter and attenuator consist of many CMOS switches which result in relatively high insertion losses due to the conductive silicon substrate. To recover the signal level from the losses of the aforementioned functional circuits, a broadband gain amplifier has to be included in the signal path of each T/R module. Since passive phase shifter and attenuator can operate in both transmit and receive directions, it is required that the gain amplifier should also be bi-directional to make the module more compact. The typical structure of a bi-directional amplifier is composed of two SPDT switches selecting signal paths between two separate amplifiers [5]. Even though this configuration can be optimized independently to achieve high output power transmission and low noise figure for receive paths, it shows poor high-frequency performance due to the loss of MOS switches and takes up large chip area because of separate amplifiers. As an attempt to remove T/R switches, a topology utilizing controllable impedance matching networks has been proposed [6]. This approach could separate the power amplifier and low-noise amplifier by setting different matching conditions directly via biasing. However, two separate amplifiers are still needed, and operable bandwidth is limited due to the impedance matching. Another way to remedy its shortcomings was by configuring common gate, which makes possible to select the amplification direction [7]. However, lossy MOS switches and low output power are significant drawbacks of this configuration. To resolve this weakness as mentioned earlier, taking the distributed amplifier's characteristic, which is well-known with its wideband, was proposed. The conventionally distributed amplifiers have been adapted to provide bi-directional operation by adding a parallel amplification branch for a "reverse direction mode." It can be a satisfactory solution for low-cost wideband applications [8, 9]. However, additive gain mechanism sets limitation upon the gain of the bidirectional distributed amplifier and also output power is not high enough.

This paper presents a new bidirectional distributed gain amplifier inherited broadband characteristic from the conventional distributed amplifier, high gain from the

a. Corresponding author; jdpark@dongguk.edu

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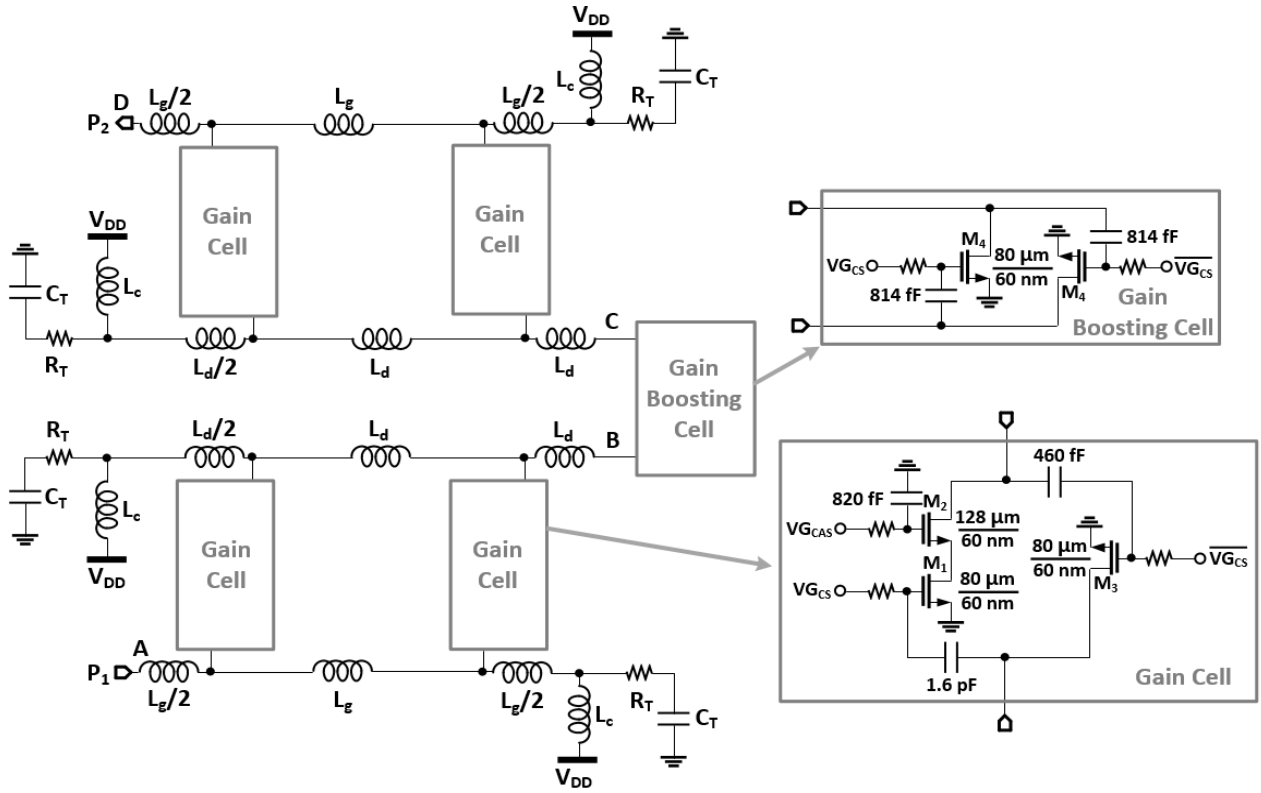

Fig. 1. The circuit schematic of new BDGA with gain and output power enhancement.

multiplicative mechanism, and high output power from the asymmetric gain cell configuration.

II. DESIGN OF BDGA

In general, with the assumption that the transmission lines are lossless, the voltage gain (G) of the conventional distributed amplifier can be expressed as:

$$\mathrm{G} = G_0\mathrm{N} = \frac{g_0 Z_0 N}{2} \tag{1}$$

where N is the number of the distributed stages, g_m represents the transconductance of a single stage, and G_0 is the gain of a single stage. The characteristic impedance Z_0 is typically 50 Ω. It is noteworthy that the factor of ½ implies that half of the output signal travels along the opposite direction towards the drain termination. As observed from the estimated gain equation, the conventional distributed amplifier shows the additive gain mechanism $\mathrm{N} \times G_0$ contrasting with the gain of a cascade of N amplifier stages which increase as $G_0\mathrm{N}$. This fundamental characteristic of the conventional structure of distributed amplifier leads to the gain limitation, which is typically less than 10 dB for the reported designs.

Conventional BDGA shows that the limitation on the gain is from the additive gain mechanism as well as the loss of artificial transmission lines. To overcome this bottleneck, we cascaded two separate BDGAs with a common source (CS) stage. As demonstrated in Fig. 1, the circuit is composed of two 2-stage BDGAs and a CS stage for the gain-boosting in the middle. With the basic concept similarly to conventional BDGA, on-chip inductors and parasitic capacitances of transistors form the input and output artificial transmission lines which make the circuit broadband operation. Because of the cascade connection between each BDGA, the circuit takes advantage of the multiplicative gain mechanism. The voltage gain of cascade BDGA can be approximated by (2)

$$\begin{aligned} A_v &= A_{v1} \times A_{v2} \times A_{v3} \\ &= 2\left(g_{m1}\frac{Z_0}{2}\right) \times (g_{m2}Z_0) \times 2(g_{m3}\frac{Z_0}{2}) \end{aligned} \tag{2}$$

The number of gain cells in the first and third stages is chosen equal to two considering total chip area which is comparable with existing conventional BDGAs. If the building elements of all three cascaded stages are made the same, even though the gain can be significantly improved, the circuit introduces degradation in the output power. Hence, the first stage employs a cascode transistor pair configuration which is better for higher gain while second and third stages are made up by a single transistor in CS configuration demonstrating improvement on output power. The asymmetry of the unit gain cell does not affect the bidirectional function of the circuit. As can be seen in Fig. 1, the forward and backward paths are entirely identical. The detailed circuit schematics and device parameters of the gain cell and gain boosting stage are shown in Fig. 1.

The gain cell consists of cascode transistor pair (M_1 and M_2) in the forward direction and CS structure for reverse direction in connection with gate and drain inductors (L_G and L_D), 50 Ω termination resistors, and RF chokes inductors (L_C). Cascode configuration provides better gain-bandwidth and simpler biasing. The mechanism to control the operation mode of the amplifier is set by changing the bias voltages applied to gate terminals. For instance, in the forward mode operation, transistor M_1 and M_2 are ON in saturation region, and the transistor M_3 is OFF. The shunt capacitances at the input are comprised of the gate capacitance of M_1 in saturation and drain capacitance of M_3 in off, which along with gate inductances $L_D/2$ form the artificial transmission line whose characteristic impedance Z_0 is approximately expressed as:

$$Z_0 = \sqrt{L_G/C_G} = \sqrt{L_D/C_D} \quad (3)$$

By appropriately choosing MOSFET device sizes and inductor values, we can achieve Z_0=50 Ω of the artificial transmission-line. As a result, the circuit demonstrates wideband frequency response with better input and output return loss. To supply for the circuit in both operating modes, two V_{DD}'s are supplied at two ends of the amplifier. The capacitor at the gate of input transistor isolates its gate bias voltage from V_{DD}. All bias voltages are provided through 24 kΩ resistors as shown in the figure. All the parasitics and coupling of the passive elements were considered in design by performing 3D EM simulation with HFSS as shown in Fig. 2.

Fig.3 demonstrates the improvement of output P_{1dB} with asymmetric cell structure in which CS configuration is employed at the output stage in comparison with the symmetric one using symmetric cascode structure. Two different structures were investigated with post-layout simulation at the same DC bias current. The output P_{1dB} of the proposed cell structure is significantly better than that with the symmetric structure. Since the signal after the gain boosting cell is quite large, the use of the cascode structure at the output stage can degrade the gain and the output power. This is mainly because the amplifier at the output stage is saturated. Therefore, it is shown that the output P_{1dB} of the proposed asymmetric structure is much better than the symmetric structure.

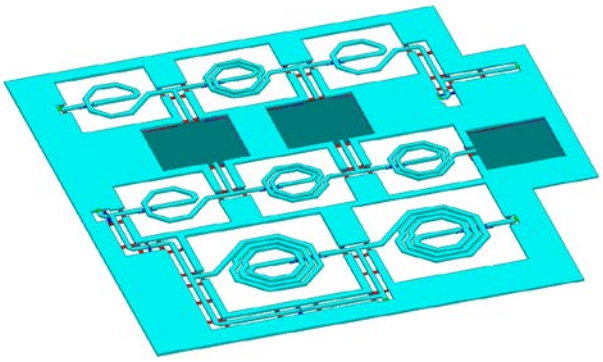

Fig. 2. Passive structure of BDGA simulated in HFSS.

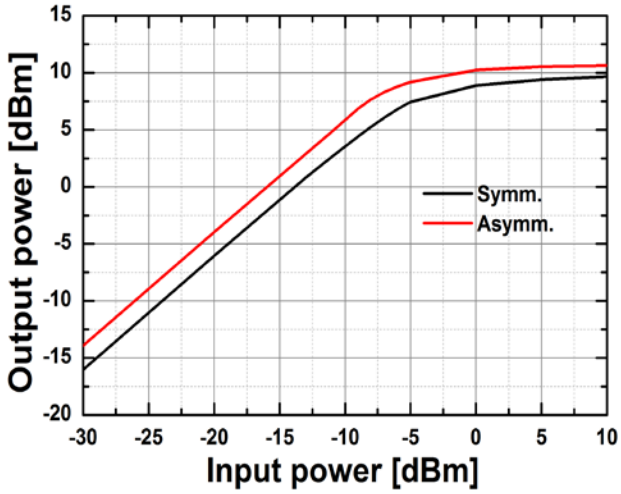

Fig. 3. The comparison between output powers of 2 different configurations.

Fig. 4 shows the voltage waveforms at nodes A, B, C, and D marked in Fig. 1, respectively. The dependence of circuit performance in temperature is shown in Fig. 5. As can be seen in Fig. 6, the proposed BDGA shows the group delay of lower than 150 ps from 4 – 24 GHz, which depends slightly on temperature. Regarding noise characteristic of the circuit, Fig. 7 presents the simulated results when varying the temperature.

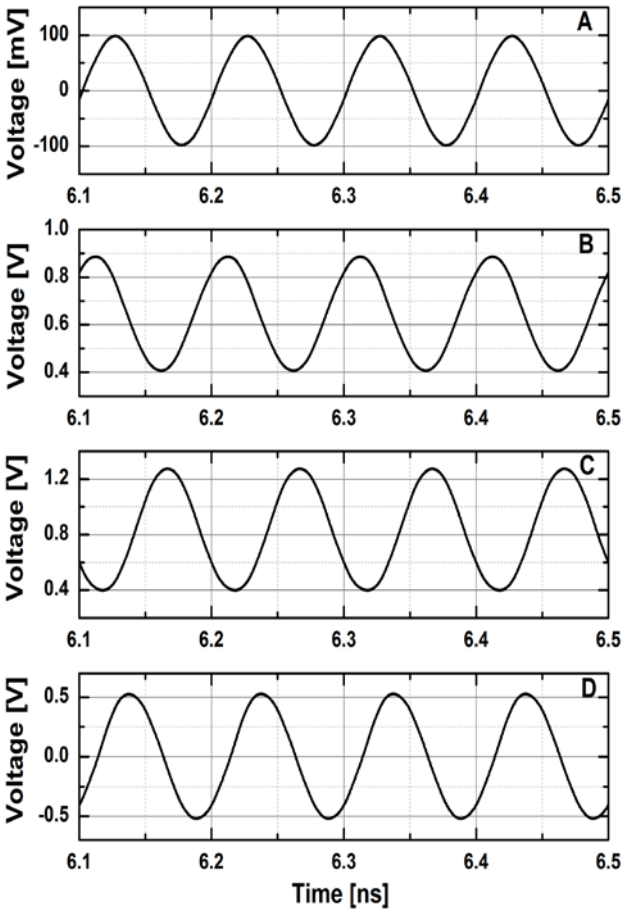

Fig. 4. The voltage waveforms at nodes A, B, C, and D marked in Fig. 1, respectively

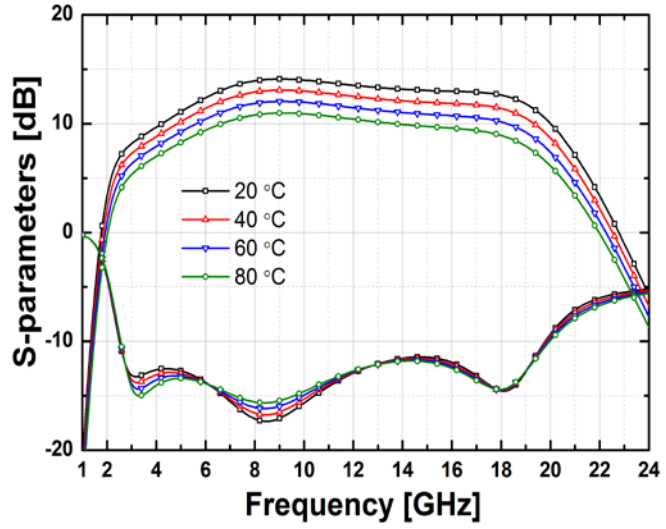

Fig. 5. Simulated S-parameters of the proposed BDGA depends on temperature.

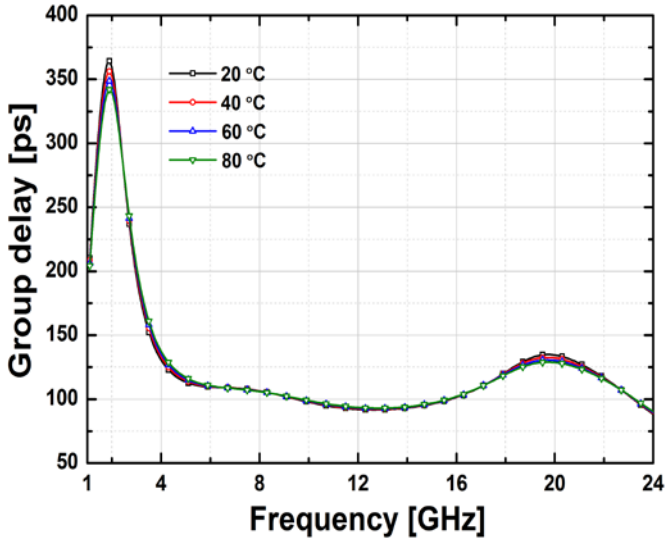

Fig. 6. Simulated group delay of the proposed BDGA

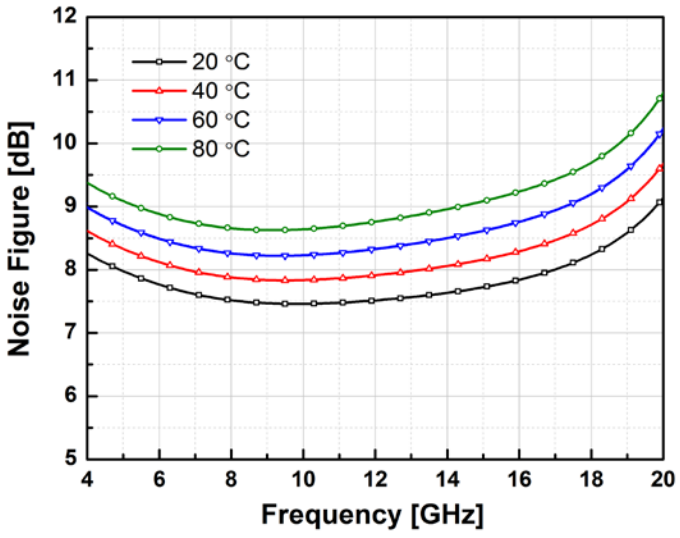

Fig. 7. Simulated noise figure of the proposed BDGA varying with temperature.

III. MEASUREMENT RESULTS

Fig. 8 shows the microphotograph of the implemented bi-directional distributed amplifier in Samsung 65nm CMOS technology. The implemented circuit occupies a die area of 1.1 x 0.6 mm^2 without pads. The setup for S-parameter measurement is sketched in Fig. 9. S-parameters are measured on-chip by Keysight PNA Network Analyzer with SOLT calibration. The measured results are correctly matched with the simulation as it is shown in Fig. 10. The transmission gain (S_{21}) of the fabricated BDGA is about 10.5 dB at 10 GHz, and input/output return losses are around 10 dB at 6 – 18 GHz. The isolation between the forward and reverse directions is better than 50 dB. Bi-directional performance of the implemented BDGA. As depicted in Fig. 10, the similarity between the forward and reverse directions is visualized in a graph. The measured output P_{1dB} is 6.8 dB m, and the saturated output power of the implemented BDGA is 9.3 dBm at 10 GHz as presented in Fig. 12.

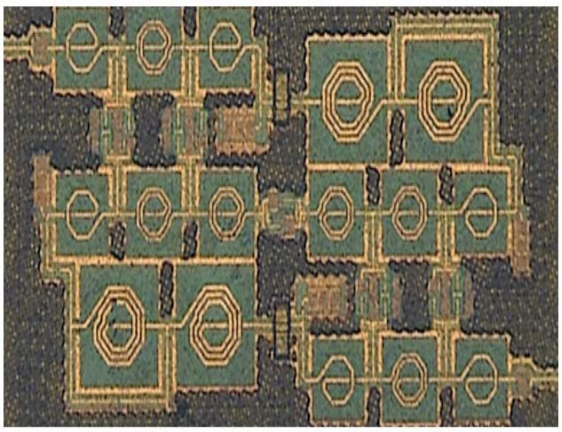

Fig. 8. The microphotograph of the proposed bi-directional distributed amplifier.

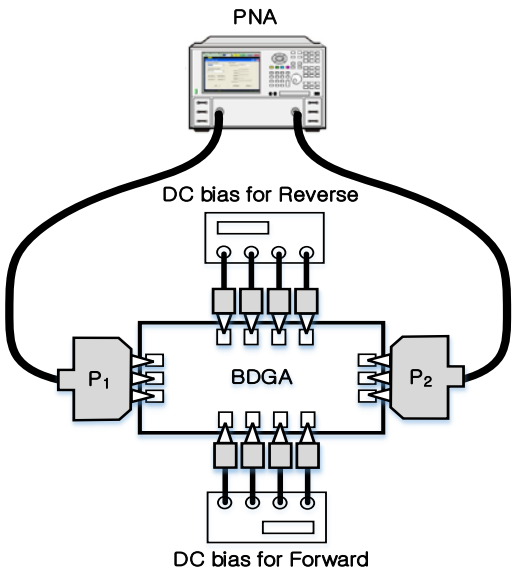

Fig. 9. Setup for S-parameter measurement of the fabricated BDGA.

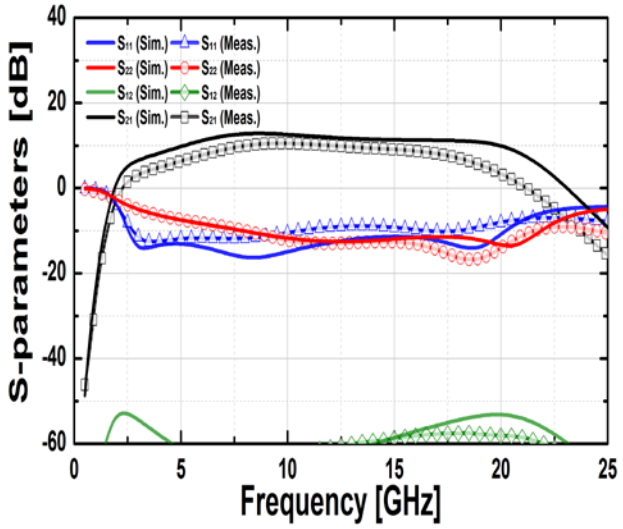

Fig. 10. The measured and simulated S-parameters of the BDGA

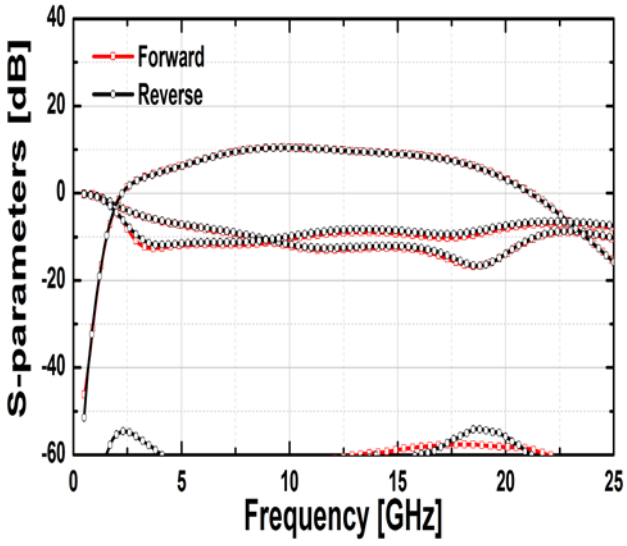

Fig. 11. The measured S-parameters of the BDGA in two directions.

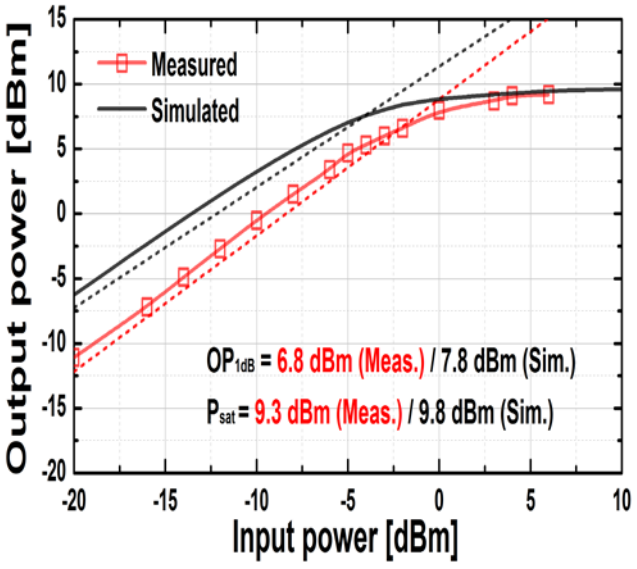

Fig. 12. The measured and simulated output power of the BDGA at 10 GHz.

IV. CONCLUSIONS

A bi-directional distributed gain amplifier with relatively high gain and high output P_{1dB} is presented. The proposed amplifier utilizes a cascaded stage in the middle of the distributed amplifier to boost gain and consists of the asymmetric bi-directional gain cells to improve the output P_{1dB}. The fabricated BDGA achieves 11.8 GHz of the 3-dB gain-bandwidth (5.8 - 17.6 GHz), 6.8 dBm of output P_{1dB} and 11 dB of the saturated output power whereas drawing 75 mA from a 1.2 V supply.

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Van Viet Nguyen received the B.S. degree in electrical and electronics engineering from Ho Chi Minh City University of Technology, Vietnam, in 2015, and is currently studying the Master's degree in electrical and electronics engineering at Dongguk University, Seoul, Korea.
His research interest is T/R module designs for phased-array systems.

Hyo Hyun Nam received the B.S. and M.S. degree in electrical and computer engineering from University of Seoul, Seoul, Korea, in 2013 and in 2015, respectively. He is currently pursuing the Ph.D. degree in electronics and electrical engineering at Dongguk University, Seoul, Korea.
His current research interests include advanced CMOS device designs and RF integrated circuits.

Jung Dong Park received the B.S. degree from Dongguk University, Seoul, Korea, in 1998, the M.S. degree in GIST, Gwangju, Korea, in 2000, and the Ph.D. degree in EECS from the UC Berkeley, in 2012. During his Ph.D. studies, he explored various analog, RF, mm-wave, THz circuits, and TRx architectures in Silicon.
His research area includes device physics & modeling, analog, RF, mm-wave IC, and microwave electronics.

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401, 12, Munjeong-ro, Seo-gu, Deajeon, Republic of Korea

IC Design Education Center (IDEC)
291 Daehak-ro, Yuseong-gu, Daejeon, 34141, Republic of Korea
Tel. +82-42-350-8533 / Fax. +82-42-350-8540

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