Analysis of audio frequency ground integrity in TDMA smartphone system

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***Abstract* - In this paper, we designed a first-order discrete-time sigma-delta modulator to analyze the effects of ground noise coupling to audio circuits. The noise-coupling problem generally occurs in a time-division multiple access (TDMA) smartphone when its RF amplifier switch at 217 Hz to transmit signals for communication. We designed the modulator for operation at 3.3 V DC power and 6.144 MHz sampling frequency with 48 kHz baseband sampling frequency and 128 oversampling rate. With the designed modulator, we analyzed the output noise of the modulator when a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground node of the circuit. The modulator has shown a -50 dB 6 kHz noise power. Furthermore, we fabricated different designs of PCBs to mount the designed modulator and analyze the output noise of the modulator depending on PCB design. In the analysis, the amount of noise coupling reduced as the shared return current path between the modulator and a noise source on PCBs reduces.**

***Keywords*—Delta-sigma modulator, Ground noise, Time-division multiple access**

I. INTRODUCTION

In recent years, multifunction systems with small form factors have become a common requirement in the mobile device market. Because of this demand, various circuit blocks such as analog, digital, mixed mode, and RF blocks has been increasingly integrated into small systems, which is increasing the signal, power, and ground noise coupling between integrated circuits (ICs). Therefore, many researches are being conducted on signal and power integrity in integrated systems to solve signal and power integrity problems [1]-[9]. However, little research has been conducted on ground integrity (GI) [10], [11], and even those studies are mainly discussing GI in the high frequency domain [12]. This is because, even until recently, low frequency grounding is misunderstood as an equipotential point or plane that serves as a reference potential for circuits and systems.

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However, since the grounding structure of a handheld device has a finite size, it has finite impedance and can no longer be defined as equipotential points or planes. This will consist of a network of all interconnections that carry the current returning from the power-consuming circuits to the power supplier, and is termed the ground distribution network (GDN). Even at low frequencies, the small but finite impedance of GDN may cause ground noise coupling to low frequency targeting analog circuits and degrade the circuit performance. A common example is audio noise on smartphones using time-division multiple access (TDMA) communications [13]. Audio noise can have a direct impact on users and can have a significant impact on the reputations of smartphones.

The common audio noise in smartphones is bumblebee sound generated by the cellular phone's TDMA RF power

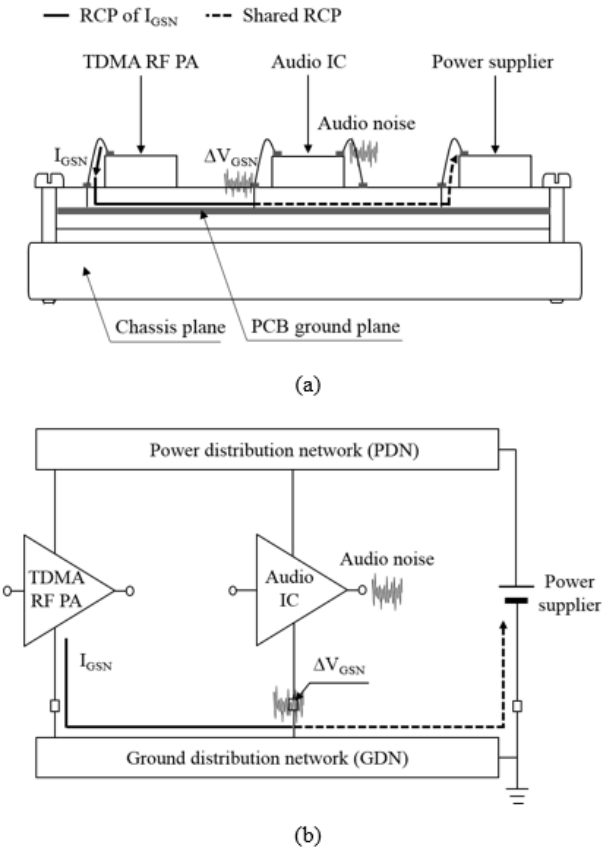

Fig. 1. Ground noise coupling mechanism between an audio IC and a TDMA PA in a smartphone. (a) Conceptual diagram (b) Block diagram.

amplifier (PA). Since 1990s, there have been many studies to solve this problem. However, the studies are focusing only on radio frequency interference or suppression of the noise through post processing the audio signal [14]-[18], and there is no research into ground noise coupling from RF PA to audio ICs.

Fig. 1 illustrates the mechanism by which ground noise is coupled and eventually leads the bumblebee noise to an audio IC in a TDMA smartphone. Ground noise coupling can occur while the operating current of the TDMA RF PA is flowing through the GDN of a smartphone that is composed of various components, such as the PCB plane and the chassis plane. TDMA RF PAs operate by switching at an audio frequency, which consumes a large switching current from the power supply during switching. For example, RF PAs in Global System for Mobile Communications (GSM), a typical example of a TDMA communication standard, consumes large switching currents of 1 to 3A (I_{GSN}) with a duty cycle of 12.5% at a frequency of 217 Hz [19]. This large current returns to the power supplier via the smartphone's GDN, and the path that this return current takes is called the return current path (RCP). When a large current flows through RCP, the non-zero impedance of the GDN causes the GDN voltage to fluctuate. At this time, when the audio IC is placed on the RCP of the RF PA and shares the RCP of the RF PA, the voltage of the ground node of the audio IC fluctuates to the TDMA frame rate. The ground voltage fluctuation (ΔV_{GSN}) degrades the performance of the audio IC and generates audible noise to the user.

Therefore, in this paper, we design a discrete-time sigma-delta modulator, the most suitable block in the data converters for audio application [20], to analyze the audio frequency ground noise coupling effect on audio circuits.

II. EXPERIMENTS

A. System level design of sigma-delta modulator

The first-order discrete-time modulator is designed and simulated with Virtuoso schematic editor from Cadence. Fig. 2 shows the overall block diagram of the designed circuit. The modulator comprises sampling circuits, an amplifier, a comparator and 1-bit DAC. The design and targeted performance of each block are discussed in later chapters. The maximum signal-to-noise (SNR) for n-order modulator can be expressed as (1), where N is the order and OSR is the over-sampling ratio of the modulator [21]. According to (1), the maximum SNR of the modulator becomes 66 dB.

$$SNR_{\max} = 10\log(\frac{3}{2}2^{2N}) + 10\log(\frac{3}{\pi^2}(OSR)^3) \quad (1)$$

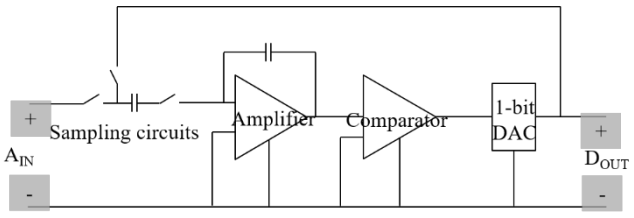

Fig. 2. Block diagram of the designed first-order discrete-time sigma delta modulator

B. Design of a switched capacitor integrator

The two switched capacitors sample the internal thermal noise as well as the input signal. Due to the oversampling operation of the modulator, the frequency bandwidth of the sampled noise power is spread and the noise power of the baseband is adjusted to a value divided by oversampling, and (2) expresses this value. With a 4dB additional noise margin and a target SNR of 70dB, the minimum required capacitor can be found \ as in (3). We set the capacitor value as 1 pF.

$$P_{noise} = \frac{2KT}{C \times OSR} \quad (2)$$

$$\sqrt{P_{noise}} \le -70dB \quad (3)$$

C. Design of a two-phase non-overlapping clock generator

A switched capacitor circuit requires two-phase non-overlapping clocks to reduce the signal-dependent charge injection. Fig. 3 shows the block diagram of the designed clock generator. The two cross-coupled NAND gates with inverters generate two clock signals with opposite phases, CLK1 and CLK2. A series of two inverters consist a single delay line, and it delays the two clock signals and generate CLK1D and CLK2D. The delay time is determined 32 ns, one-fifth of the input clock signal. Table I shows the transistor parameters of the designed clock generator.

D. Design of an operational amplifier

A folded cascode scheme is chosen to keep the output range as broad as possible. A differential input and single-ended output folded cascode operational amplifier is designed to have a DC gain higher than 60 dB, a gain-bandwidth greater than 24.6 MHz, which is 4 times the sampling frequency, and slew rate greater than seven times the reference frequency multiplied by a reference voltage of 1.65V, for reliability of the entire modulator. Fig. 4 shows

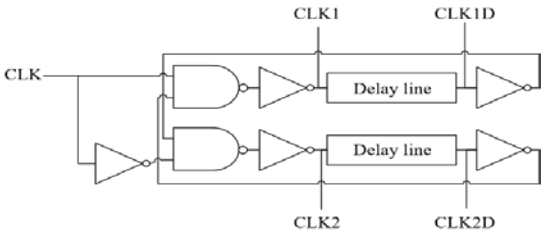

Fig. 3. Block diagram of the designed clock generator

TABLE I.
Transistor parameters of the designed two-phase non-overlapping clock generator

Transistor name	Transistor size W/L[um/um]
PMOS of inverters	0.595/0.35
NMOS of inverters	0.220/0.35
PMOS of delay lines	0.595/4.9
NMOS of delay lines	0.220/4.9
PMOS of NAND	1.015/0.35
NMOS of NAND	0.440/0.35

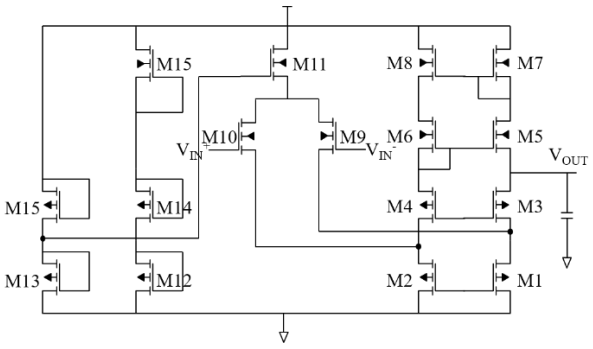

Fig. 4. Schematics of the designed folded cascode operational amplifier

TABLE II
Transistor parameters of the designed folded cascode operational amplifier

Transistor name	Transistor size W/L[um/um]
M1 ~ M10	150/0.7
M11, M15	3/0.7
M12 ~ M15	50/0.7

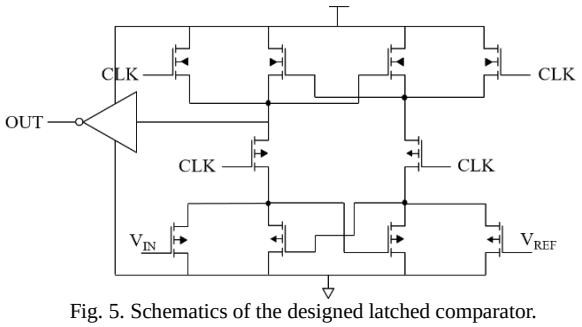

Fig. 5. Schematics of the designed latched comparator.

TABLE III
Transistor parameters of the designed latched comparator

Transistor name	Transistor size W/L[um/um]
PMOS of the comparator	0.595/0.35
NMOS of the comparator	0.220/0.35

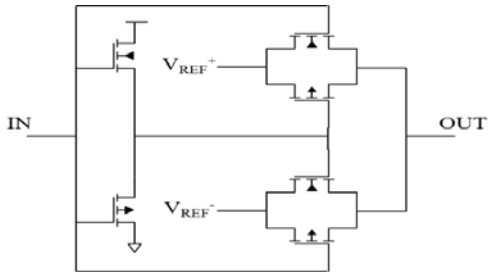

Fig. 6. Schematics of the designed 1-bit DAC.

TABLE IV
Transistor parameters of the designed 1-bit DAC

Transistor name	Transistor size W/L[um/um]
PMOS of the comparator	0.595/0.35
NMOS of the comparator	0.220/0.35

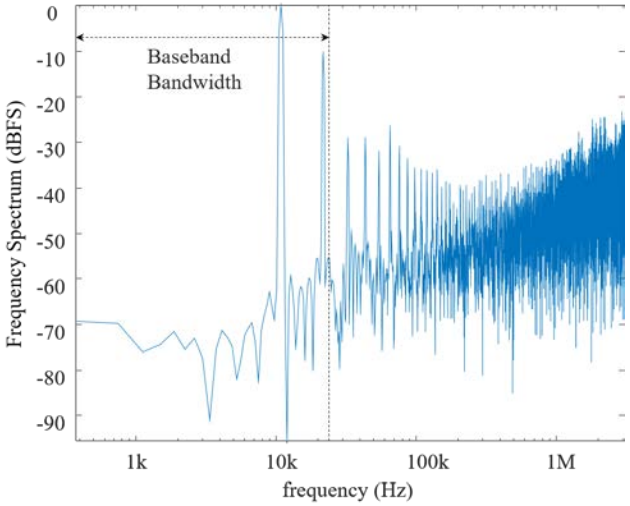

Fig. 7. Simulated frequency spectrum of the designed sigma delta modulator

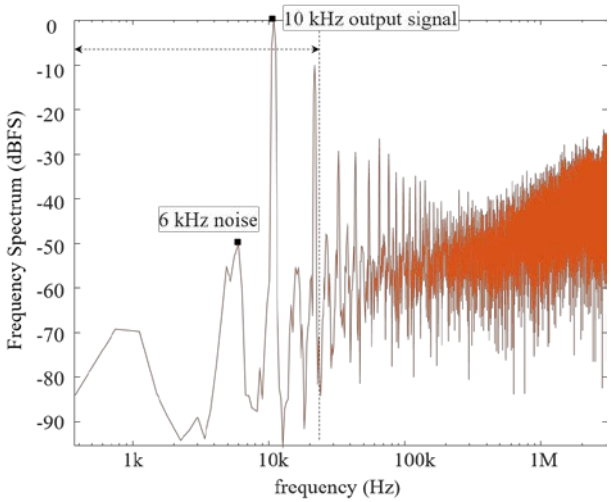

Fig. 8. Simulated frequency spectrum of the designed sigma delta modulator with ground noise

schematics of the designed folded cascode operational amplifier. Table II shows the transistor parameters of the circuit.

E. Design of a comparator

A latched comparator is designed for high-speed operation. An analog input is converted into VDD and GND after being compared to the reference voltage. Fig. 5 shows the schematics of the designed latched comparator. Table III shows the transistor parameters of the circuit.

F. Design of 1-bit digital-to-analog converter

A 1-bit digital-to-analog converter (DAC) converts digital to analog signal and feeds back to the integrator. It has two reference voltages, 1 V and 2.3 V. If the input data is 0, the output becomes 1 V, and if the input data is 1, the output becomes 2.3 V. Fig. 6 shows the schematics of the designed 1-bit DAC. Table IV shows the transistor parameters of the circuit.

III. RESULTS AND DISCUSSIONS

A. Analysis of audio frequency ground noise effect on the first-order discrete-time sigma-delta modulator

After completing the design, the first-order discrete-time sigma-delta modulator is simulated in the time-domain using a Virtuoso Analog Environment Simulator from Cadence. A sinusoidal input signal with a 0.7 V amplitude and a 10 kHz frequency is applied. The simulated time-domain waveform is processed into the frequency domain with FFT. Before the FFT, the waveform is Hanning-windowed to limit the spectrum leakage. The spectrum is scaled to the input signal frequency. The frequency spectrum is shown in Fig. 7. The spectrum shows the baseband noise successfully spread to over-sampled frequency range. The modulator has shown a 55.7 dB SNR. The harmonic components of the output signal is excluded in the calculation of SNR.

To check whether audio frequency ground noise coupling affects the performance of the designed circuit, a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground of the circuit. Fig. 8 shows its frequency spectrum. The modulator has shown a -50 dB 6 kHz noise power.

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B. PCB and Ground Designs for TDMA Smartphones

Fig. 9 shows two PCB designs for audio frequency GI analysis. The designed modulator and a noise source are placed on the PCBs. The ground noise is analyzed in simulation level by using power distribution network model of designed PCBs and circuit models. The noise source is an ideal current source which draws peak-to-peak 3 A of current at 217 Hz. The two PCBs differ the positions of the modulator and the noise source. On the first PCB named CASE A, the components are placed in the order of a noise source, a modulator and a power supply. On second PCB named CASE C, the components are placed in the order of a modulator, a power supply and a noise source. The modulator and noise source are placed radially from the power supply.

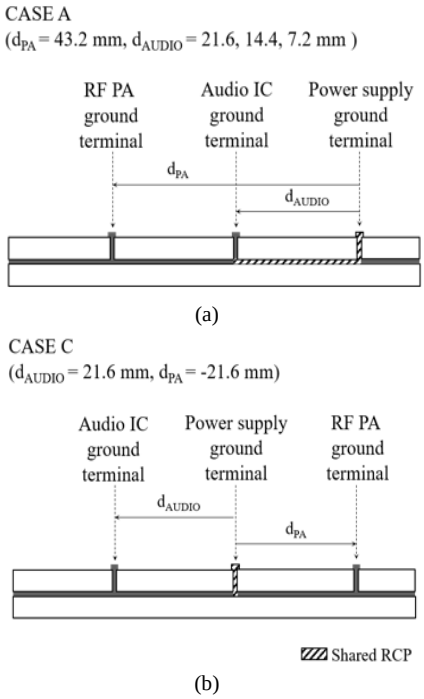

Fig. 9. Two PCB designs for audio frequency GI analysis.

Fig. 10 shows the frequency spectrum of the output of the designed modulators each in PCB CASE A and CASE C. In the ground design of CASE A, the location of the modulator determines the shared RCP as shown in Fig. 9 (a). The length of the shared RCP determines the ground noise coupled at the modulator. In the ground design of CASE C, the modulator and the noise source nearly do not share RCP, and therefore, the ground noise coupled at the modulator is much less than that in the PCB CASE A. Because the ground noise coupled at the modulator of CASE C is smaller than that of CASE A, the output noise of the modulator of CASE C is smaller than that of CASE A as shown in Fig. 10. The modulator of CASE C shows better SNR than CASE A.

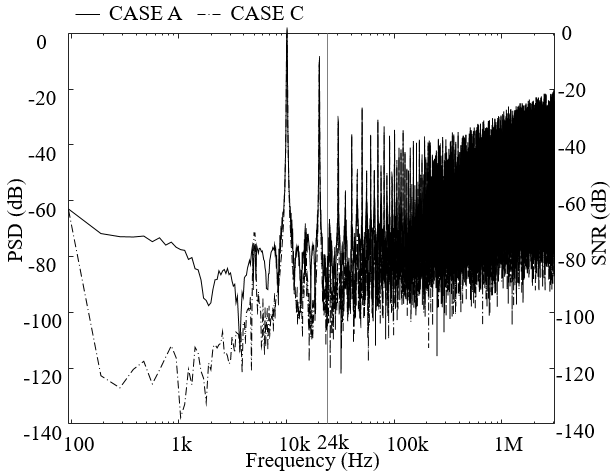

Fig. 10. Two PCB designs for audio frequency GI analysis.

IV. CONCLUSION

In this paper, we designed and simulated a first-order discrete-time sigma-delta modulator circuits with Virtuoso Schematic Editor and Analog Environment Simulator from Cadence to analyze audio frequency ground noise coupling effect on audio. The designed modulator operates at 3.3 V DC power and a 6.144 MHz sampling frequency with a 48 kHz baseband sampling frequency and a 128 over-sampling ratio. The spectrum shows the baseband noise successfully spread to over-sampled frequency range, and the modulator has shown a 55.7 dB SNR. When a sinusoidal ground noise with a 100 mV amplitude and 6 kHz frequency is applied to the ground of the circuit, the modulator has shown a -50 dB 6 kHz noise power. The designed modulator is further analyzed by being simulated with PCB power and ground network model, a supply, and a noise source. The amount of noise coupling reduces as the shared RCP between the modulator and a noise source reduces. The result clearly shows that the grounding structure of a system should be carefully designed to prevent degradation of the audio IC in systems that cause audio-frequency ground noise coupling.

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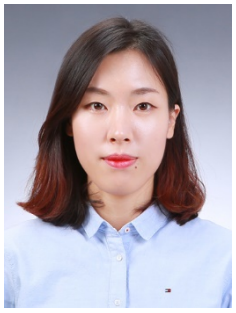

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Since joining KAIST, his research centers on EMC modeling, design, and measurement methodologies of 3D IC, TSV, Interposer, System-in-Package, multi-layer PCB, and wireless power transfer (WPT) technologies. Especially, his major research topic is focused on chip-package-PCB co-design and co-simulation for signal integrity, power integrity, ground integrity, timing integrity, and radiated emission in 3D IC, TSV and Interposer. He has authored and co-authored over 480 technical papers published at refereed journals and conference proceedings. Also, he has given more than 263 invited talks and tutorials at the academia and the related industries.

Recently, he published a book, “Electrical Design of Through Silicon Via”, by Springer in 2014. Dr. Joungho Kim will be Conference chair of IEEE EDAPS 2015 in Seoul, and Joint conference chair of Japan-Korea Microwave society in 2015. He also was the conference chair of IEEE WPTC (Wireless Power Transfer Conference) 2014, held in Jeju Island, Korea. And he was the symposium chair of IEEE EDAPS Symposium 2008, and was the TPC chair of APEMC 2011. He is also an associated editor of the IEEE Transactions of Electromagnetic Compatibility. He served as a guest editor of the special issue in the IEEE Transactions of Electromagnetic Compatibility for PCB level signal integrity, power integrity, and EMI/EMC in 2010, and as a guest editor of the special issue in the IEEE Transactions of Advanced Packaging for TSV (Through-Silicon-Via) in 2011. He served as a guest editor of the mini-special issue in the IEEE Transactions of Microwave Theory and Techniques, for IEEE WPTC in 2015. He received Outstanding Academic Achievement Faculty Award of KAIST in 2006, KAIST Grand Research Award in 2008, National 100 Best Project Award in 2009, KAIST International Collaboration Award in 2010, KAIST Grand Research Award in 2014, and Teaching Award in 2015, respectively. He was appointed as an IEEE EMC society distinguished lecturer in a period from 2009-2011. He received Technology Achievement Award from IEEE Electromagnetic Society in 2010. He is IEEE fellow.