A Random and Systematic Jitter Suppressed DLL-Based Clock Generator with Effective Negative Feedback Loop

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***Abstract* - A random and systematic jitter suppressed delay locked loop (DLL)-based clock generator with an averaging circuit (AC) and an effectively negative feedback functioned capacitor is presented. The AC averages the delay time of successive delay stages and equalizes the delay time of all delay stages. In addition, a capacitor with a switch working effectively as a negative feedback function is introduced to reduce the variation of the loop filter output voltage. Measurement results of the DLL-based clock generator fabricated in a one-poly six-metal 0.18μm CMOS process shows 13.4-ps rms jitter.**

I. INTRODUCTION

DLL and phase locked loops (PLL's) have been typically employed for the generation of on-chip clock signals. While the phase error of PLL's is accumulated and persists for a long time in noisy environment, that of DLL's is not accumulated, and thus, the clock signal generated form of DLL's has lower jitter. Therefore, DLLs are often used in clock multiplication where lower jitter characteristic is required. Recently, greater emphasis is being placed on suppressing jitter in clock signals as the speed of modern chips rapidly increases.

The combination of a PLL with a recirculating DLL is used to generate a high frequency and low jitter clock signal but it requires a clean reference signal and complicated circuits [1]. A DLL with a divider and a VCO-like VCDL is used for frequency multiplication. The VCDL includes a MUX which selects the reference signal or the VCDL output signal [2]. A DLL does not accumulate noise over many cycles in the voltage controlled delay line (VCDL). It combines equally spaced edges from delay cells in the VCDL to generate a high frequency clock signal. These equally spaced edges are combined to generate the desired high frequency clock signal. Various techniques are used to generate a higher frequency clock signal without controlling the timing uncertainty of edges caused by delay stages in VCDL [3]-[6]. Timing uncertainty of the edges due to random and systematic variations among the delay stages in the VCDL causes a larger jitter.

To suppress the jitter caused by random and systematic variations among the delay stages in the VCDL, several techniques have been published. Phase averaging and interpolation by using resistor arrays has been proposed to suppress the timing uncertainty of delay stages but it requires a large area for process sensitive resistor arrays [7]. A digital DLL using the closet edge selection method has also been proposed to suppress the timing uncertainty [8]. The timing uncertainty among delay stages is compared by using multiple phase detectors to suppress timing uncertainty [9]. Phase detectors that consist of capacitors which are sensitive to process variations may generate variation among their output. A self-calibration method utilizing a delay calibration buffer and a timing error comparator is used to reduce the timing uncertainty [10]. The current mismatch of the timing error comparator can cause the systematic timing uncertainty. Additional negative feedback loops for each delay cell in the VCDL are introduced to suppress systematic delay mismatches of every delay stage [11]. In [11], a delay variance voltage converter (DVVC) is applied to the jitter caused by random variation among the delay stages in the VCDL but it cannot suppress systemic variation among the delay stages in the VCDL.

In this paper, an average circuit (AC) is introduced in [11] to suppress the systematic and random jitter among the delay stage in the VCDL. Moreover, a capacitor with a switch working effectively as a negative feedback function is introduced to the loop filter for further suppressing jitter. It has been implemented in a 0.18μm CMOS process to verify the proposed DLL-based clock generator with DVVC and AC.

The rest of the paper is organized into six parts where Section II discusses the architecture of the DLL. Section III analyzes the proposed loop filter. Section IV presents the circuits used in the DLL. Section V demonstrates the measurement result, and finally Section VI provides some conclusions.

II. ARCHITECTURE OF THE DLL WITH AVERAGING CIRCUIT

The architecture of the DLL-based clock generator with an AC is shown in Fig. 1. It consists of a phase detector (PD), a charge pump (CP), a loop filter (LF) which is made of a

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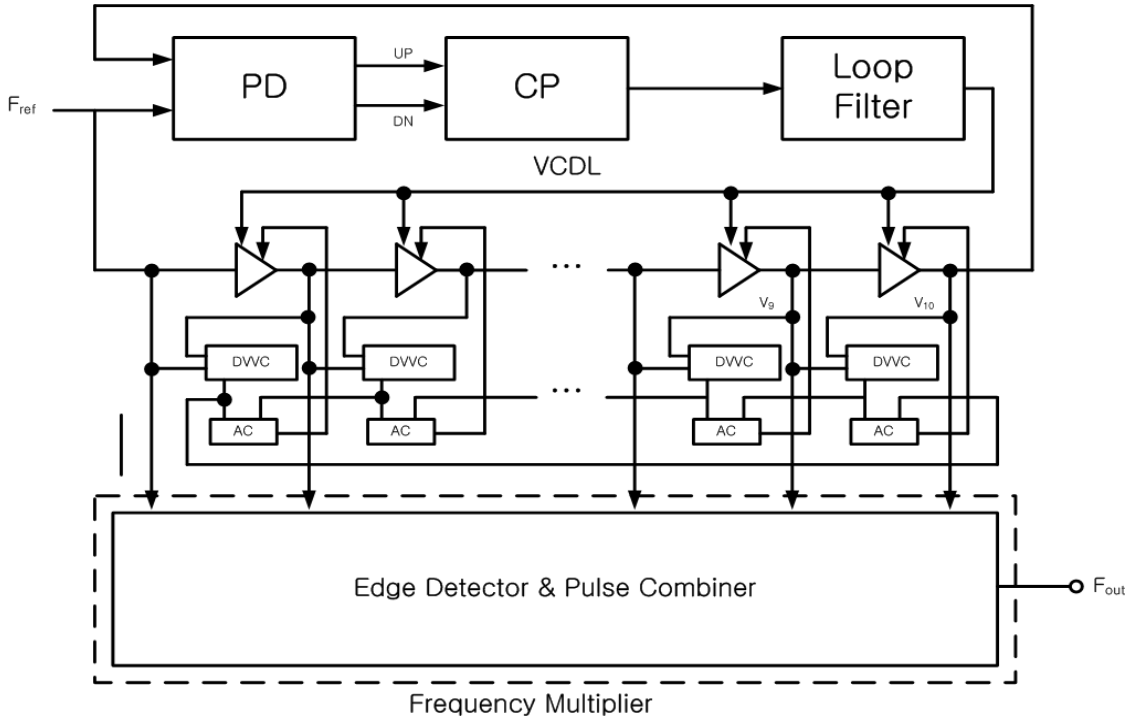


Fig. 1. Block diagram of the proposed DLL-based clock generator.

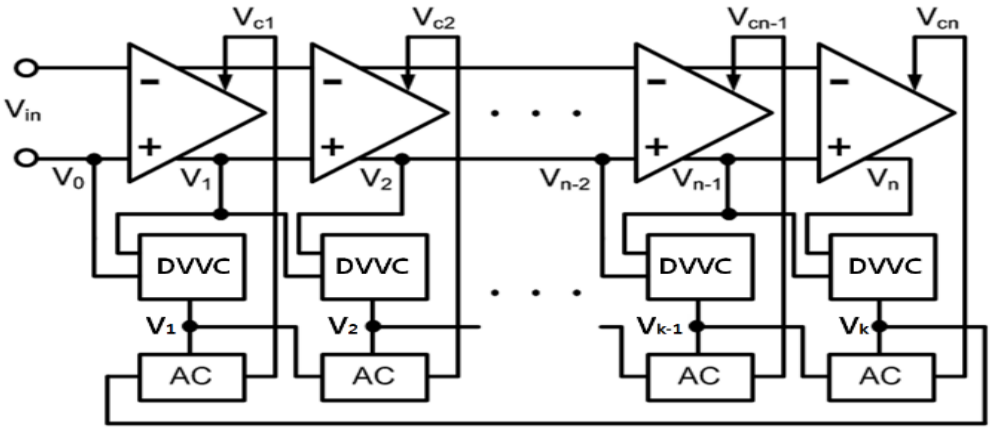


Fig. 2. Block diagram of the proposed VCDL. The VCDL is negative feedback looped with a DVVC and an AC.

capacitor with a switch working effectively as a negative feedback function, a voltage controlled delay line (VCDL), a delay variance voltage converter (DVVC), an averaging circuit (AC), and a frequency multiplier (FM). The DVVC, the AC and the single capacitor LF with a switch are introduced to a conventional DLL to suppress the systematic and random jitter. The VCDL in Fig. 2 is made of ten differential delay stages. The delay stage is negative feedback looped with an AC and has two input signals from LF and AC. V_n, V_k and V_{cn} are the output signals of VCDL, DVVC and AC, respectively.

The blocks of PD, CP, LF and VCDL consist of the main negative feedback loop. The output voltage of the LF is from the main negative feedback loop and is used to control the delay time of the whole VCDL. The additional negative feedback loop consists of one delay stage in the VCDL and AC. The DVVC monitors the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the systematic and random delay variance of each delay stage in the VCDL.

The AC and DVVC in Fig. 3 (a) and (b) are used to eliminate the delay variance of each delay stage in the VCDL. The non-overlapped control signals, $\Phi_{m.1}$, $\Phi_{m.2}$ and $\Phi_{m.3}$, in Fig. 3 (a) and (b) are generated by using the control signal generator in Fig. 3 (c). The AND gate in the DVVC generates a signal, V_m, using the output signals of delay stages, V_{n-1} and V_n, as the input signals as shown in Fig. 3 (a). The signal, V_m, charges the capacitor, C_x, by turning on the PMOS in DVVC. The charge of C_x is transferred to C_y by the signal, $\Phi_{m.1}$. In the ideal condition of zero delay variance, the output voltage of DVVC is always constant. The charge of C_y is transferred to C_z at the AC by signals, $\Phi_{m.2}$ and $\Phi_{m+1.2}$, and C_x is discharged by signal, $\Phi_{m.3}$.

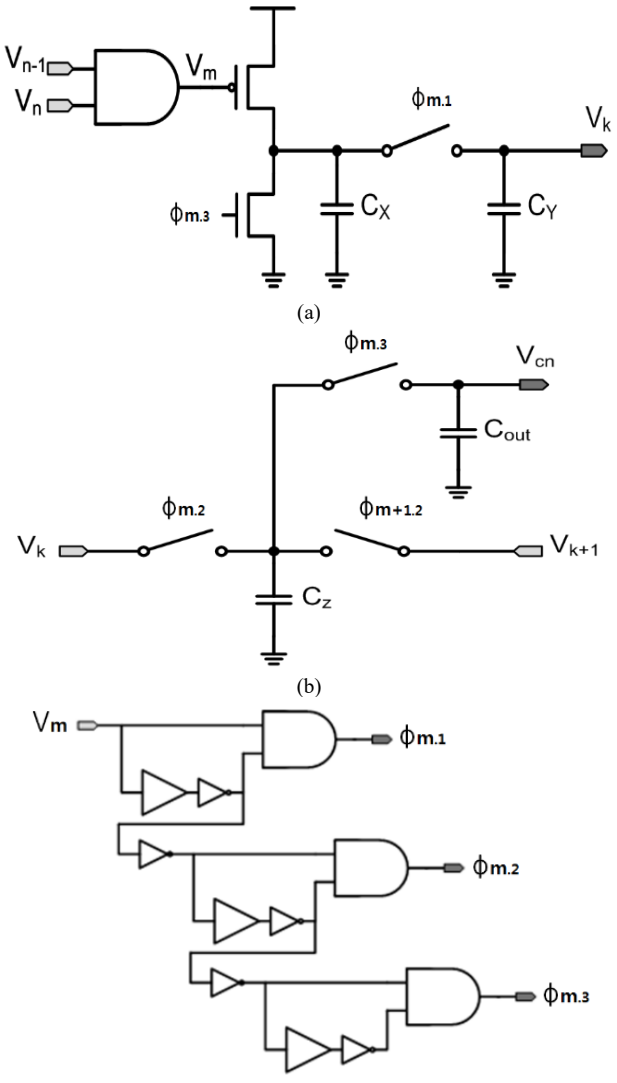
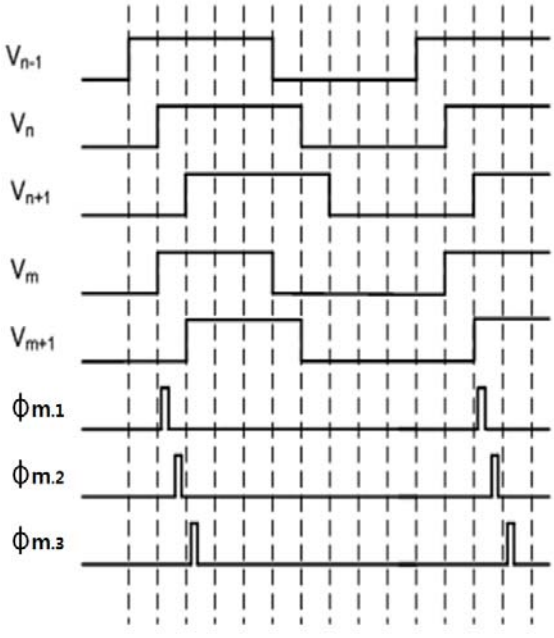
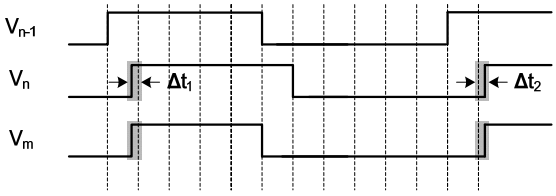


Fig. 3. (a) Delay-variance voltage convertor circuit, (b) Averaging circuit, (c) Control signal generator.



(a)



(b)

Fig. 4. (a) Control signal timing, (b) Timing of input-output signals of DVVC at delay mismatch.

Both random and systematic delay variance occurs among the delay stages in the VCDL. When two signals, Vn-1 and Vn, are applied to the AND gate in the DVVC, and if there is delay variance, Δt1, as shown in Fig. 4 (b), the "Low" period of Vm shortens as much Δt1 resulting in a lower output voltage from the DVVC, Vk, because of the shortened turn on time of the PMOS. Alternatively, if there is delay variance, Δt2, as shown in Fig. 4 (b), then the "Low" period of Vm lengthens as much as Δt2 resulting in higher output voltage from the DVVC, Vk, because of the lengthened turn on time of the PMOS.

The AC consists of capacitors as shown in Fig. 3 (b). The signals, Vk and Vk+1, are generated from the DVVC with the signals, Vn-1 and Vn, and Vn and Vn+1, respectively. These two signals, Vk and Vk+1, are applied to the input of AC at Φ m.2 and Φ m+1.2 as shown in Fig. 3 (b). The magnitude of Vk and Vk+1 represents the delay time of the delay stages in the VCDL. The averaged charge of Cz transfers to Cout at Φm.3 and generates Vcn which controls the delay time of the delay stages in the VCDL. Eventually, the AC equalizes the delay time of the delay stages in the VCDL.

Whenever there are delay time variances due to the systematic and/or random causes among the delay stages in the VCDL, the negative feedback function of the DVVC and AC makes the delay time of the delay stages in the VCDL as follows

$$t_1 = t_2$$

$$t_2 = t_3$$

$$t_{n-1} = t_n \qquad (1)$$

where t_n is the delay time of the n_{th} delay stage of the VCDL.

If the delay time of the n_{th} delay stage increases such as for Δt_2 in Fig. 4 (b), the output voltage of the n_{th} AC increases and the output signal of the VCDL leads the reference signal. Two things happen simultaneously. The main negative feedback loop of the DLL generates a signal to compensate for the delay difference between the reference signal and the output signal of VCDL while the AC eliminates Δt_n and the sum of all delay times for each delay stages in the VCDL equals T_{ref} as follows

$$T_{ref} = (t_1 + \Delta t_1) + (t_2 + \Delta t_2) + \cdots + (t_{n-1} + \Delta t_{n-1}) + (t_n + \Delta t_n) \qquad (2)$$

where T_{ref} and Δt_n are the period of the reference signal and the delay time variance of delay stages in the VCDL, respectively. The negative feedback loop of the PD, CP, LF and VCDL and the additional negative feedback loop of the DVVC, AC and VCDL result in suppressing the jitter of the clock signal generated by the proposed DLL.

III. ANALYSIS OF THE EFFECTIVE NEGATIVE FEEDBACK LOOP IN LOOP FILTER

A DLL is a delay control system that uses a negative feedback loop. As the main block, VCDL is controlled by the control voltage in loop filter, V_{LPF}. The wave form of V_{LPF} is the most essential index to estimate the jitter characteristic in the DLL. As a result, transforming the loop filter structure can suppress jitter further. The voltage wave forms in a conventional and proposed loop filter are shown in Fig 5. A conventional loop filter is shown in Fig. 5 (a). This structure has just one pole at the origin.

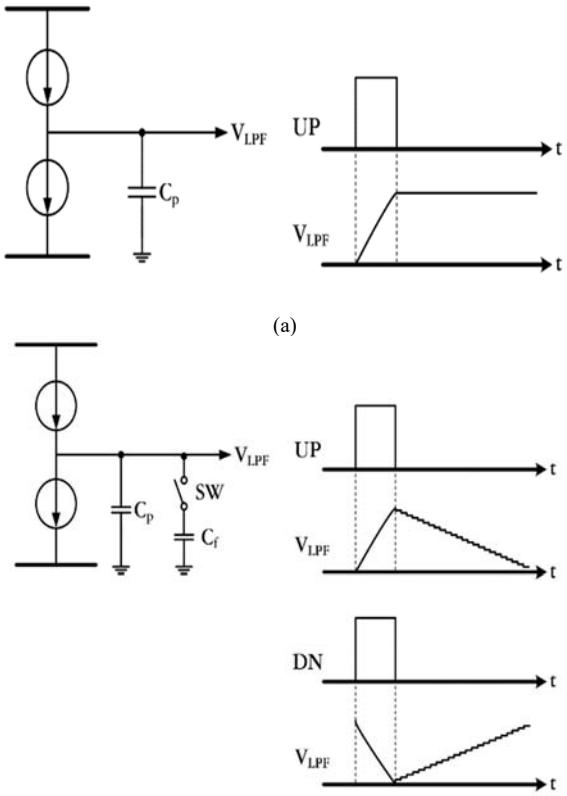


Fig. 5. (a) Conventional single capacitor LF,
(b) Single capacitor and a capacitor (Cf) with a switch working effectively as negative feedback function.

In Fig. 5 (b), a switch with a capacitor is introduced to reduce the fluctuation of the loop filter output voltage. The switch control circuit which is not shown in Fig. 1 and its timing are shown in Fig. 6. The switch is operated by the high frequency DLL output signal as shown in Fig. 6 (a) and is "off" while UP/DN pulse presents as shown in Fig. 6 (b). The output voltage of the loop filter increases/decreases during the UP/DN pulse, and after the UP/DN pulse the output voltage is decreased/increased by the added switch and capacitor.

Thus, the added switch and capacitor performs a negative feedback function for the loop filter. To be specific, when the switch is turned on during the previous reference periods, the final value of V_{LPF} is stored in C_f. For example, if the last voltage of C_f is lower than the present voltage of C_p after the UP signal, the charge on C_p transfers to C_f at F_{out} and the output voltage of LF decreases as shown in Fig. 5 (b). Also, if the last voltage of C_f is higher than the present voltage of C_p after the DN signal, the charge on C_f transfers to C_p at F_{out} and the output voltage of LF increases as shown in Fig. 5 (b).

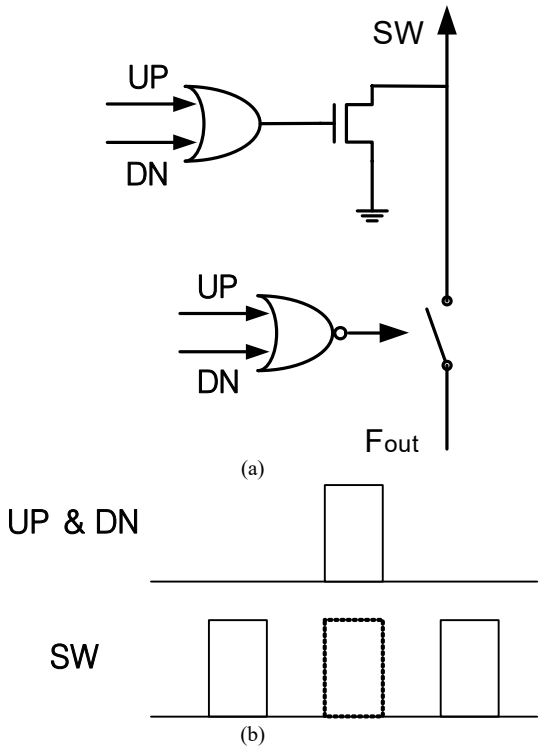
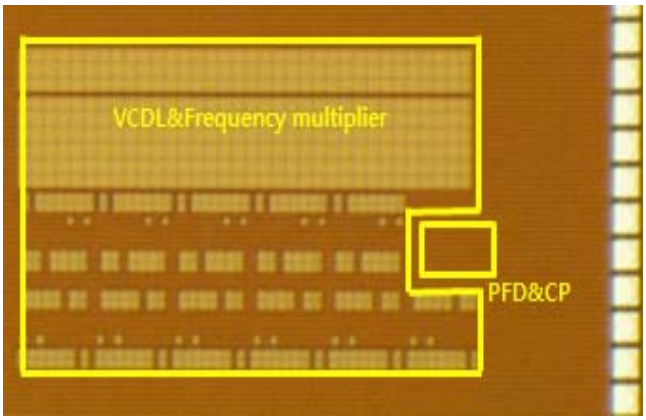


Fig. 6. (a) Control signal generator for switch in LF, (b) Timing of signals.

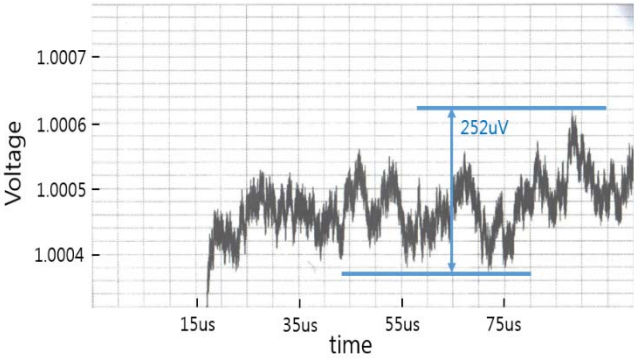
Excessive delay shift during a reference signal period is minimized and resulted in jitter reduction. That is a negative feedback function which reduces the variation of V_{LPF}, caused by the UP/DN pulse as shown in Fig. 5 (b) [12]. In [12], it shows the reduction of V_{LPF} variation which can result in a jitter characteristic improvement. The VCDL and the frequency multiplier in [11] are used.



(a)

(b)

Fig. 7. (a) Chip photograph, (b) Layout of DLL.



(a)

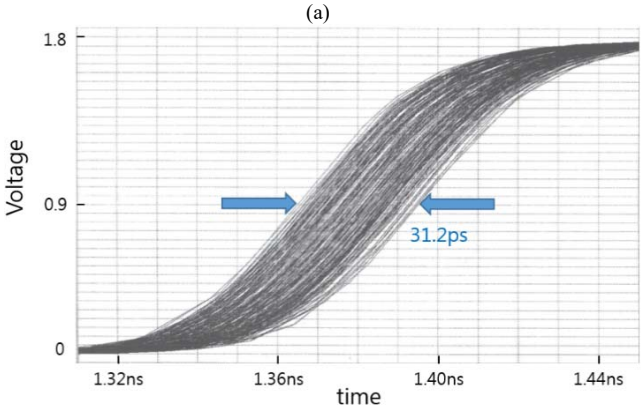


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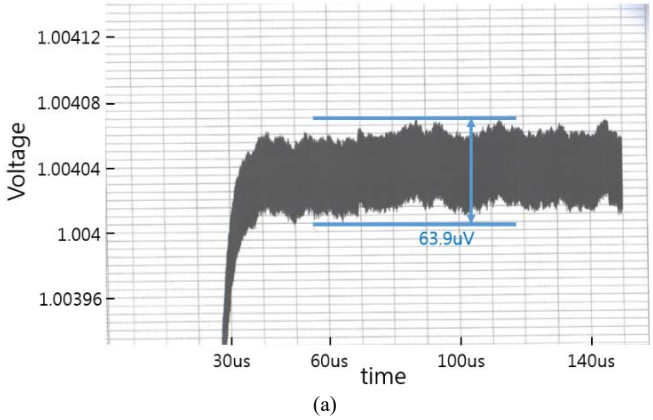
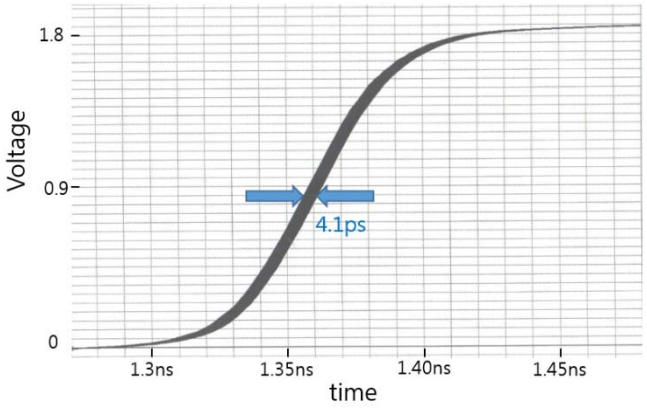
Fig. 8. Simulation results of (a) output voltage variation of loop filter, (b) jitter characteristic of the conventional DLL.



(a)



(b)

Fig. 9. Simulation results of (a) output voltage variation of loop filter, (b) jitter characteristic of the proposed DLL.

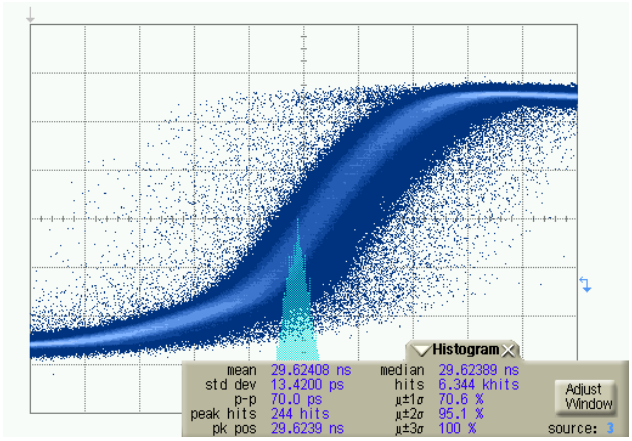


Fig. 10. Measurement results of jitter characteristic of the conventional DLL at 500MHz.

IV. MEASUREMENT RESULTS

The proposed DLL was implemented using a one-poly six-metal 0.18μm CMOS process. The chip photographs, layouts are shown in Fig. 7. The lower layers of transistors and capacitors are not seen because of the thick multi-inter-metal layers. The die area is 1110 μm * 730 μm in Fig. 7 without LF capacitors.

The simulation results of loop filter output voltage variation are shown in Fig. 8 (a) and Fig. 9 (a). In the simulation results as shown in Fig. 8 (b) and Fig. 9 (b), the jitters of DLL without and with DVVC and AC are approximately 31.2ps and 4.1ps, respectively. The simulation results show that the jitter of the proposed DLL is approximately 20% less than that of the DLL with DVVC alone in [11]. The jitter characteristic deteriorated by the systematic mismatches among VCDL delay cells can be further improved by the additional AC circuits.

The measured multiplied output clock signal has 13.4-ps rms jitter as shown in Fig. 10. In this paper, although the DLL uses a VCDL with additional AC circuits compared with that of [11], the measured result of the jitter characteristic is not superior to that of the DLL in [11]. The added AC circuits may introduce jitter degradation in view of a process variation and a layout. The additional AC circuits make the size of the proposed DLL two times bigger

than the DLL in [11]. All signal paths in the ACs and DVVCs block inevitably have different individual parasitic capacitance, and thereby each path has a different delay time. Therefore, it is presumed that the complicated circuit related layout of DVVCs and ACs in the VCDL causes jitter degradation.

V. CONCLUSION

This paper suggests that using a DLL-based clock generator with an AC in the VCDL can suppress both random and systematic jitter. The DVVCs and ACs form a negative feedback loop in the VCDL. The DVVC senses the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the random and systematic delay variance of each delay stage in the VCDL. In addition, the loop filter comprising a capacitor and a capacitor with switch working effectively as a negative feedback function is introduced to reduce the fluctuation of loop filter output voltage. However, the fabricated DLL does not show results as expected by simulation due to the complicated circuit and its related layout.

ACKNOWLEDGEMENT

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