Two-negative feedback loop PLL with frequency voltage converter loop

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***Abstract* - To reduce the phase noise and jitter of the conventional PLL, the proposed PLL uses frequency voltage converter (FVC). The inner negative feedback loop consisting of a voltage controlled oscillator (VCO) and a frequency voltage converter is nested inside a conventional outer PLL loop. When the output voltage (VCO input voltage) of the loop filter changes, the output voltage of the FVC changes in the opposite direction at a much higher sampling frequency in the negative feedback looped VCO. Thus, whenever the VCO output frequency varies, the FVC works as a compensator and it results in VCO noise reduction. It improves the phase noise characteristic and the stability of PLL. It has been simulated and proved by HSPICE in a CMOS 0.18µm 1.8V process. Measurement result of the two-negative feedback loop PLL fabricated in a one-poly six-metal 0.18µm CMOS process shows approximately 20dB improvement at 1MHz offset from 1GHz carrier frequency.**

***Keywords*—Frequency-to-voltage Converter, Phase Locked Loop, Phase Noise**

I. INTRODUCTION

Phase Locked Loop (PLL) is a core component included in next-generation communication systems and digital chips because it is used as a frequency synthesizer in wireless communication and clock signal generators in digital chips that operate at high speed. The carrier frequency of next-generation mobile communications is increasing to transport a lot of data in a short time, and the operating speed of semi-conductor chips is also increasing. Therefore, the new frequency synthesizer should have better phase noise characteristics and the clock signal generator should have very small jitter.

Typically, a PLL consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a divider [1].]. A PLL is usually the third-order closed loop system that includes the second-order LF which consists of two capacitors and one resistor. It has one low frequency zero, and three poles consisting of two poles at origin and one pole at high frequency. In general, a narrow bandwidth has an advantage for suppressing phase noise and spur, but it needs a low phase noise VCO and takes a long locking time. A higher frequency pole can be introduced to suppress phase noise further. Careful design of poles and zero location is required to ensure a stable operation of PLL. The design of PFD and CP should deal with linearity, dead zone, current mismatch, timing mismatch in two output signals of PFD, charge sharing and injection, because these performances degrade the phase noise characteristics of PLLs. LC-VCO is preferable to ring VCO for low phase noise PLL because of its better phase noise performance [2].

Various architectures of PLLs and DLLs have been proposed to improve phase noise and jitter characteristics. The optimal loop-bandwidth has been derived from a discrete-time PLL model to find a loop-bandwidth which shows a good jitter performance [3]. Jitter optimization using PLL design parameters has been derived [4]. These theories are helpful in the design of PLL, but their effect on fabricated PLLs is not great because they are susceptible to process variations. A VCO realignment method has been introduced to reduce accumulated jitter in VCO periodically [5]. The accurate timing of realignment is not easy to implement in a PLL even though it has a maximum of 10dB improvement in phase noise performance. Sub-sampling phase detector has been used to improve phase noise and spur characteristics [6] [7]. PD/CP noise is not multiplied by N^2 in the sub-sampling scheme but the VCO noise which is usually the largest in PLL cannot be suppressed. Various architectures of DLL-based clock generator or frequency synthesizer have been proposed to improve the phase noise and jitter characteristics of PLL [8]-[10]. The frequency synthesizer in [8] multiplies reference frequency by a fixed multiplication factor. The clock generator in [9] can generate a wide range of clock signals by a fixed multiple multiplication factor. A clock multiplier combines a PLL and a recirculating DLL which has low phase noise characteristic [10]. These DLL-based frequency synthesizers or clock generators have difficulty in generating multiple narrowly spaced channel frequencies. Various PLLs with this structure have been published. However, this structure still has an issue of how to accurately deliver periodical input signals to VCO.

Previously published PLL structures have one negative feedback loop. To overcome the characteristic limits of one

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negative feedback loop PLL, a new scheme is required. Therefore, the new architecture of PLL with two negative feedback loop will be studied [11]. It can be applied to design a frequency synthesizer with an outstanding phase noise characteristics to be used in next-generation mobile communication systems and a clock signal generator with very small jitter to be used in high-speed chips.

II. PROPOSED PLL

A phase locked loop is a circuit that usually produces a high frequency signal. The most commonly used PLL architecture is shown in Fig. 1.

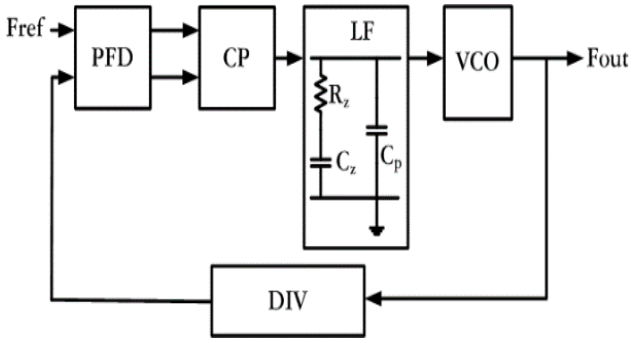


Fig. 1. Conventional PLL

The PLL consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider (N).

In conventional PLL, a PFD compares the phase and frequency of a signal generated by a VCO with a reference frequency (F_{ref}) signal input from the outside, and generates signals corresponding to the difference in phase and frequency to drive CP. The CP charges or discharges a LF which generates a signal to drive a VCO, consequently the VCO generates the output signal (F_{out}), PLL out signal.

In a PLL with a narrow bandwidth, it is not easy to reduce the phase noise of the VCO. Otherwise, widening the bandwidth to reduce the phase noise of the VCO makes it difficult to reduce the phase noise of other parts. In order to overcome the limit of a conventional PLL, the proposed PLL uses a frequency-to-voltage converter (FVC) to reduce the phase noise of the VCO. The FVC is a circuit that inputs the output signal of the VCO and generates a voltage according to the frequency. The FVC which is connected to the VCO in negative feedback loop operates to reduce jitter and phase noise.

Fig. 2 is a block diagram of the proposed two-negative feedback loop PLL. An FVC is added to the conventional PLL. The PLL with FVCs has a different bandwidth which reduces the VCO's phase noise.

Fig. 3 shows the transfer function of the proposed PLL. The characteristics of PFD, CP, LF, VCO, FVC, and divider are shown using s-parameters, and the characteristic of FVC is added in the transfer function of general PLL. Here, the PLL LPF (LPF_E (s)) the FVC filter (LPF_I (s)) are implemented with two capacitors and a resistor, and one capacitor, respectively.

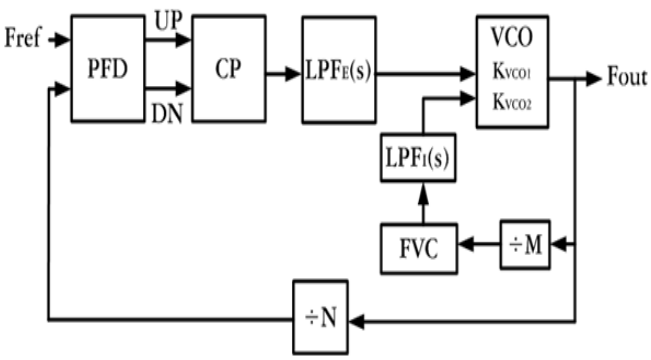


Fig. 2. Proposed two-negative feedback loop PLL

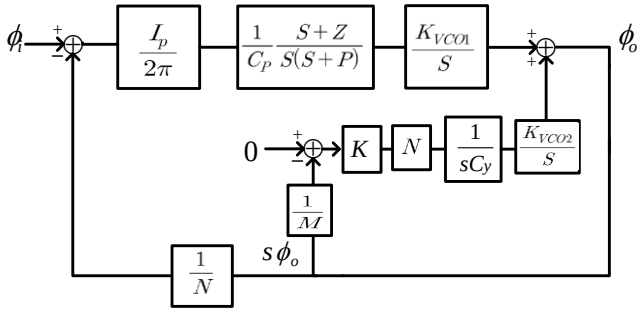


Fig. 3. Transfer function of proposed PLL

The signal output from the overall signal can be expressed by the following equation.

$$\phi_o = (\phi_i - \frac{\phi_o}{N})\frac{Ip}{2\pi}\frac{1}{cp}\frac{s+z}{s(s+p)}\frac{k_{vco1}}{s} + (-s\phi_o)K\frac{1}{sc_y}\frac{k_{vco2}}{s} \quad (1)$$

The closed and open loop transfer function is as follows

$$\frac{\phi_o}{\phi_i} = \frac{\frac{Ip}{2\pi}\frac{1}{cp}\frac{s+z}{s(s+p)}\frac{k_{vco1}}{s}}{1+\frac{1}{N}\frac{Ip}{2\pi}\frac{1}{cp}\frac{s+z}{s(s+p)}\frac{k_{vco1}}{s}+K\frac{1}{sc_y}\frac{k_{vco2}}{s}} \quad (2)$$

$$T_{op} = \frac{1}{N}\frac{Ip}{2\pi}\frac{1}{cp}\frac{s+z}{s(s+p)}\frac{k_{vco1}}{s}+K\frac{1}{sc_y}\frac{k_{vco2}}{s} \quad (3)$$

Where K, K_{VCO2} and C_y are FVC transfer function, VCO gain for FVC loop and FVC loop filter.

K, K_{VCO2}, and C_y are introduced by the FVC in the conventional transfer function. Adding the FVC circuit reduces the bandwidth in the entire closed loop transfer function and can reduce the jitter of the entire PLL as shown in Fig. 4. There is no requirement on the ratio between K_{VCO1} and K_{VCO2} because both loops work as complementary.

Fig. 5 (a) shows the VCO circuit as a ring oscillator. Fig. 5 (b) shows the CMOS circuit inside the VCO delay cell. Gain of K_{VCO1} and K_{VCO2} is generated by receiving the voltage of LF and the voltage of FVC. Fig. 6 (a) shows the FVC circuit, in which the Φ_1 and Φ_2 signals are generated by the VCO output signal as shown in Fig. 6 (b). Fig. 6 (c) shows the signal waveforms of Φ_1 and Φ_2.

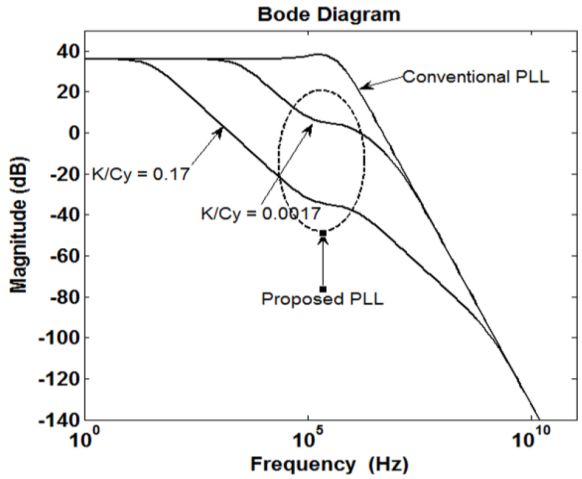
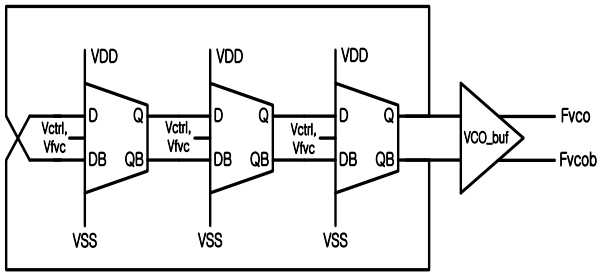
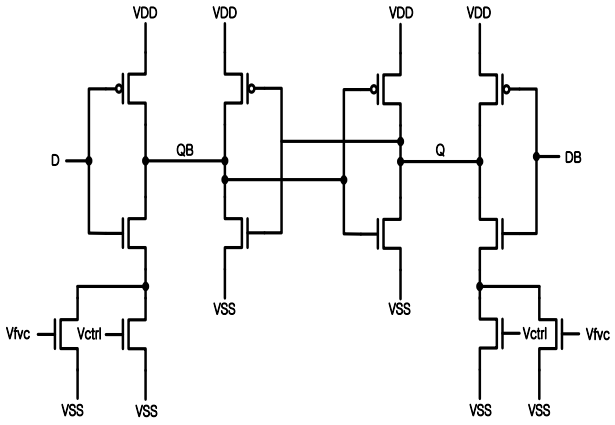


Fig. 4. Bode diagram of conventional and proposed PLL

In a conventional second-order loop filter except the FVC shown in Fig. 7 (a), the two terms of proportional and integral control signals in V_{LF} are produced by a resistor and two capacitors as shown in V_{LF} of Fig. 7 (c), respectively. Fig. 7. (b) demonstrates the conceptual block diagram of the proposed two-negative-feedback-loop PLL. When a PFD detects a phase error, it asserts UP or DN outputs in a way that their net pulse width is proportional to the error. As these PFD outputs control the activation of the up and down currents of the CP, most of the current fed into the C_p would be proportional to the phase error. This current gives rise to a voltage ($V_{proportional}$) across the capacitor, C_p, of which net contribution to the VCO phase is proportional to the present phase error. After UP/DN output, the charge stored in C_p moves to C_z. This current gives rise to a voltage ($V_{intergral}$) across the capacitor, C_z, which is equal to the integral of all the current fed to the filter, hence the sum of the phase errors. The sum of $V_{proportional}$ and $V_{intergral}$ determines the VCO frequency and phase as shown in V_{LF} of Fig. 7 (c). FVC decreases/increases the input voltage of the VCO more abruptly. During the UP pulse, a CP dumps the error charge to a capacitor C_p, giving rise to a voltage equal to $V_{proportional}$ + $V_{intergral}$ as shown in V_{LF} + V_{FVC} of Fig. 7 (c). It increases the VCO frequency and then the output voltage of FVC begins to decrease, leaving only $V_{intergral}$ on the VCO. The shaded area of the effective input voltage, V_{LF} + V_{FVC}, becomes smaller than that of V_{LF} of a conventional second-order LF as shown in Fig. 7 (c). It means that the sum of phase error becomes smaller and the PLL becomes more stable. Therefore, the FVC works as a noise suppressor and stability enhancer.

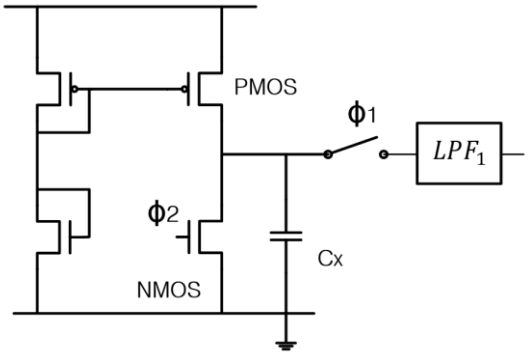


(a)

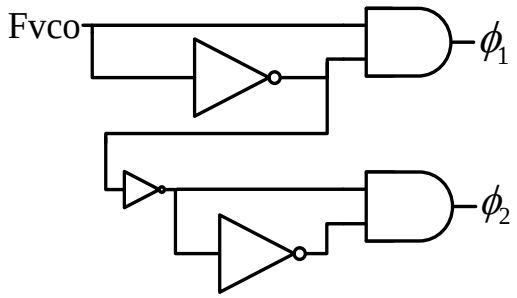


(b)

Fig. 5. Voltage controlled oscillator (a) block (c) delay cell circuit



(a)



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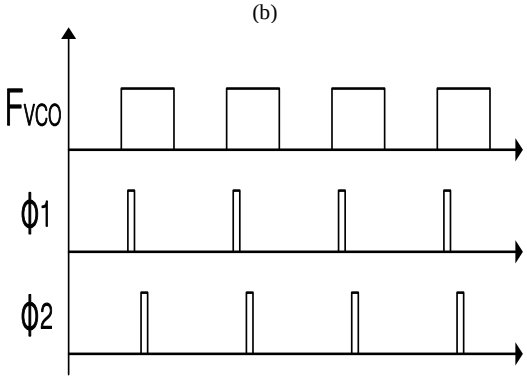


(c)

Fig. 6. Frequency to voltage converter (a) circuit (b) control signal block (c) control signal timing

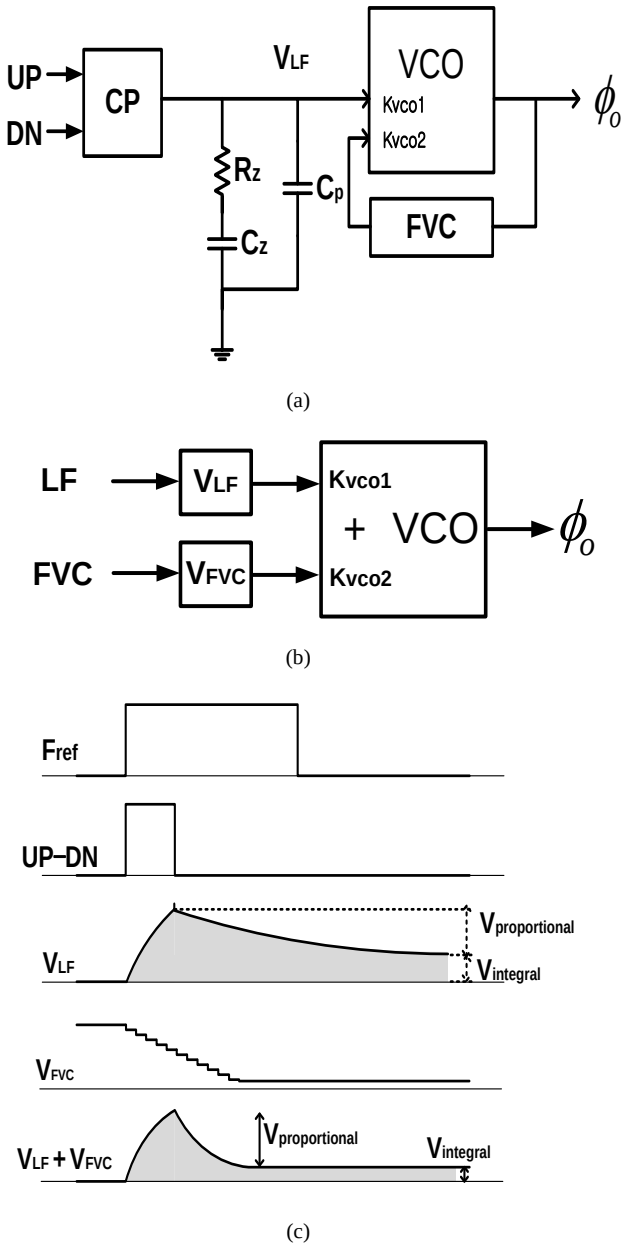


Fig. 7. (a) Second-order loop filter with the inner negative feedback loop consists of a VCO and an FVC. (b) Conceptual block diagram. (c) Output signals of LF and FVC and an effective VCO input voltage of $V_{LF} + V_{FVC}$.

III. SIMULATION AND MEASUREMENT RESULT

The proposed two-negative feedback loop PLL was simulated with HSPICE by using the 0.18μm CMOS process variable. The input frequency is 31.25 MHz. The ratio of divider is 32. Output frequency is set at 1GHz and current of CP is 300μA and gain of VCO is 850MHz/V. The parameters used for the loop filter are R_z = 2 KΩ, C_z = 200 pF, C_p = 20 pF.

Figure 9 shows the simulation results of the conventional PLL. ΔV_{LF} is the magnitude of loop filter voltage fluctuation after lock and determines phase noise characteristic. $\Delta\Delta V_{LPF}$ is the magnitude of loop filter voltage fluctuation generated during one reference signal period after lock and determines spur performance.

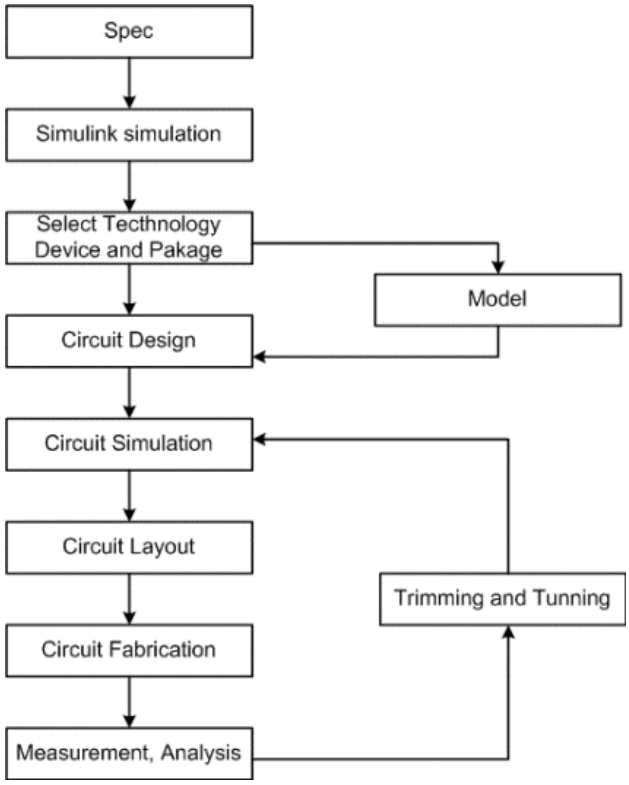


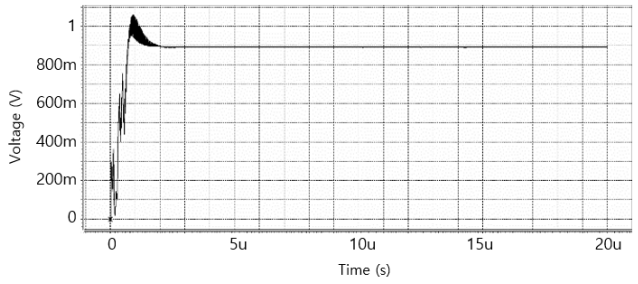
Fig. 8. Design flow

Fig. 8 shows the design flow for designing the proposed two-negative feedback loop PLL.

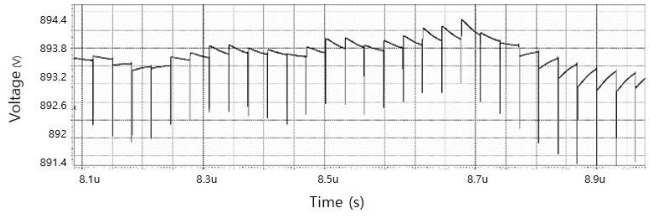
Fig. 9 (a) shows that the phase is locked at 3μs. Fig. 9 (b) shows $\Delta\Delta V_{LF}$ which determines the excess phase shift. It has a value of approximately 220 μV. Fig. 9 (c) shows the jitter (rms) of 1.066ps. The VCO gain of the proposed PLL is 850/550 MHz/V, and the values used for CP current and loop filter are same. The current of FVC is 185μA and the capacitors C_x and C_y are 10pF, respectively.

Fig. 10 shows the simulation results of the proposed two-negative feedback loop PLL. In Fig. 10 (a), we can see the loop filter voltage and the FVC voltage waveform. It is locked at 5μs. The inner loop of FVC makes the proposed PLL more stable and it does not increase locking time. Fig. 10 (b) shows $\Delta\Delta V_{LF}$ $\Delta\Delta V_{FVC}$. Even if the $\Delta\Delta V_{LPF}$ has 345μV, the actual effective voltage is lower than that of the conventional due to $\Delta\Delta V_{FVC}$ which is the voltage subtracted through FVC. Therefore, as shown in Fig. 10 (c), the jitter (rms) shows the jitter of 286.28fs which much lower than that of conventional PLL. Table 1 and 2 show the simulation results of the conventional PLL and the proposed two-negative feedback loop PLL, respectively.

Fig. 11 shows the top layout of the conventional and proposed two-negative feedback loop PLL using the Magna/Hynix 180nm process, where all parameters are same as pre-simulation. Overall size of proposed PLL is 650μm x 430 μm = 0.278mm^2 with 1 poly 6 metal standard CMOS process.



(a)



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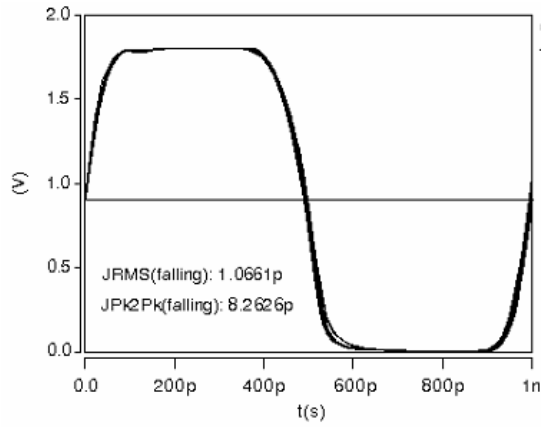
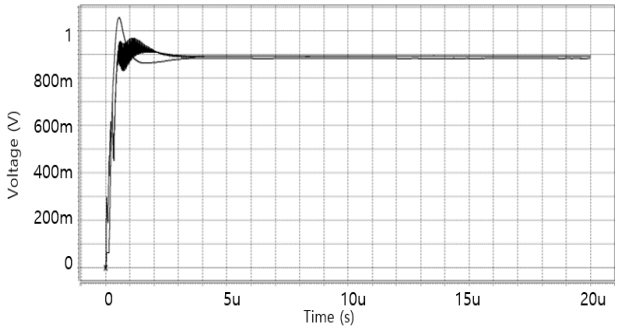


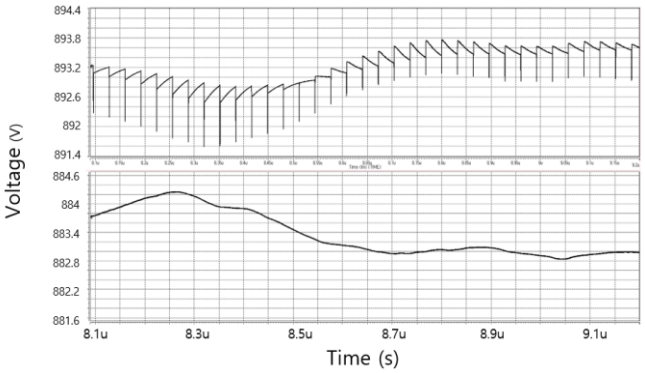
(c)

Fig. 9. Conventional PLL (a) V_{LF} (b) enlarged V_{LF} (c) jitter

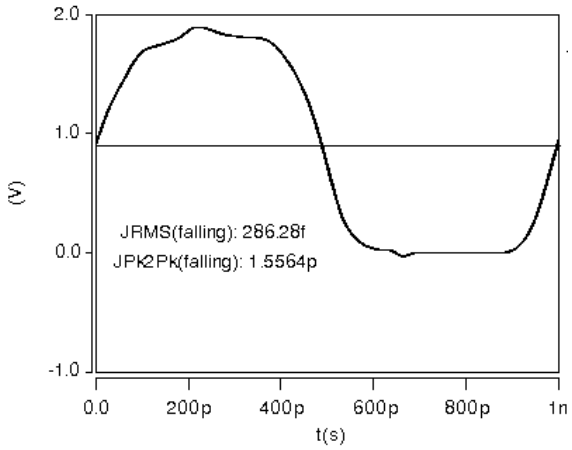


(a)

Fig. 12 shows the measurement results of the conventional and proposed two-negative feedback loop PLL. It shows approximately 20dB improvement at 1MHz offset from 1GHz carrier frequency. The reference spur shows no improvement.



(b)



(c)

Fig. 10. Proposed PLL (a) V_{LF} *and* V_{FVC} (b) enlarged V_{LF} *and* V_{FVC} (c) jitter

TABLE I.
Simulation results of Conventional PLL

Parameter name	Measurement result
Lock time	3μs
ΔV_{LF}	2.06mV
$\Delta\Delta V_{LF}$	220μV
Jitter (rms)	1.067ps

TABLE Ⅱ.
Simulation results of Proposed PLL

Parameter name	Measurement result
FVC current	185μA
Lock time	5μs
ΔV_{LF}	2.56mV
$\Delta\Delta V_{LF}$	345μV
ΔV_{FVC}	2.09mV
Jitter (rms)	286.28fs

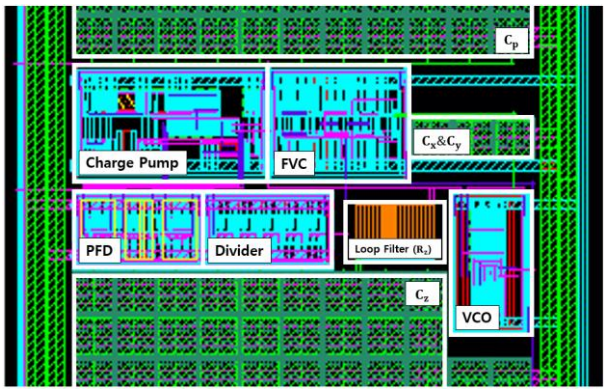
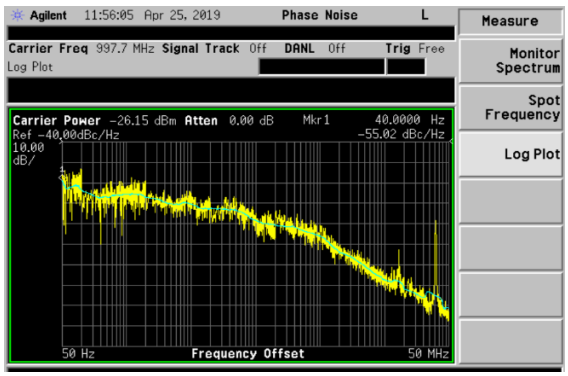


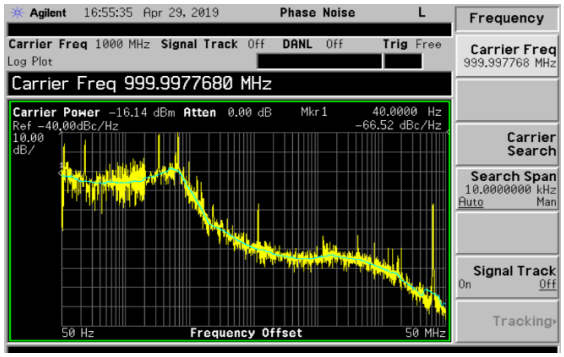
Fig. 11. Layout of the proposed PLL

IV. CONCLUSIONS

The proposed two-negative feedback loop PLL introduced the FVC to reduce the phase noise and jitter of the conventional PLL by adding one more negative feedback loop. The outer negative feedback loop is a conventional PLL loop. The inner negative feedback loop is inside the negative feedback loop of a conventional PLL. The independent inner loop does a negative feedback function to the outer loop. It improves the phase noise characteristics and the stability of PLL without requiring complicated auxiliary circuits and components which occupy a large area or consumes a large amount of power. It shows approximately 20dB improvement at 1MHz offset from 1GHz carrier frequency.



(a)



(b)

Fig. 12. Phase noise measurement result of the (a) conventional (b) proposed PLL.

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