An Implementation of MIMO PHY Modulator for IEEE 802.11n WLAN System

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***Abstract* - This paper presents designing of wireless local area network (WLAN) modem which is suited to video streaming in internet of things (IoT). Many concepts based on video streaming are introduced recently, and these systems need communication modem supporting high throughput for transmission of high quality of video. In this paper, WLAN modem using 2 × 2 multiple-input multiple-output (MIMO) orthogonal frequency division multiplexing (OFDM) technique is designed. The proposed WLAN modem can support max 260 Mbps. The ASIC is designed with several hardware-optimized techniques, and finally it can occupy 58.8 K gate counts and consumes 15.9 mW which are lower than existing designs.**

I. INTRODUCTION

Internet of things (IoT) is regarded recently as the most promising form of future wireless communication environments. Although there is no general definition about the IoT yet, many researchers have been studied to realize this IoT environment [1], [2]. Because each IoT application can need different requirement, for the selection of wireless communication technique in IoT environment, it is needed to specify the target system. Among many applications of IoT, we focus on video streaming consideration which needs higher data rates than others [3]. Wireless local area network (WLAN) technique is suited to cover this high data rate and guarantee of quality of service (QoS) [4]. Therefore, in this paper, we design of WLAN modem using multiple-input multiple-output (MIMO) orthogonal frequency division multiplexing (OFDM) technique for supporting max 260 Mbps.

The target designed system can support max 260 Mbps by using 2 × 2 MIMO-OFDM system in physical (PHY) layer. The encoding part of transmitter is designed according to the IEEE 802.11n standard [5]. The signal bandwidth 40 M is used, and accordingly the system clock is 40 M. Also, the long guard interval (0.8 μs) is used. The target designed system can support both single input single output (SISO) / MIMO technique, and each antenna configuration can support max 130 / 260 Mbps. The receiver is designed correspondingly, but some part are not defined in standard, so that we develop 3 algorithms for each MIMO decoding part; MIMO decoding algorithm, MIMO channel estimation algorithm, and MIMO phase-offset tracking and compensation algorithm.

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II. IEEE 802.11n PHY MODULATOR

The appetite for higher data rate continues as consumer demand for bandwidth hungry applications like gaming, streaming audio and video grows. Advancement in handset processors and further integration of technologies like higher mega-pixel cameras into handsets, create a never ending need for more bandwidth consuming applications at longer ranges and more efficient utilization of the limited spectrum available to network operators.

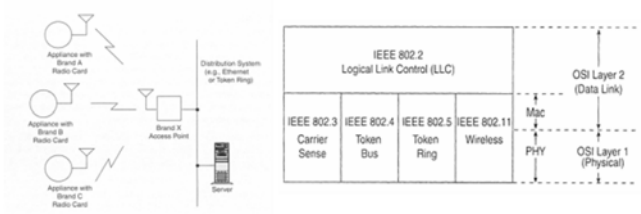

Fig. 1. IEEE 802 LAN standard family

On the other hand, WLAN as shown in Fig. 1, the technology initially expected to provide only limited range and bandwidth has come a long way. Since the first IEEE 802.11 standard in 1997, the maximum data rate has climbed from 2 to 54 Mbps [6]. Unfortunately, every increase in rate came at the expense of a loss in range. In the IEEE 802.11a/g standards, for instance, the highest data rate of 54 Mbps is achieved through the use of 64-QAM. The use of such highly spectral efficient higher order modulations requires a significant larger SNR than the simple BPSK modulation used for the lowest 1 Mbps rate, resulting in a significant loss in range. In addition, the link becomes more vulnerable to co-channel interference, which reduces the total system capacity.

The solution to obtain significant higher data rates and increase range performance at the same time is MIMO-OFDM [7, 8]. MIMO-OFDM increases the link capacity by simultaneously transmitting multiple data streams using

multiple transmit and receive antennas. It makes it possible to reach data rates that are several times larger than the current highest 802.11a/g rate of 54 Mbps without having to employ a larger bandwidth or a less robust QAM constellation [9]. After almost a decade of research on MIMO-OFDM, this technique is now ready to succeed OFDM as the dominant transmission technique in wireless LAN. With the introduction of MIMO-OFDM wireless LAN products in 2004 by Airgo Networks and the advent of the MIMO-OFDM based 802.11n standard, the performance of wireless LAN in terms of throughput and range is brought to a significantly higher level, enabling new applications outside the traditional wireless LAN area. The one time vision to replace wires in home entertainment applications, like TV cable replacement, has become a reality.

In July 2003, the 802.11n task group was formed to create a new wireless LAN standard as shown in Fig. 2. The main goal of this new standard is to give a throughput of at least 100 Mbps at the MAC data service access point [10]. A number of proposals were made that all share three common elements: the use of MIMO-OFDM, 20 and 40 MHz channels, and packet aggregation techniques. Based on this common ground, in July 2005 a joint proposal group was formed to create the first draft 802.11n standard [5]. The 802.11n standard defines a range of mandatory and optional data rates in both 20 and 40 MHz channels. Table 1 lists the mandatory Modulation and Coding Schemes (MCS) and their corresponding data rates. In addition to these rates, there are several other optional rates. One optional feature is to use a reduced guard interval of 400 ns instead of 800 ns, which increases the maximum data rate for 2 spatial streams in a 40 MHz channel to 300 Mbps. Other optional rates use 3 or even 4 spatial streams. The highest optional data rate defined by 802.11n is 600 Mbps, which is achieved by using 4 spatial streams in a 40 MHz channel with a 400 ns guard interval. The achievable data rates as MCS, when the 2x2 MIMO scheme, 800ns GI, 20MHz BW are assumed, are listed on Table 2. The achievable data rate for 40MHz BW can be calculated by be double of the data rate for 20MHz BW.

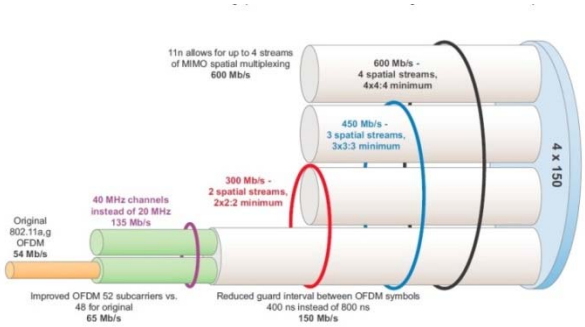

Fig. 2. Developments in IEEE 802.11n standard

As shown in Fig. 3, PHY layer includes the following 3 functional entities: 1) Physical Medium Dependent function (PMD), 2) Physical Layer Convergence function (PLCP), 3) Physical Layer Management function. High throughput (HT) OFDM PHY later consists of next two protocol function: 1) PMD function, which defines the characteristics and method of transmitting and receiving data through a wireless medium between two or more stations, each using the HT OFDM PHY, 2) PHY convergence function, which adapts the capabilities of the Physical Medium Dependent (PMD) system to the PHY service and defines a method of mapping the IEEE 802.11 PHY sublayer Service Data Units (PSDU) into a framing format suitable for sending and receiving user data and management information between two or more stations using the associated PMD system. Fig. 4 shows the Tx block diagram for HT format packet.

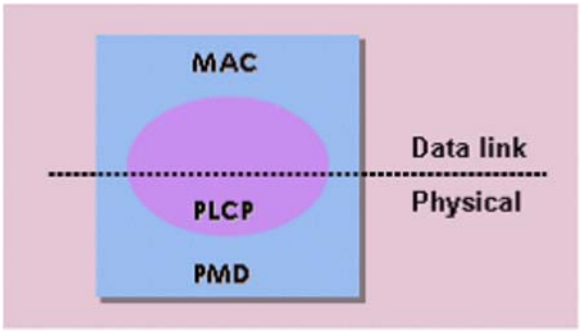

Fig. 3. PHY components

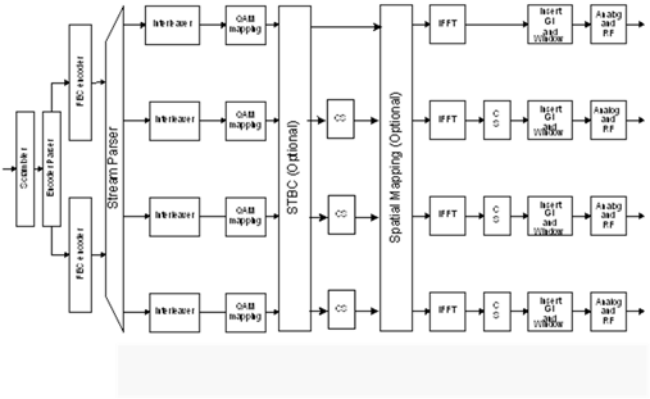

Fig. 4. Tx block diagram for HT format packet

III. SYTEM DESCRIPTION

Fig. 5 shows the block diagram of the designed MIMO PHY modulator. As shown in Fig. 2, all blocks of Tx module are architected and designed according to the IEEE 802.11n standard. In case of interleaver, it is designed to use 2 block random access memory (RAM). The final output is connected to inverse fast fourier transform (IFFT) with a control signal. The transmitted signal will go through wireless channel and then come into the Rx module after FFT process.

TABLE 1.
Main features of the designed MIMO PHY modulator

Parameters	Features
System	Compliant with IEEE 802.11n standards
Data rate	Max. 130Mbps @ 20MHz Max. 260Mbps @ 40MHz
Transmission Scheme	2x2 MIMO-OFDM scheme with STBC/SDM

Parameters	Features
Bandwidth	20 MHz / 40 MHz
Modulation	BPSK / QPSK / 16QAM / 64QAM
RF Freq.	5GHz
Guard Interval	Long guard interval (800ns)

TABLE 2.
Data rate as MCS at 2x2 MIMO / 800ns GI / 20MHz BW

MCS	Modulation	Coding Rate	Data rate (Mbps)
8	BPSK	1/2	13
9	QPSK	1/2	26
10	QPSK	3/4	39
11	16-QAM	1/2	52
12	16-QAM	3/4	78
13	64-QAM	2/3	104
14	64-QAM	3/4	117
15	64-QAM	5/6	130

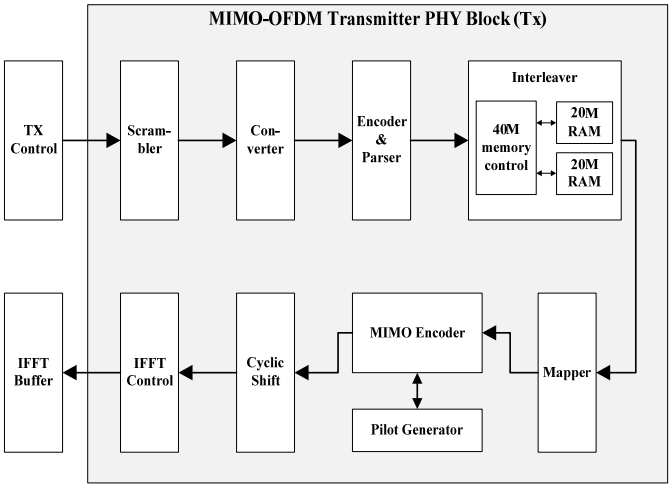

Fig. 5. Block diagram of the designed MIMO PHY modulator

IV. BLOCK DESCRIPTION

In this section, detail descriptions for each several block are presented. The block descriptions are presented as an order of data path which input data might be gone through sequentially. However, since there are so many detail blocks in this system, we focus to describe major and important hardware-optimized blocks we designed.

The first function is scrambler. The scrambler converts an input string into a seemingly random output string of the same length, thus avoiding long sequences of bits of the same value. The scrambler is designed as shown in Fig. 6.

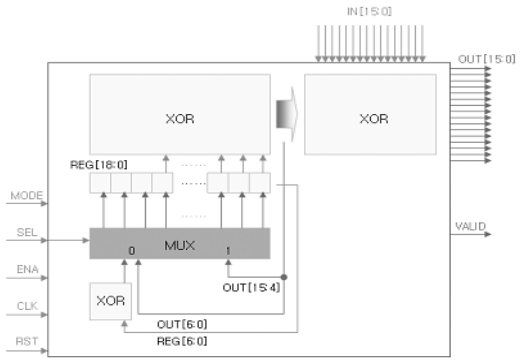

Fig. 6. Block diagram of the designed scrambler

The next function is convolutional encoder. The encoder makes the input data be coded with longer length in order to be robust to the error during the communication. In this system, the convolutional encoder is designed as shown in Fig. 7.

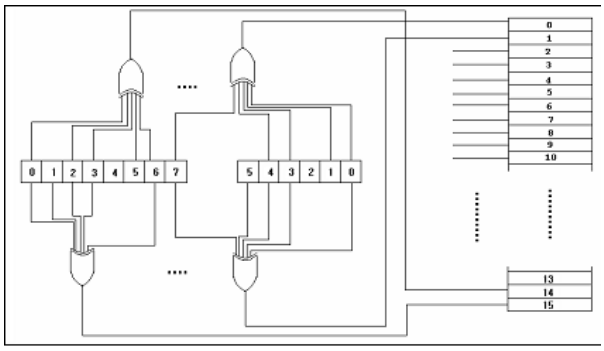

Fig. 7. Block diagram of the designed convolutional encoder

The detail description for parser function is omitted in this paper, because it is the exactly same with standard document. The next function is interleaver. The interleaver function shuffles source symbols across several code words, thereby creates a more uniform distribution of errors. In this system, the interleaver is designed as shown in Fig. 8.

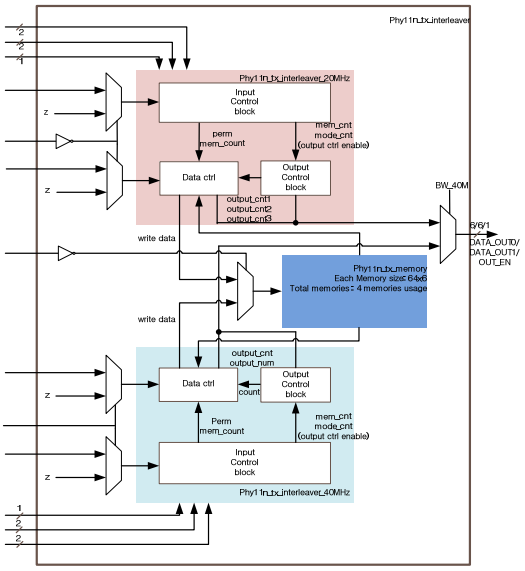

Fig. 8. Block diagram of the designed interleaver

The mapper and pilot generator is exactly same with standard document, so the detail descriptions for those functions are omitted.

MIMO encoder allows the use of spatial multiplexing and transmit diversity transmission schemes. In this system, the MIMO encoder is designed as shown in Fig. 9.

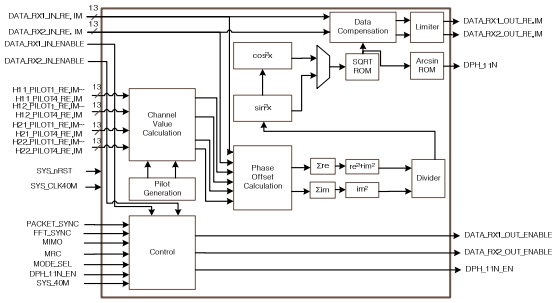

Fig. 9. Block diagram of the designed MIMO encoder

Finally, the encoded data is gone through IFFT function. In this system, IFFT function is implemented externally, so the control block is designed as shown in Fig. 10.

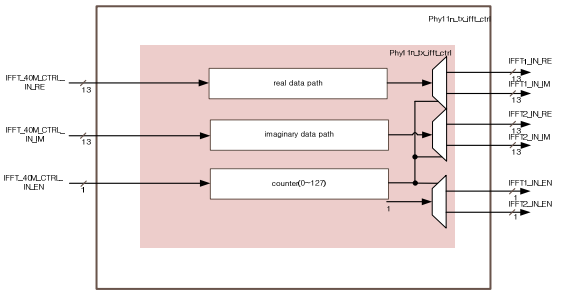

Fig. 10. Block diagram of the designed IFFT controller

V. FPGA IMPLEMENTATION AND RESULTS

The proposed MIMO-OFDM PHY modem is synthesized and mapped on Xilinx field programmable gate array (FPGA) using core of Vertex-4: xc4vlx160ff1148-10. The implementation result is summarized in Table 3.

The verification scenario is based on video transmission as shown in Fig. 11. The input video data is generated with a size of 320x240, which video size is marginally covered by throughput of 130Mbps at 60fps. Corresponding Rx part is designed on PC ideally for testing Tx part. As a verification result, the designed system can support 60fps for 20MHz system clock and 120fps for 40MHz. The result can prove the designed system is suited to target throughput of 130/260 Mbps.

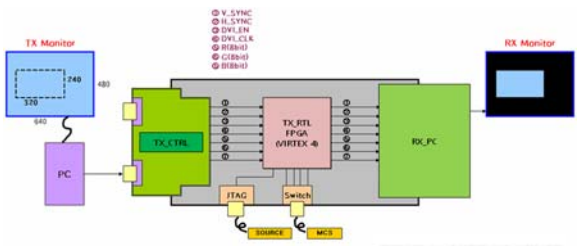

Fig. 11. FPGA verification scenario

TABLE 3.
FPGA Implementation results

Item	Usage (proportion)
Register bits	18148 (13%)
Block Rams	2 (0.7%)
DSP48s	96 (100%)
Global Clock Buffers	4 (12%)
LUTs	59911 (44%)
Max. Frequency	101.5 MHz

VI. CHIP IMPLEMENTATION AND RESULTS

As a synthesis with 65nm CMOS technology, gate counts for each block are presented in Table 4. The total gate count is around 58.8k.

TABLE 4.
Gate count for each blocks

Block	Gate count
Tx Controller	4.1k
Scrambler	0.8k
Convolutional Encoder + Interleaver	20.8k
Converter	1.2k
Mapper	6.1k
Pilot Generator	1.6k
MIMO Encoder	5.9k
Cyclic shift	14.5k
IFFT controller	3.8k
Total	58.8k

Fig. 12 and Fig. 13 show the photo of the implemented chip. The chip is implemented using the 65nm CMOS technology and packaged with 208-pin QPF. The operating clock frequency is 40MHz, and the supply voltage is 3.3V and 1.2V for I/O and core each. The gate count of the implemented chip is about 60K, and the active area occupied is about 1.69mm^2.

We compared our design with several existing ASIC design for the similar target system. [10-13] were designed for wireless communication system based on IEEE 802.11n standard. Since our designed system is PHY Tx, for the comparison, we estimated the information of designed ASIC correspond to the PHY Tx for each designed System. Table 5 shows the comparison results. We can see our designed ASIC can show lower gate count and power consumption.

TABLE 5.
Comparison of the proposed system with previously implemented 802.11n transceivers

	[10]	[11]	[12]	[13]	This work
Integration	MAC/PHY	PHY	MAC/PHY/RF	PHY	PHY (Tx)
Antenna	3 × 3	2 × 3	2 × 2	2 × 2	2 × 2
Max. data rate	300 Mbps	270 Mbps	300 Mbps	130 Mbps	260 Mbps
Gate count	3.56 M	2.078 M	N/A	1.133 M	0.58 M
Clock frequency	N/A	40 MHz	N/A	40 MHz	40 MHz
Technology	180 nm	130 nm	130 nm	180 nm	65 nm
Core area (digital)	60.84 mm^2	9.7 mm^2	25 mm^2	16.7 mm^2	1.69 mm^2
(Estimated) gate count (PHY Tx)	399 K	869 K	N/A	98.4 K	58.8 K
(Estimated) power (PHY Tx)	210mW	195 mW	293 mW	31mW	15.9 mW

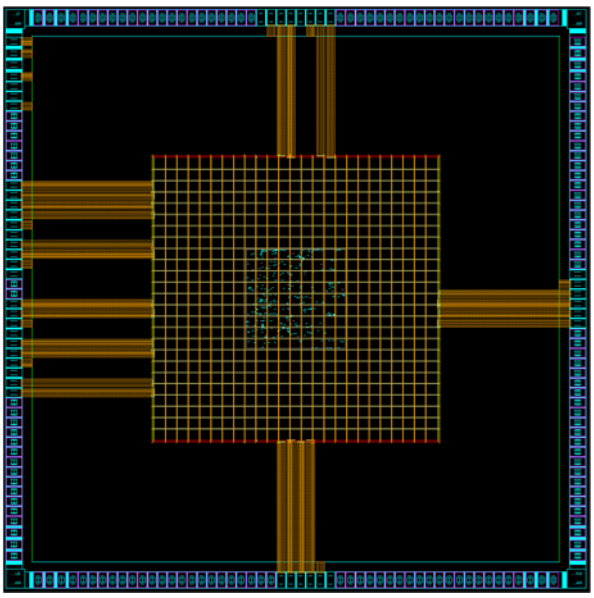

Fig. 12. Layout of the designed MIMO PHY modulator chip

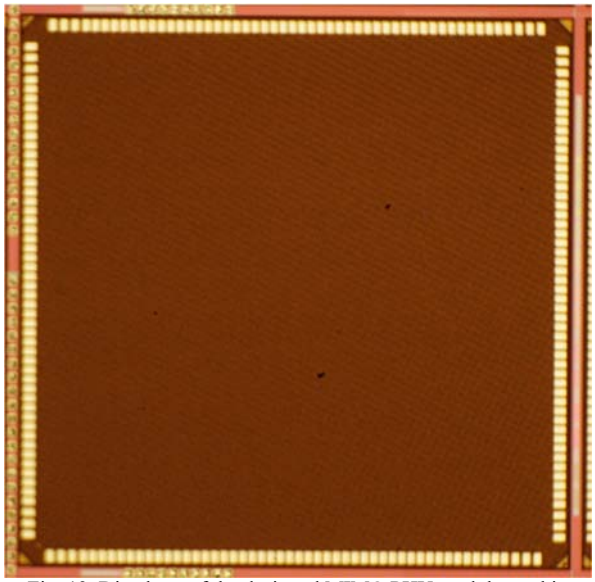

Fig. 13. Die photo of the designed MIMO PHY modulator chip

VII. CONCLUSIONS

In this paper, we designed 2 × 2 MIMO-OFDM PHY modem for video streaming service in IoT systems. The video streaming application in IoT systems needs high data rate, so that we selected WLAN technique based on IEEE 802.11n technique. Finally, the designed modem can support max 260 Mbps. We implemented our design to FPGA using Xilinx Vertex-4. As a FPGA implementation result, the designed MIMO-OFDM PHY modem uses 44% of total LUTs and works in clock frequency of 101.5 MHz. In addition, through 65nm CMOS technology and packaging with 208-pin QPF, we successfully implemented our design to ASIC chip. The operating clock frequency is 40 MHz, and the supply voltage is 3.3 V and 1.2 V for I/O and core each. The gate count of the implemented chip is 58.8 K, and the active area occupied is about 1.69 mm^2. Furthermore, the power consumption of the implemented chip is 15.9 mW. By comparing with other designs for similar target system, we can result that the gate count and consumed power of our design are lower than existing designs.

ACKNOWLEDGMENT

This work was supported by the Industrial Core Technology Development Program (10049009, Development of Main IPs for IoT and Image Based Security Low-Power SoC) funded by the Ministry of Trade, Industry & Energy. This work was also supported by IDEC (IPC, EDA Tool, MPW).

REFERENCES

[1] L. Tan and N. Wang, “Future internet: The internet of things,” in Proc. 3rd Int. Conf. Adv. Comput. Theory Eng. (ICACTE), Chengdu, China, Aug. 2010, pp. V5-376-V5-380.
[2] Y. Liu and G. Zhou, “Key technologies and applications of internet of things,” in Proc. 2012, 5th Int. Conf. Intell. Comput. Technol. Autom. (ICICTA),

Zhangjiajie, China, Jan. 2012, pp. 187-200.
[3] R. Pereira and E. G. Pereira, “Video Streaming Considerations for Internet of Things,” in Proc. Future Internet of Things and Cloud (FiCloud), 2014 International Conference on, Barcelona, Spain, Aug. 2014, pp. 48-52.
[4] V. Jones and H. Sampath, “Emerging technologies for WLAN,” IEEE Commun. Mag., vol. 53, no. 3, pp. 141-149, Mar. 2015.
[5] IEEE standard 802.11n supplement. Part 11: Wireless LAN Medium Access Control(MAC) and Physical Layer(PHY) Specifications. Amendment 5: Enhancements for higher throughput (2009).
[6] R. van Nee, G. Awater, M. Morikura, H. Takanashi, M. Webster, and K. Halford, “New High Rate Wireless LAN Standards”, IEEE Communications Magazine, Vol. 37, No. 12, pp. 82–88, Dec. 1999.
[7] G.G. Raleigh and J.M. Cioffi, “Spatio-Temporal Coding for Wireless Communications”, in Proc. 1996 Global Telecommunications Conf., pp. 1809–1814, Nov. 1996.
[8] G.G. Raleigh and V.K. Jones, “Multivariate Modulation and Coding for Wireless Communication”, IEEE Journal on Sel. Areas in Comm., Vol. 17, No. 5, pp. 851–866, May 1999.
[9] R. van Nee, A. van Zelst, and G. Awater, “Maximum Likelihood Decoding in a Space Division Multiplexing System”, IEEE VTC 2000, Tokyo, Japan, May 2000.
[10] P. Petrus, et al. “An integrated draft 802.11n compliant MIMO baseband and MAC processor”. in Proc. of IEEE international solid-state circuits conference, pp. 266–267, Feb. 2007.
[11] J. Son, I. Lee, and S. Lee, “Asic implementation and verification of MIMO-OFDM transceiver for wireless LAN”, in proc. of IEEE international symposium on personal indoor and mobile radio communications, pp. 1–5, Sep. 2007.
[12] M. Zargari, et al. “A dual-band CMOS MIMO radio SoC for IEEE 802.11n wireless LAN”, IEEE Journal of Solid State Circuits, vol. 43, no. 12, pp. 2882–2895, Dec. 2008.
[13] J. Im, M. Cho, Y. Jung, Y. Jung, and J. Kim, “A Low-power and Low-complexity Baseband Processor for MIMO-OFDM WLAN Systems”, vol. 68, pp. 19-30, Dec. 2012.

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