

# A Chopper-Stabilized Current-Feedback Instrumentation Amplifier with a Tunable Gain and Low-cutoff Frequency for EEG Acquisition Applications

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**Abstract** - A chopper-stabilized current-feedback instrumentation amplifier (CFIA) for EEG acquisition applications is presented. The proposed design includes an AC-coupled CFIA and a switched-capacitor (SC) integrator. By using appropriate chopper modulation technique in both input and output stages of the CFIA,  $1/f$  noise is reduced. An input-referred noise power spectral density (PSD) of  $63 \text{ nV}/\sqrt{\text{Hz}}$  is obtained. The SC integrator was employed to control the low cutoff frequency of the CFIA by adjusting the sampling frequency of the SC integrator. Simulation results show that the proposed amplifier provides a common mode rejection ratio (CMRR) of 114 dB and a tunable gain up to 57 dB. The low cutoff frequency is determined within a range from mHz to a few Hz depending on the switching frequency of the SC integrator and the high cutoff frequency is approximately 600 Hz. The total power dissipation of the CFIA is  $1.9 \mu\text{W}$ .

## I. INTRODUCTION

There have been efforts to develop efficient devices to read bio-potential information for human machine interface applications. Since CMOS technology and low power integrated circuit (IC) design technique have advanced, there has been great interest in efficient portable devices for human machine interface applications. Various types of front-end circuits for bio-potential measurements were reported [1]–[10]. From Fig. 1 [11], the common bio-potential signals including Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) have different frequency ranges and small signal amplitude. Thus integrated circuits (ICs) for acquisition of bio-potential should be able to accommodate a wide range of signal amplitude and frequency since they have to amplify the weak bio-potential signals detected by microelectrodes and

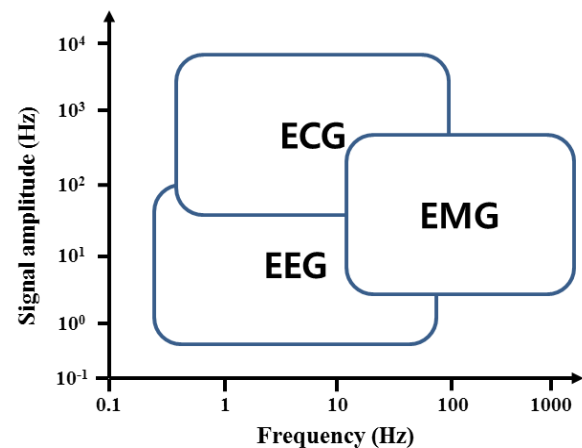


Fig. 1. Frequency range and amplitude range of typical bio-potential signals.

selectively filter out the unnecessary signals. In addition they should have low noise characteristic and high common mode rejection ratio (CMRR). As a result, one of the most challenging parts in the design of neural recording system is neural signal amplifier. To satisfy former requirements, an instrumentation amplifier (IA) is preferred. Compared to ordinary non-inverting and inverting feedback amplifiers, an IA has many advantages including a high open-loop gain, a high CMRR, and very high input impedance. There are some methods to implement an IA including voltage-feedback method, current-feedback method. Compared to a voltage-feedback IA, a current-feedback instrumentation amplifier (CFIA) has an advantage of low power consumption [12], which is appropriated for low power requirement of bio-potential acquisition devices. A CFIA can be implemented in two configurations; the one is a direct current-feedback (DCF) configuration and the other is indirect current-feedback (ICF) configuration. The ICF configuration is preferred since it has better linearity and larger common-mode input range compared with the DCF configuration [13].

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In addition, since the frequency of EEG signals range from mHz to a few hundred Hz [1] that the reduction in 1/f noise is critical for EEG measurements. Moreover, large DC offsets present across recording electrodes owing to electrochemical effects at the electrode-tissue interface [2]. Thus integrated circuits (ICs) used for bio-potential measurements require DC offset blocking technique and low-frequency noise reduction techniques including a chopper modulation technique [14].

In this paper, an AC-coupled CFIA utilizing the chopper modulation technique to improve low-frequency noise performance is introduced. Also proposed design includes the switched-capacitor (SC) integrator for low cutoff frequency control. Unlike the previously reported CFIA [10], where an additional  $G_m$ -C high-pass filter (HPF) stage was used for control of low cutoff frequency, the proposed CFIA uses an SC integrator in internal loop that provides reduced power consumption and improved area efficiency.

## II. ARCHITECTURE OF AMPLIFIER DESIGN

### A. Overall Circuit Design

The schematic of the proposed CFIA architecture is shown in Fig. 2. The proposed CFIA has AC-coupled input, which reduces electrode offset voltage to avoid saturation of amplifier, a SC integrator for low cutoff frequency control and offset reduction. AC-coupling has many advantages: rail-to-rail sensing ability, high-gain accuracy, and DC offset cancellation. In this design input capacitor  $C_{1,2}$  are 40 pF and both chopping frequency of 1st and 2nd are 500 Hz and 1 kHz, respectively, which are higher than 1/f noise corner frequency. The amplifier's gain is determined by input transconductance  $G_{m1}$ , feedback transconductance  $G_{mf}$ , and the ratio of the resistors  $R_1$ ,  $R_{21}$ , and  $R_{22}$  [12]. Thus the overall gain of the proposed CFIA is

$$A_M = \frac{G_{m1}}{G_{mf}} \frac{R_1 + R_{21} + R_{22}}{R_1}, \quad (1)$$

where  $R_{21}$  and  $R_{22}$  are consisted of a diode-connected PMOS transistor that acts as a pseudo-resistor and  $R_1$  is 1 k $\Omega$  poly resistor. Compared to conventional poly resistors, the diode connected pseudo-resistors can achieve extremely large resistance value while they occupy small area [2]. By tuning the bias voltage, resistance value across  $R_{21}$  and  $R_{22}$  changes. As a result, tunable gain can be realized. Gain is varied from 37 dB to 57 dB.  $C_3$  and  $C_4$  are compensation capacitors. Fig. 3 shows the block diagram of the SC integrator. The SC integrator in this paper consumes much less power compared with that with a  $G_m$ -C HPF [10] since the SC integrator consumes less power (50 nW) compared with the HPF (800 nW). Even more using SC integrator is more beneficial that low-cutoff frequency can be easily controlled by tuning switching frequency of SC integrator, while  $G_m$ -C HPF stated in [10] only provides constant low-cutoff frequency. The proposed CFIA also has a simpler circuit structure for the high-pass-filtering characteristics compared to the previously reported amplifier [3]. The low cutoff

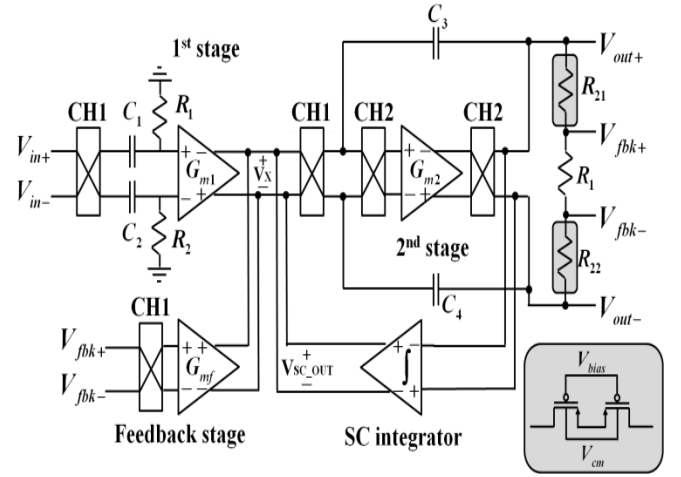


Fig. 2. Schematic of the proposed current feedback instrumentation amplifier.

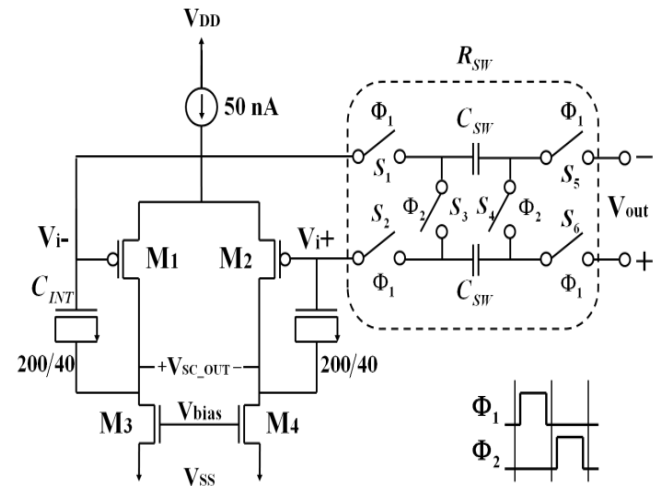


Fig. 3. Schematic of the switched-capacitor integrator.

frequency of the amplifier reported in [3] is determined by input and feedback SC networks. Thus the gain and the low cutoff frequency of these amplifiers are determined by the ratio between four capacitors, requiring optimization between the gain and the low cutoff frequency. However, the gain and the low cutoff frequency of the proposed amplifier can be determined independently. The SC integrator loop of the proposed CFIA is made up of the 2<sup>nd</sup> stage of the CFIA and the SC integrator.

### B. Design of SC integrator

The implemented SC integrator, shown in Fig. 3, is a conventional integrator [15]. With help of derivation procedure of [12], the transfer function of the SC integrator loop can be derived by the following order. Assume that the voltage gain of the integrator amplifier has a finite open-loop gain of  $A_{SC}$ . Next, using the Norton's theorem and after doing some mathematical procedure the transfer function of the SC integrator is given by

$$\beta(s) = \frac{V_{SC\_OUT}}{V_{out}} = - \left( \frac{A_{SC}}{sC_{INT}R_{SW}(1+A_{SC})+1} \right). \quad (1)$$

Assuming that  $A_{SC} \gg 1$  and  $A_v$  is the DC gain of the second stage, the transfer function of the SC integrator loop can be expressed as

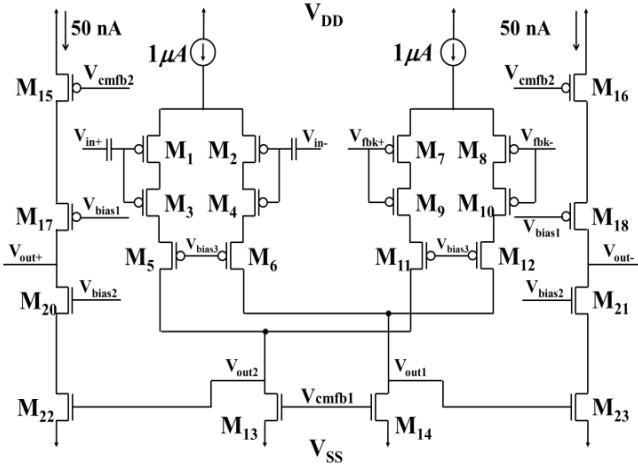


Fig. 4. Schematic circuit of the 1st, feedback, and 2nd stage.

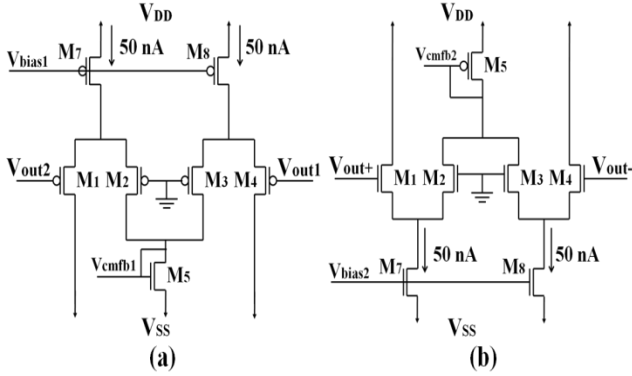


Fig. 5. Schematic of the common-mode feedback circuits (a) and (b).

$$\frac{V_{out}}{V_X}(s) = \frac{A_v}{1 + A_v \beta(s)} \approx \frac{sC_{INT}R_{SW} + 1/A_{SC}}{sC_{INT}R_{SW}/A_v + 1}, \quad (2)$$

where  $R_{SW}$  is the equivalent resistor of the switch network with  $R_{SW} = 1/f_s C_{SW}$  ( $f_s$  is the switching frequency) [15]. The overall high-pass filtering capability is determined by combination of high-pass term of AC-coupling and transfer function of SC integrator loop described by

$$\frac{V_{out}}{V_{in}} = \frac{s\tau_1}{s\tau_1 + 1} \frac{R_1 + R_{21} + R_{22}}{R_1} \frac{sC_{INT}R_{SW} + 1/A_{SC}}{sC_{INT}R_{SW}/A_v + 1} \quad (3)$$

where  $\tau_1 = R_1 C_1$  and  $\tau_2 = R_{SW} C_{INT} / A_v$ . Because of  $R_1$  is consisted of large pseudoresistor,  $\tau_1$  is much larger than  $\tau_2$ . Therefore, from (3) it is clear that the SC integrator loop provides high-pass filtering characteristics and the low cutoff frequency is

$$f_L = \frac{1}{2\pi} \frac{A_v}{C_{INT} \left( \frac{1}{f_s C_{SW}} \right)} = \frac{1}{2\pi} \frac{C_{SW}}{C_{INT}} A_v f_s. \quad (4)$$

From (4), the low cutoff frequency is determined by the ratio of the capacitor pair in the SC integrator and the DC gain of the second stage. For 1 Hz cutoff frequency  $C_{SW}$  is chosen to be 100 fF and  $C_{INT}$  is selected to be 2.4 pF.  $C_{INT}$  is MOS capacitors of a thick oxide NMOS transistor to obtain a large capacitance value with smaller area. Fig. 4 describes the schematic circuit of the 1<sup>st</sup>, feedback, and 2<sup>nd</sup> stage of the CFIA amplifier. The proposed CFIA employs two-stage cascoded amplifier with a cascoded input stage with shared current-summing and output-stage. Cascoded input stage is adopted to increase the CMRR. To minimize 1/f noise, a PMOS transistor was chosen as an input transistor. Transistors  $M_1$ – $M_4$  and  $M_7$ – $M_{10}$  have an identical W/L value of 200/1 to maximize their transconductance and to minimize the influence of thermal noise from them [2]. Transconductance  $G_{m1}$  and  $G_{mf}$ . The bias currents of 1<sup>st</sup> and feedback stage were 1  $\mu$ A and that of the cascode and the second stage was 50 nA. The channel current is scaled differently for each branch to improve noise performance and to save power. Using the noise analysis, approximated input-referred thermal noise and flicker noise of this circuit can be described as

$$\overline{v_{n,th}^2} \approx \frac{16kT}{3} \frac{1}{g_{m1}} \left[ 2 + \frac{g_{m13}}{g_{m1}} \right] \quad (5)$$

$$v_{n,1/f}^2 \approx \frac{2}{W_1 C_{ox} f} \left[ \frac{2K_{F1}}{L_1} + \frac{K_{F13} \mu_n L_1}{\mu_p L_{13}^2} \cdot \frac{I_{D13}}{I_{D1}} \right] \quad (6)$$

where  $r_o$  is the output resistance,  $f$  is the signal frequency,  $W$ ,  $L$ , and  $\mu$  are the channel width, channel length, and the effective mobility of the MOSFET device, respectively, and  $K_F$  is the process-dependent coefficient of flicker noise. From (5), it is clear that increasing transconductance  $g_{m1}$  leads to the lower thermal noise. Thus, the majority of bias current flows through the input pair to maximize its  $g_m$ . To achieve high  $g_m$  under circumstances of small current level, it is good to operate transistors  $M_1$ – $M_4$  and  $M_7$ – $M_{10}$  in the subthreshold region. In addition from (6), flicker noise is inversely proportional to gate width as well as gate length; large transistor size is selected to minimize the influence of flicker noise. Also, PMOS transistor has an isolated back gate, which enables input  $g_m$  to be less dependent on the input common-mode (CM) voltage: This increases the CMRR. The schematic of the two common-mode feedback (CMFB) circuits are shown in Fig. 5. The bias currents to each branch  $M_5$ ,  $M_7$ ,  $M_8$  are set to 50 nA to reduce power consumption.

### III. RESULTS AND DISCUSSION

The proposed CFIA was designed using the 0.18  $\mu$ m standard CMOS process and simulated using the

CADENCE SPECTRE and SPECTRE RF with 1 V DC supply voltage. The power dissipation of the CFIA is 1.9  $\mu$ W. Fig. 6 is a layout of proposed amplifier. Fig. 7 and Fig. 8 show the simulated Periodic AC Analysis (pac) of the amplifier's small-signal gain. Simulation results show that the maximum voltage gain is 57 dB and the high cutoff frequency is 600 Hz.

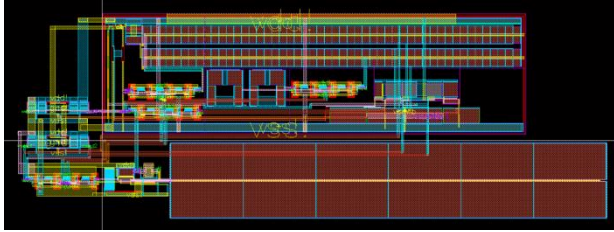


Fig. 6. Layout of proposed circuit.

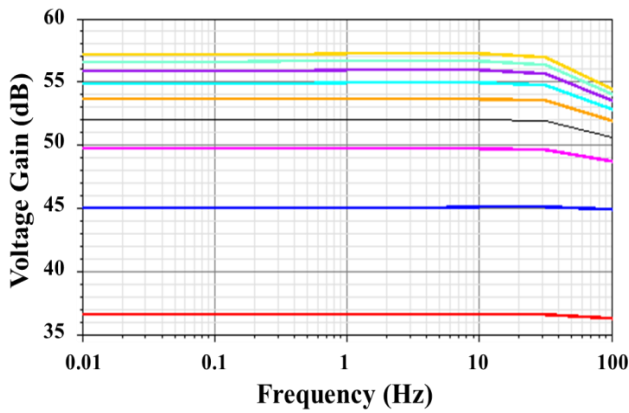


Fig. 7. Simulated periodic AC analysis of the amplifier showing tunable gain.

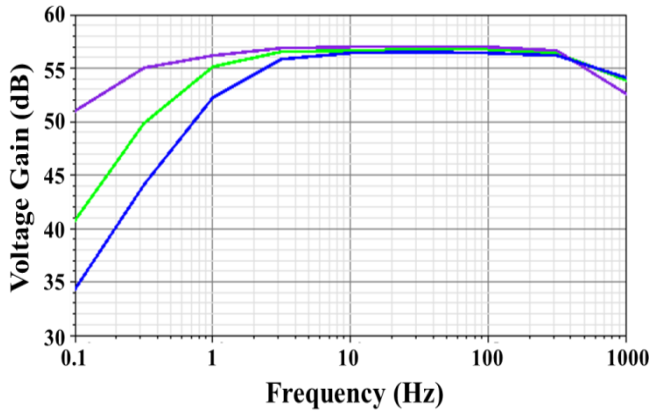


Fig. 8. Simulated periodic AC analysis of the amplifier showing tunable low cutoff frequency.

Fig. 8 reveals the low cutoff frequency can be changed by tuning the switching frequency of the SC integrator. For example, when the frequency is changed from 20 Hz to 100 Hz, the low cutoff frequency was shifted from 240 mHz to 1.7 Hz. Fig. 9 describes the common-mode gain of the amplifier as a function of the frequency. Since the common-mode gain was approximately  $-54$  dB the CMRR was calculated to be approximately 114 dB. Fig. 10 depicts simulation results of SPECTRE RF periodic noise (pnoise) analysis with chopping and without chopping. Twice

chopper modulation was used to suppress input and intermediate stage  $1/f$  noise. When the both chopper modulation technique were used, a  $1/f$  noise power spectral density (PSD) of 117  $\text{nV}/\sqrt{\text{Hz}}$  was obtained at 100 mHz. However, without the chopping a  $1/f$  noise PSD of over 1  $\text{mV}/\sqrt{\text{Hz}}$  was obtained at 100 mHz. The proposed amplifier showed an input noise PSD of approximately 63  $\text{nV}/\sqrt{\text{Hz}}$  at 100 Hz. The total input referred noise integrated from 100

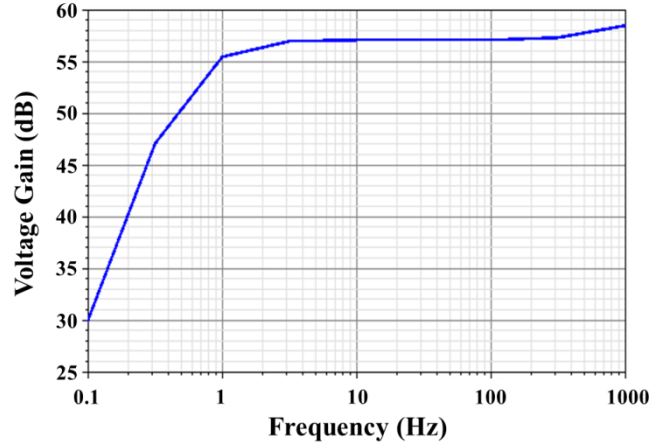


Fig. 9. Simulated periodic transfer function of the common-mode gain of the amplifier.

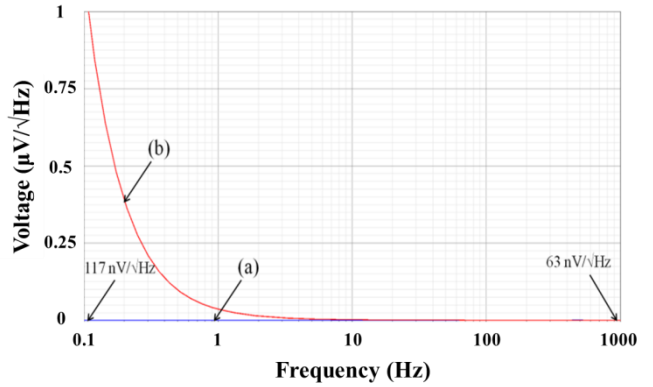


Fig. 10. Periodic noise analysis of the CFIA (a) with chopping (b) without chopping.

mHz to 100 Hz was  $0.71 \mu\text{V}_{\text{rms}}$ . To measure tradeoff between noise and power, the Noise-efficiency-factor (NEF) introduced by [16] is used. When NEF is lower it has better tradeoff. The formula of NEF is given by

$$NEF = V_{ni,rms} \sqrt{\frac{2 \cdot I_{total}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (9)$$

where  $V_{ni,rms}$  is the input-referred rms noise voltage,  $I_{total}$  is the total current drain in the amplifier,  $k$  is the Boltzmann's constant,  $U_T$  is the thermal voltage  $kT/q$ , and  $BW$  is the frequency bandwidth. The proposed amplifier achieves a NEF of 3.76. Both gain bandwidth and input noise measurement were done using Agilent dynamic signal analyzer 35670A. The experimental results of the neural amplifier are summarized in table I and they are compared

to state-of-the-art amplifiers. Comparing with others, it appears that this work achieves a good noise to power tradeoff performance, better area efficiency, and comparable CMRR.

TABLE I.  
Summary of Performance of Bioamplifiers

|                            | This work        | [10]                       | [3]               | [4]              |
|----------------------------|------------------|----------------------------|-------------------|------------------|
| Year                       | 2012             | 2011                       | 2007              | 2008             |
| Gain (dB)                  | 36-57            | 65                         | 41                | 48               |
| Low cutoff frequency (Hz)  | tunable          | 0.25                       | Tunable           | 0.5              |
| High cutoff frequency (Hz) | 600              | 1.1 k                      | 120               | tunable          |
| CMRR (dB)                  | 114              | 96                         | 105               | >120             |
| Input noise PSD (nV/√Hz)   | 63 (at 100 Hz)   | 51                         | 100 (at 100 Hz)   | 55.8 (at 100 Hz) |
| Input referred noise (μV)  | 0.71 (0.1-100Hz) | 0.73 (0.1-100Hz)           | 0.98 (0.05-100Hz) | 0.59 (0.5-100Hz) |
| Supply current (μA)        | 1.9              | 2.65 (CFIA) / 3.45 (total) | 1.1               | 2.3              |
| Supply voltage (V)         | 1                | 1                          | 1.8               | 3                |

IV. CONCLUSIONS

In this paper, a chopper-stabilized CFIA with a switched-capacitor (SC) integrator for EEG acquisition application is presented. The switched-capacitor (SC) integrator is used for control of the low cutoff frequency. The low cutoff frequency had a range from a few mHz to Hz and the high cutoff frequency was approximately 600 Hz. With the chopper stabilization an input-referred noise PSD of 63 nV/√Hz was obtained by the SPECTRE RF pnoise analysis. The CMRR and voltage gain were 114 dB and 57 dB, respectively. The CFIA showed a total power consumption of 1.9 μW under 1 V DC voltage supply.

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