# A DC-DC Converter with Voltage-Mode PWM Control

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***Abstract*** **- In this paper, a voltage-mode PWM controlled buck converter is addressed. It consists of a pair of fully-integrated switches, an LC filter, a type 3 compensation loop, an internal ramp & clock generator, and a dead-time generator. A portion of output is taken with a resistive divider and subtracted from an external reference voltage to generate an error voltage. Then the error voltage is compared with a ramp signal, creating a PWM signal for controlling high-side and low-side switches. This buck converter is fabricated in 0.18-μm CMOS process and area of control block is 0.28 mm$^2$. Input voltage is 3.3 V and target output voltage is 1.8 V. Peak measured power conversion efficiency is 94.38% at 150 mA constant load condition. In a load transient testing from 100 mA to 300 mA, overshoot settling time measures 17.44 us. Overshoot magnitude is 68 mV and undershoot settling time and magnitude is 8.56 us and 60.8 mV, respectively.**

***Keywords*****—Buck converter, Dead-time, Power conversion efficiency, Voltage-mode PWM control**

## I. INTRODUCTION

In many electronic devices, DC-DC conversion is required to supply power with desired voltage level. Since the output voltage of DC-DC converters is supplied as a VDD to subsequent circuits, ripple of the output voltage should be minimized. Linear regulators are well known for their superiority in ripple suppression. However, linear regulators are generally not suitable for applications that need efficient power converters. Efficiency of linear regulators depends on the difference between the input and output voltage level. Assuming a constant input voltage, if required output voltage gets lower, then power that is lost by the linear regulator increases proportionally. The reason for this efficiency degradation is that the voltage drop across a pass transistor of the linear regulator is the output voltage subtracted from the input voltage. Therefore, in order to maximize the efficiency of linear regulators, the output voltage should be close enough to the input voltage [1]. In other words, output voltage range of linear regulators lacks flexibility.

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Another problem arises when high current flows through pass transistors. Not having any switching elements, linear regulators have to let the current flow all the time which results in excessive thermal stress [2]. To disperse the heat effectively heat sinks could be adopted, which will make the system bulkier [3]. So it is not a decent solution for applications that require compact circuits.

One good example of such applications is portable devices. These run with a rechargeable battery that only supplies limited amount of energy. Among many aspects, especially when it comes to maximizing battery life of portable devices there has been an increasing demand for efficient DC-DC converters. Switched-mode power supply (SMPS) is inherently efficient compared to linear regulators [4], because its pass transistors toggle between on and off state to minimize the wasted energy. Also the switching action reduces heat dissipation, which allows DC-DC converters to operate without any heat sink, or at least smaller heat sink.

In this work, a voltage-mode pulse width modulation (PWM) controlled buck converter is implemented. In Section II, structure of the buck converter control circuits and details of important sub-blocks are explained. Simulation and measurement results are discussed in Section III. And lastly the conclusion is given in Section IV.

## II. DESIGN METHODOLOGY

### *A. Block Diagram*

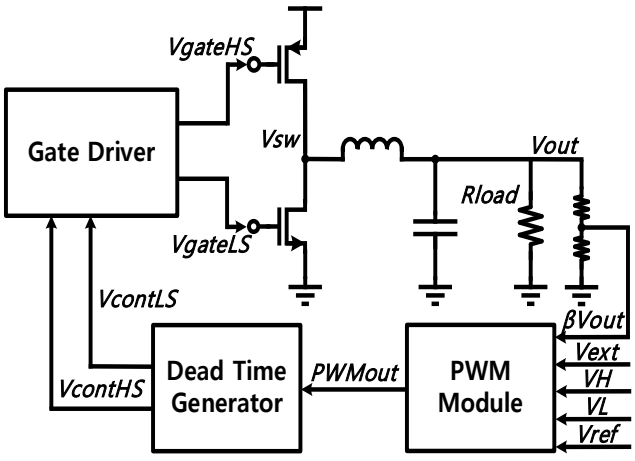


Fig. 1. Top block diagram of voltage-mode PWM controlled buck converter

Fig. 1 shows the overall structure of the proposed work. It consists of two CMOS switches, an off-chip inductor, an off-chip capacitor, a load circuit, a PWM module, a dead-time generator, and a set of gate drivers. At cold start, high-side pMOS switch is initially turned on and inductor current builds up during on-state. After on-state, off-state begins and high-side pMOS switch is turned off while low-side nMOS switch is turned on for the continuous flow of inductor current. With a pair of identical resistors that are integrated in the chip, a portion of the output voltage $\beta V_{out}$, which is half in this work, is delivered to the PWM module. By subtracting $\beta V_{out}$ from an external DC voltage $V_{ext}$, amplified error voltage is produced. Then that error voltage is compared with an internally-generated ramp voltage to generate a digital control signal *PWMout*. The structure of PWM module is illustrated in Fig. 2.

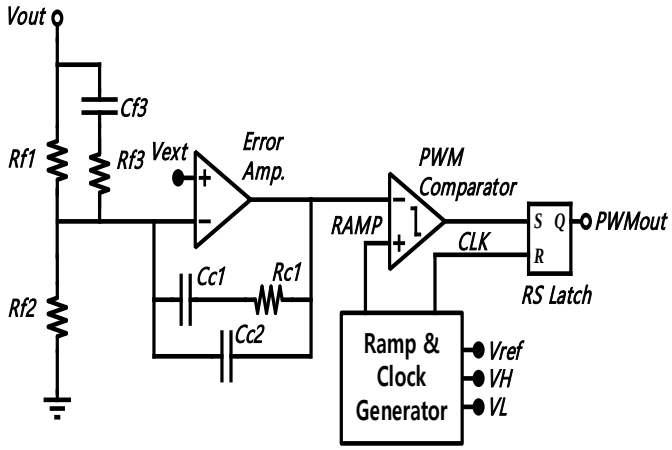


Fig. 2 Structure of PWM module

*B. Type 3 Compensation Loop*

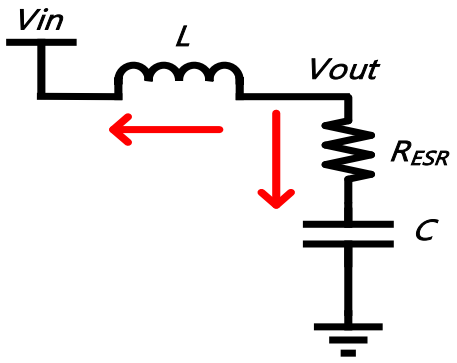


Fig.3 Simple modeling of the LC filter of a buck converter for analyzing double pole and ESR zero

From the simplified structure of a buck converter, a Kirchhoff's Current Law (KCL) equation

$$\frac{V_{out}-V_{in}}{sL}+\frac{V_{out}}{R_{ESR}+\frac{1}{sC}}=0 \quad (1)$$

is obtained. Therefore the frequency of double pole and equivalent series resistance (ESR) zero is

$$f_{LC}=\frac{1}{2\pi\sqrt{LC}} \quad (2)$$

$$f_{ESR}=\frac{1}{2\pi R_{ESR}C} \quad (3)$$

, respectively. To reduce output voltage ripple, ESR should be minimized and that usually set the frequency of ESR zero much higher than that of the double pole [5]. Phase will reach -180° before ESR zero boosts the phase. Thus there is a need for a compensation loop that counteracts the double pole for power stage stability.

A type 3 compensation loop is adopted for the PWM module to cancel the phase drop caused by the LC filter. In Fig. 2 additional passive components *Rf3*, *Cf3*, *Cc1*, and *Rc1* are added to the basic feedback path to introduce two zeros and two poles for compensation. Values of the components are chosen by the following procedure [5]:

1. Choose switching frequency $f_{sw}$ and crossover frequency $f_{cross}$. Rule of thumb is $0.1f_{sw} \le f_{cross} \le 0.2f_{sw}$.

$$f_{sw}=870\ kHz \rightarrow\ f_{cross}=87\ kHz \quad (4)$$

2. Calculate double pole frequency $f_{LC}$ and ESR zero frequency $f_{ESR}$.

$$f_{LC}=\frac{1}{2\pi\sqrt{10uH*6.8uF}}=19.3\ kHz \quad (5)$$

$$f_{ESR}=\frac{1}{2\pi*45m\Omega*6.8uF} \quad (6)$$

3. Decide frequency of required poles and zeros.

$$f_{z2}=f_{LC}=19.3\ kHz \quad (7)$$

$$f_{z1}=0.75*f_{z2}=14.5\ kHz \quad (8)$$

$$f_{p2}=f_{ESR}=487.6\ kHz \quad (9)$$

$$f_{p3}=\frac{f_{sw}}{2}=439\ kHz \quad (10)$$

4. Calculate passive components. Start by giving a reasonable value to $C_{f3}$.

$$C_{f3}=10\ pF \quad (11)$$

By selecting $L=10\ uH$ & $C=6.8\ uF$,

$$R_{f3}=\frac{1}{2\pi*C_{f3}*f_{p2}}=30.6\ k\Omega \quad (12)$$

$$R_{f1}=\frac{1}{2\pi*C_{f3}*F_{z2}}-R_{f3}=794\ k\Omega \quad (13)$$

$$R_{c1} = \frac{2\pi * f_{cross} * L * C * V_{osc}}{V_{in} * C_{f3}} = 2.271 \ M\Omega \quad (14)$$

$$V_{osc}: \ ramp \ voltage \ magnitude$$

$$C_{c1} = \frac{1}{2\pi * R_{c1} * f_{z1}} = 4.84 \ pF \quad (15)$$

$$C_{c2} = \frac{1}{2\pi * R_{c1} * f_{p3}} = 159.7 \ fF \quad (16)$$

$$R_{f1} = R_{f2} = 1 \ M\Omega \ for \ precise \ matching$$

Grounds for selecting the frequency of each pole and zero is summarized in Table. I.

TABLE I. Grounds for the frequency of poles and zeros

| Frequency | Grounds |
|---|---|
| $f_{z1}$ | Compensating DC pole |
| $f_{z2}$ | Compensating a pole of the LC filter |
| $f_{p2}$ | Cancelling the ESR zero |
| $f_{p3}$ | Attenuating frequency components higher than the half of the switching frequency |
| $f_{cross}$ | Suppressing output voltage ripple |

*C. Ramp & Clock Generator*

On-chip ramp & clock generator is utilized in this work. The generator receives three external DC voltages that define the frequency of generated ramp and clock signals.

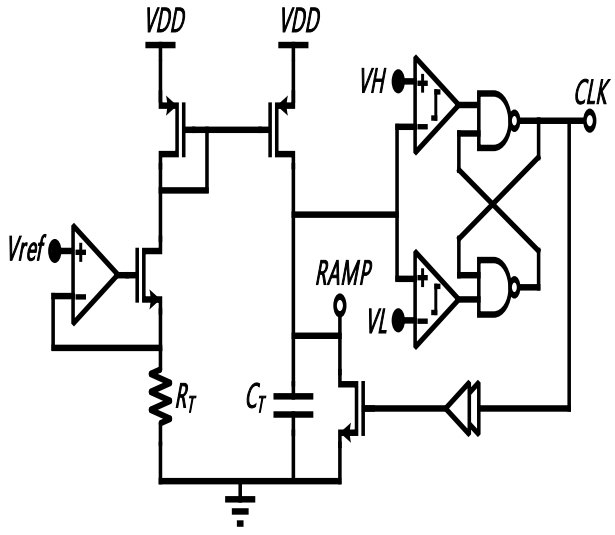


Fig. 4 Structure of ramp & clock generator

In Fig. 4 the schematic of the ramp & clock generator is given [6]. After start up, $V_{ref}$ is assigned across $R_T$ and current defined by the resistor is mirrored to another branch. That current charges $C_T$ and rising ramp signal is generated. When ramp signal exceeds voltage *VH*, *CLK* is set to logical high. Then an nMOS transistor turns on and discharges $C_T$ until it goes below *VL*. As soon as discharging phase finishes the nMOS transistor is turned off and subsequent charging phase follows.

The frequency of ramp and clock signals can be approximated as,

$$f_{sw} = \frac{V_{ref}}{(V_H - V_L) * C_T R_T} \quad (17)$$

Parameters are chosen to simplify calculations.

TABLE II. Parameters for ramp and clock signals

| Parameter | Value |
|---|---|
| $V_{ref}$ | 1 V |
| $V_H$ | 2.5 V |
| $V_L$ | 0.5 V |
| $C_T$ | 5 pF |
| $R_T$ | 100 kΩ |
| $f_{sw}$ | 870 kHz |

Strength of nMOS and pMOS transistors decides the speed of charging and discharging $C_T$. The strength is designed to set the time ratio of ascending and descending as 91.2:8.8. This is a dominant factor of the duty-cycle range of the buck converter. Since this work targets output voltage lower or equal to 3 V with the input of 3.3 V, maximum duty-cycle of the converter is limited to 91.2% whereas lower bound of it is 8.8%. To push the range further, wider transistors are needed.

*D. Dead-Time Generator*

In a buck converter, pMOS and nMOS switches toggle in complementary manner. Ideally the switches change their state instantly, but they spend some time to change in practical cases. If the on-state of nMOS and pMOS transistors coincide then shoot-through current flows directly from VDD to VSS. The rush of current can be observed as a sharp spike and that degrades the overall efficiency of the buck converter. Therefore, there should be a way to force a switch to be toggled only after turning off the previously on-state switch.

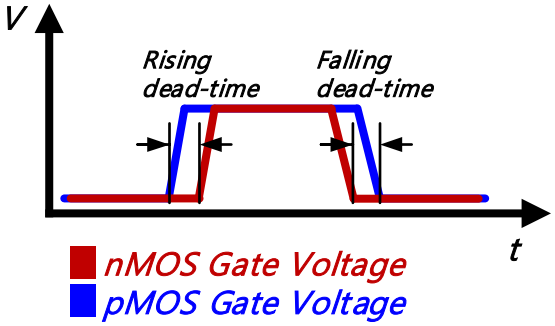


Fig. 5 Definition of dead-time

The amount of time interval between the state transition of a high-side switch and a low-side switch is defined as dead-time. It should be noted that if dead-time is too short then partial shoot-through current will flow whereas body diode of the nMOS transistor will be a conduction path for the inductive current that has been flowing if dead-time is too long. Without the transition of the pMOS transistor, output voltage of buck converter will continue to fall.

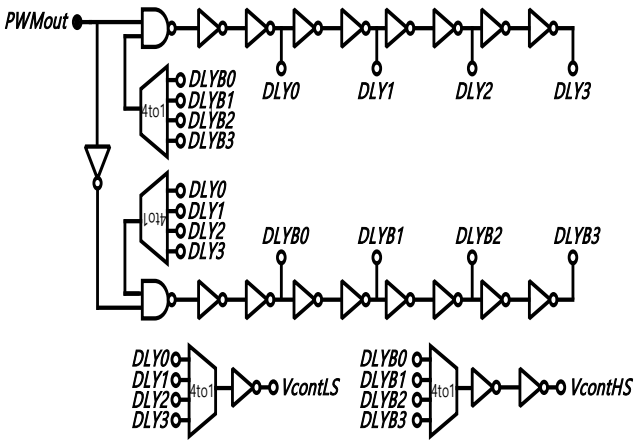


Fig. 6 Structure of dead-time generator

Fig. 6 shows the structure of the dead-time generator. 4-to-1 multiplexers are controlled by a 2-bit external input SEL, realized by two single-put-double-throw switches soldered on a testing printed circuit board (PCB). Dead-time of gate driving signals is the number of inverter stages multiplied by propagation delay. Dead-time can be controlled within the range from 1.7 ns to 4.9 ns by selecting the number of inverter stages with external digital input.

TABLE III. List of available dead-times

| SEL<1> | SEL<0> | Rising dead-time [ns] | Falling dead-time [ns] |
|---|---|---|---|
| *0* | *0* | 1.78 | 1.96 |
| *0* | *1* | 2.88 | 3.06 |
| *1* | *0* | 3.98 | 4.16 |
| *1* | *1* | 4.89 | 5.07 |

## III. RESULTS AND DISCUSSIONS

Chip micrograph is shown in Fig. 7. Dummy metal blocking layer was applied to the PWM module, the ramp and clock generator, the dead-time generator, a bias circuit, and a high-side gate driver.

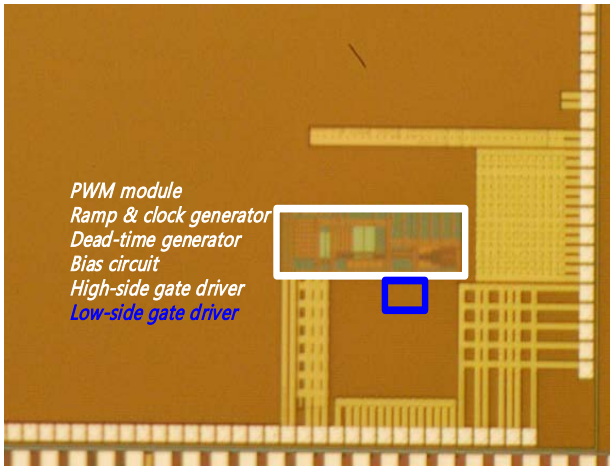


Fig. 7 Chip micrograph

Some off-chip components were used to configure a testing PCB. A list of components is shown in Table IV. An aluminium electrolytic capacitor is used to minimize output voltage ripple by reducing ESR.

TABLE IV. List of off-chip components

| Components | Value/ Usage |
|---|---|
| *LT3042* | Off-chip low dropout regulator |
| *SMD inductor* | 10 uH/ LC filter |
| *Aluminium electrolytic capacitor* | 6.8 uF/ LC filter |
| *IRLZ24N* | Off-chip power MOSFET/ Load-controlling transistor |

* SMD: Surface-Mount Device

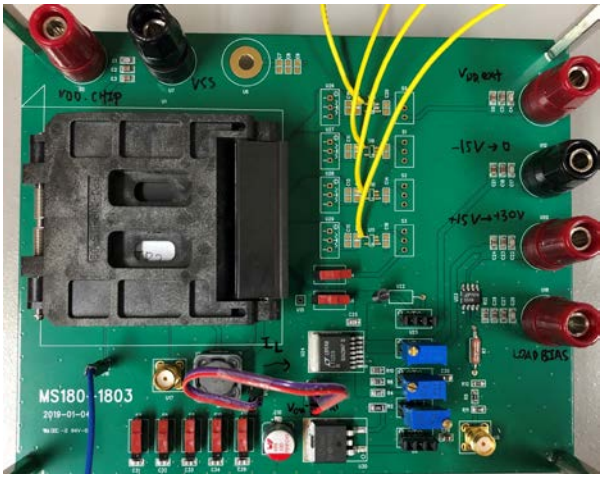

Fig. 8 Configuration of the testing PCB

Two-bit input of the dead-time generator was toggled to check the difference. However, calculated output power based on measured results showed almost no difference which was 542.7 mW in 300 mA constant load. Considering possible measurement error, the minimum and maximum dead-time did not make noticeable difference to efficiency.

Inductor current in no load condition is measured with a current probe and a digital phosphor oscilloscope. DC coupled output voltage and inductor current is illustrated in Fig. 9. The frequency of inductor current is 877.2 kHz, which is in phase with the internally generated ramp and clock signal. Average output voltage is 1.81V.

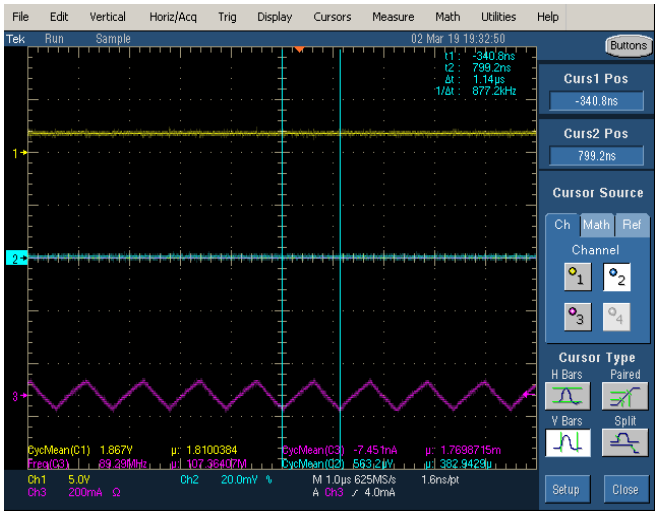


Fig. 9 Measurement result of no load condition

Inductor current in 100 mA constant load condition is measured and the result is plotted in Fig. 9. AC coupled output voltage ripple is measured to stay in a 5.2 mV voltage window.


Fig. 10 Measurement result of 100 mA constant load condition

In Fig. 11, power conversion efficiency (PCE) is calculated and plotted based on measured results. Load current is swept from 0 to 1.57 A. Maximum PCE is 94.38 % when the load current is 150 mA. PCE in high-load current condition fell below 90 % because there are some undesired parasitic resistances in testing PCB configuration. A pair of short jump wires was used to connect the LC filter inductor and capacitor, which made it easy to install a current probe.

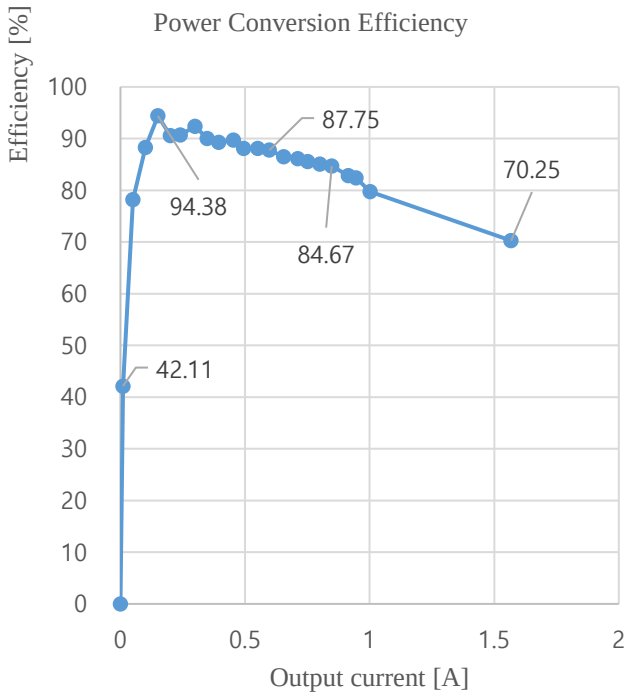


Fig. 11 Plot of PCE versus output current

Load transient test from 100 mA to 300 mA is measured. The result is shown in Fig. 12. Square wave signal is applied to the gate of an off-chip power MOSFET to make a load transition. Frequency of the square wave signal is 2 kHz and rising time and falling time is both 1 ns. Average output voltage is 1.816 V and average output current is 195.11 mA.

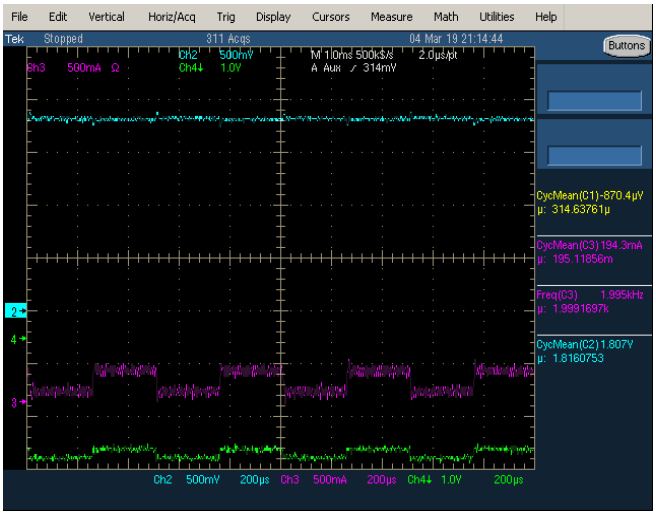


Fig. 12 Measurement result of a load transient condition from 100 mA to 300 mA

AC coupled output voltage is measured in the same load

TABLE V. Comparison table

| | [7] | [8] | This work |
|---|---|---|---|
| Technology | TSMC 0.35 um | 0.18 um | Magnachip 0.18 um |
| Control mode | Hysteresis & dynamic frequency | Hysteresis & PFM | PWM |
| Input voltage | 2.7 ~ 4.2 V | 2.7 ~ 3.3 V | 3.3 V |
| Output voltage | 2 V | 1.2 V | 1.8 V |
| Inductor | 10 uH | 1.2 uH | 10 uH |
| Capacitor | 20 uF | 22 uF | 6.8 uF |
| Load current range | 20 m ~ 600 mA | 10 m ~ 500 mA | 50 m ~ 1 A |
| Switching frequency | 50 k ~ 1.38 MHz | 9.7 k ~ 250 kHz (light load)<br>1.97 MHz (heavy load) | 870 kHz |
| Load transient | 8.26 us (100 mA to 600 mA)<br>7.44 us (600 mA to 100 mA) | 3.7 us (500 mA to 10 mA) | 8.56 us (100 mA to 300 mA)<br>17.44 us (300 mA to 100 mA) |
| Overshoot/ undershoot | 79 mV/ 67 mV | 2.5 mV | 68 mV/ 60.8 mV |

transient condition to measure overshoot and undershoot. Fig. 13 and Fig. 14 display cursors on an overshoot situation and an undershoot situation, respectively. Measured values are listed in Table VI.


Fig. 13 Measurement result of output voltage overshoot

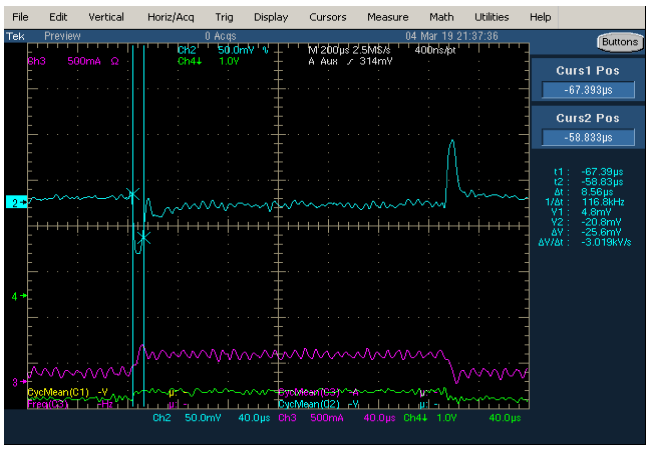


Fig. 14 Measurement result of output voltage undershoot

TABLE VI. List of measured values in load transient condition

| Average output voltage = 1.81 V | |
|---|---|
| *Overshoot settling time* | 17.44 us |
| *Overshoot magnitude* | 68 mV |
| *Undershoot settling time* | 8.56 us |
| *Undershoot magnitude* | 60.8 mV |

## IV. CONCLUSION

A voltage-mode PWM controlled buck converter is presented in this paper. A type 3 compensation loop effectively deals with a double pole and an ESR zero caused by an LC filter of the buck converter. The procedure of deciding passive components for the poles and zeros introduced by the compensation loop is fully covered. Internal ramp and clock generator eliminated the needs for external ramp and clock input. Operating frequency can be controlled by modifying applied DC voltage to the generator. To resolve shoot-through current problem, a dead-time generator is implemented. This work achieved maximum PCE of 94.38 % and overshoot and undershoot settling time 17.44 us and 8.56 us, respectively.

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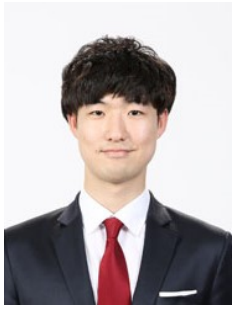

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