Design of On-interposer Active Power Distribution Network for an Efficient Simultaneous Switching Noise Suppression in 2.5D/3D IC

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Abstract - **Dynamic voltage frequency scaling (DVFS) and adaptive voltage frequency scaling (AVFS) are primary methods of conserving power in a microprocessor. By these technologies, a simultaneous switching current (SSC) spectrum drawn by integrated circuits (ICs) varies in frequency domain. However, conventional power distribution network (PDN) is impossible to respond the varying SSC spectrum due to its passive characteristics. In this paper, we propose an on-interposer active PDN to efficiently suppress the simultaneous switching noise (SSN) whose frequency is changing. The on-interposer active PDN is a controllable on-interposer decoupling capacitance scheme with external operation based on monitored SSN voltage. The operation of the proposed on-interposer active PDN is verified through simulations in frequency and time domain.**

I. INTRODUCTION

Recently, the realization of high-speed electrical systems with performance has been a continuous challenge. Two-Dimensional CMOS scaling technology reaches the limits because of the physical and economic problems. For that reason, 2.5-Dimensional (2.5D) integration, based on through silicon via (TSV) and silicon interposer, has gained substantial attention as a promising solution, toward current industrial challenges due to its improved electrical performance and compact design. The TSV technology enables vertical interconnection between vertically integrated circuits (ICs) [1-2]. The silicon interposer technology increases ICs′ integration density with fine pitch metallization. This interposer is introduced as the new component of power distribution network (PDN) in 2.5D IC [3]. Therefore, it becomes important to design an on-interposer PDN to guarantee the performance of the entire system. Also, some active circuits can be fabricated on the silicon interposer using the silicon process integration. This means that the conventional silicon interposer composed of passive components has high potentials with fabrication of additional active devices to enhance the electrical performance considering power integrity issues.

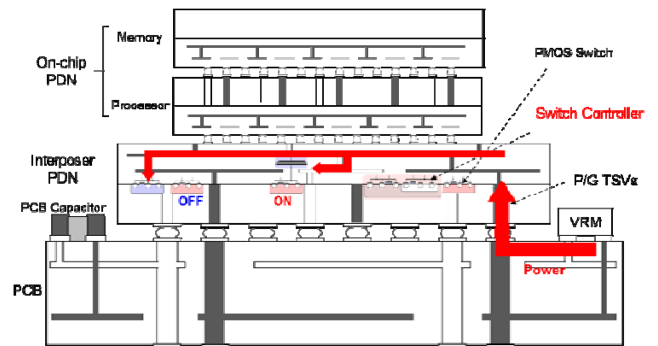

Fig. 1. Structure of on-interposer active power distribution network (PDN) in 2.5D/3D-IC

Lately, switching power consumptions and operating frequency of ICs are rapidly increasing. When active circuits switch simultaneously, a huge amount of current called simultaneous switching noise (SSN) flows through the PDN. SSN with high frequency can drop the supply voltage. This voltage fluctuations caused by the SSN disturb the normal operation of active circuits under the PDN, and degrade the electrical performance such as timing uncertainty. As a result, power integrity has become one of the most critical issues. For the SSN suppression, electromagnetic band-gap (EBG) structure or broad-band PDN design has been proposed [2].

In 2.5D IC, package inductance and on-interposer capacitance form parallel resonance that generates high PDN impedance peak. If the frequency of switching current is within the resonance frequency range of the PDN impedance, the SSN increases [3]. In the case of multi-core processor, controls their core speed and the number of activated core. This means that the frequency of the SSN current can be changed at any time. Therefore, it is highly possible that the fundamental or harmonics of the SSN current can be matched with the resonance frequency of the PDN. A conventional PDN composed of passive components cannot change its impedance according to the varying frequency of the SSN current. For the conventional PDN, the hierarchical PDN design considering all of the

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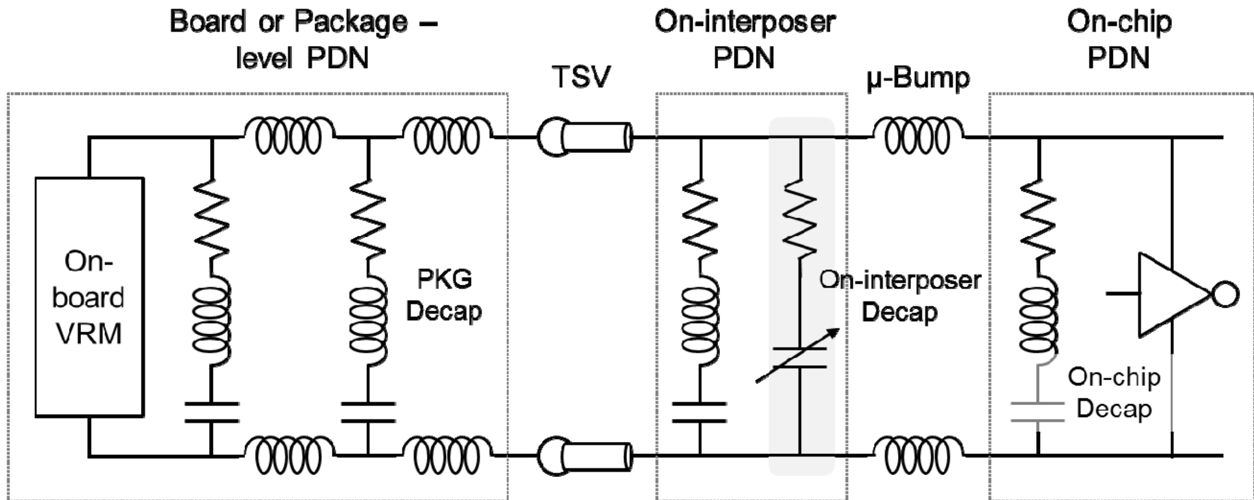

Fig. 2. Structure of on-interposer active power distribution network (PDN) in 3D-IC

possible switching current spectrum is necessary. But, it is difficult to design due to the limitations of area and cost. For that reason, a new PDN scheme, which can change its impedance, is required.

In this paper, we propose an on-interposer active PDN that has an optimal on-interposer decoupling capacitance control scheme for the SSN suppression in 3D-IC. The proposed on-interposer active PDN is an on-interposer PDN with controllable on-interposer decoupling capacitors (decaps). Each on-interposer decaps has a p-type metal-oxide-semiconductor (PMOS) transistor that can be controlled externally by hands using a toggle switch mounted on the printed circuit board (PCB). The on-interposer decoupling capacitance is externally changed to reduce the SSN in 3-D IC based on the monitored SSN voltage of the on-interposer PDN. The proposed on-interposer active PDN is successfully verified through the SSN simulated results in frequency and time domain. It is confirmed that the SSN in 3-D IC is suppressed by changing the proposed, externally controllable on-interposer decoupling capacitance.

II. EXPERIMENTS

The block diagram of on-interposer active PDN in 3-D IC is shown in Fig. 3. The proposed on-interposer active PDN is composed of conventional on-interposer, and array of on-interposer decaps with PMOS switches.

A simplified PDN model of on-chip, on-interposer, and off-chip is shown in Fig. 2. The off-chip PDN model of package contains package inductance and decap model with equivalent series resistor (ESR). Also, the on-interposer PDN is modeled by on-interposer decap with PMOS switches. The simulated self-impedance of an example PDN with the switched on-interposer capacitors is observed at on-interposer PDN. There is a parallel resonance caused by both the off-chip inductance and the on-interposer capacitance of on-interposer decaps.

Although the package or board is well designed to have tits inductance low enough, the parallel resonance between

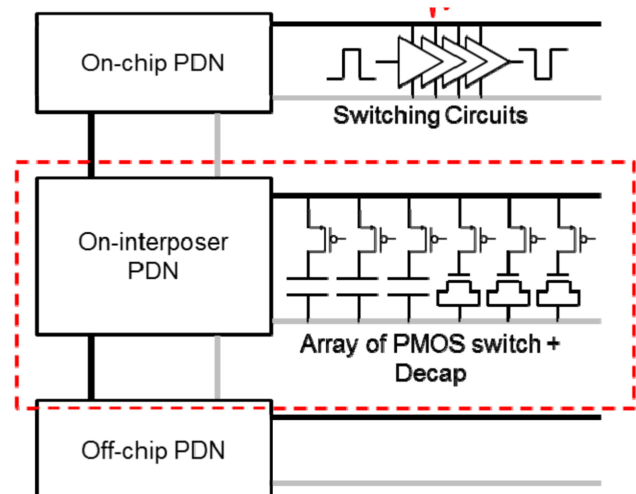

Fig. 3. (a) Block diagram and (b) simplified model of on-interposer active power distribution network.

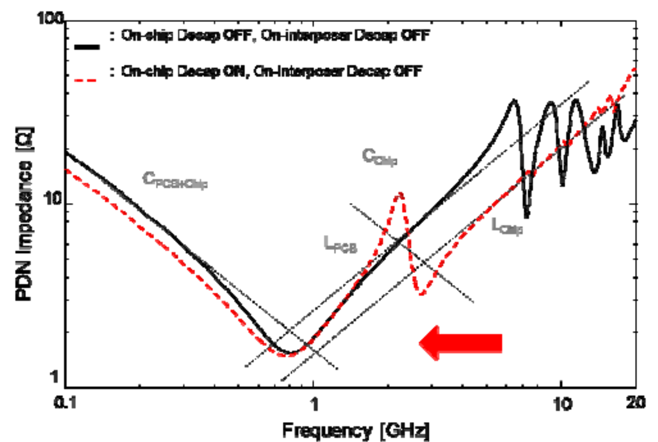

Fig. 4. Structure of on-interposer active power distribution network (PDN) in 3D-IC.

the off-chip inductance and the on-interposer capacitance cannot be avoided. Because of the resonance, the impedance of PDN is high at the resonance frequency. And if the switching frequency of the active circuits is close to the resonance frequency, enormous SSN is generated. As on-

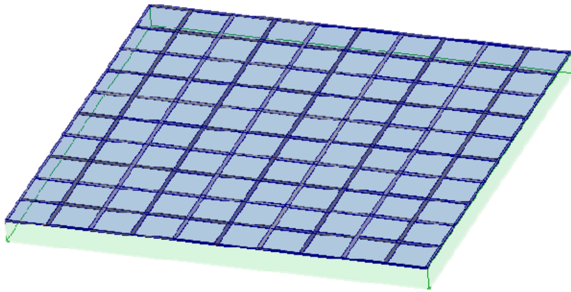

Fig. 5. 3-Dimensional view of on-interposer power distribution network.

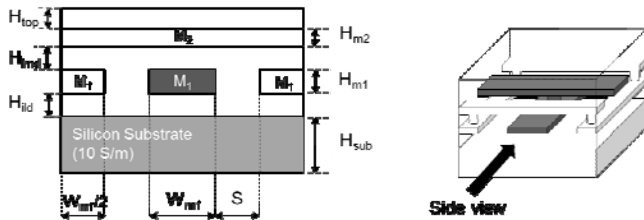

Fig. 6. Cross-section view and dimension parameters of unit cell of on-interposer power distribution network.

interposer decoupling capacitance changes, the resonance frequency is shifted. Using this scheme, it is possible to make the self-impedance at switching frequency lower by shifting the resonance frequency far away from switching frequency.

To change the on-interposer decoupling capacitance, the PMOS switches are connected to each on-interposer decap. For the on-interposer decaps, both n-type metal-oxide-semiconductor (NMOS) capacitors and poly-insulator-poly (PIP) capacitors are used. These on-interposer decaps are switched by external control. As real-time monitoring the simulated result of peak-to-peak SSN voltage changes the bias voltage of PMOS switch array to switching the on-interposer decaps.

A. Structures and Dimensions of On-interposer Power Distribution Network

The structure of an on-interposer PDN is shown in Fig. 5. The conventional on-interposer PDN is meshed type and its detailed dimension is in Table. I. To analyze the conventional PDN in frequency-domain, the RLGC modeling of the conventional PDN which showed highly correlated with 3D EM full simulator of ANSYS is completed. Also, on the PDN of interposer had pads that SSN on the PDN can be measured by directly probing on the PDN.

B. On-interposer Decoupling Capacitors

To control the on-interposer decoupling capacitance, we used NMOS capacitors and PIP capacitors. By the design rule of HYNIX 0.35um, design of a 1pF of cell-based decoupling capacitor array is used for the controllable on-interposer decoupling capacitors. The range of the controllable on-interposer decoupling capacitor is 1pF to 9pF using a conventional on-interposer decap and 8 controllable on-interposer decaps.

TABLE I.
Physical Dimensions of the On-interposer Power Distribution Network

Parameters	Symbol	Value
Height of top insulator layer	H_{top}	1.2um
Height of middle insulator layer	H_{imd}	0.85um
Height of bottom insulator layer	H_{ild}	4.08um
Height of M_1 Metal	H_{M1}	0.7um
Height of M_2 Metal	H_{M2}	0.7um
Height of substrate	H_{sub}	50um
Width of M_1 metal	W_{M1}	10um
Width of M_2 metal	W_{M2}	10um
Space between power line and ground line on M_1 and M_2 metals	S	90um
Length of on-interposer power distribution network unit cell	L_{unit}	200um

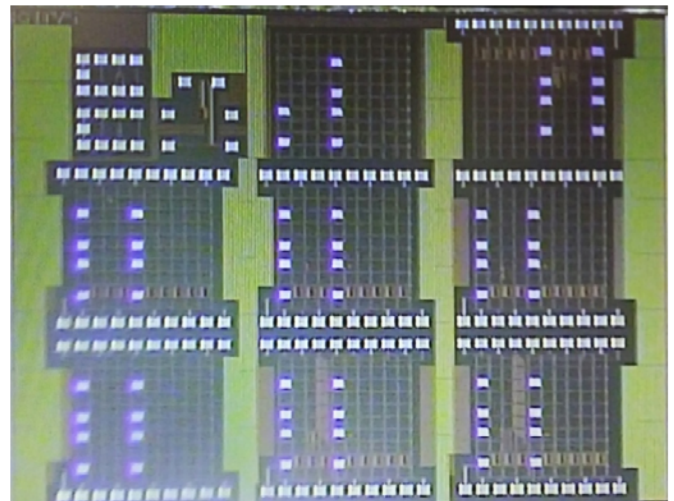

Fig. 7. Photograph of test vehicle for on-interposer active PDN scheme.

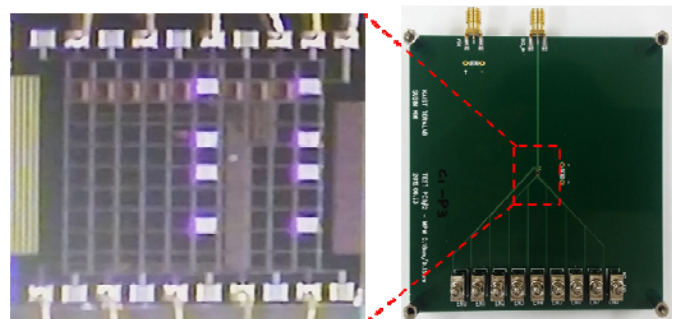

Fig. 8. Structure of on-interposer active PDN implemented in a 0.35um HYNIX CMOS process.

C. PMOS Switch

To control the on-interposer decoupling capacitance, PMOS switches are used. The PMOS switches are connected between the PDN and on-interposer decaps. The gate voltage of the PMOS switches is biased by external input signals. As a switch, n-type MOS switch can be used, but it has threshold voltage drop between VDD of the PDN and the on-interposer decaps. To connect the on-interposer decaps to the PDN without no voltage drop, we used PMOS switches.

D. Switching Inverters Design for Simultaneous Switching Noise Generation

To show the feasibility of the on-interposer active PDN, an inverter array was designed as a noise generator on the PDN. By external input signaling to the inverter array, it generated SSN on the PDN with characteristics of the input signals such as clock, input output (I/O) signal, or rush current by power gating. And we analyzed the noise immunity of the on-interposer active PDN under the switching frequency variance of the inverter array.

E. Design and Implementation

The test vehicle and assembled interposer on board of the proposed on-interposer active PDN are shown in Fig. 7 and Fig. 8. The assembled interposer on board is to supply the power on the PDN and to mount the on-board switches for biasing the on-interposer PMOS switches.

1) The switching frequency current per I/O pin = 10 mA
2) Operating frequency = 1.6 Gbps
3) Driver size of PMOS/NMOS = 20 um / 10 um

Total number of simultaneously switching inverters = 8

III. RESULTS AND DISCUSSION

In this chapter, RLGC model of the proposed scheme fabricated on the test interposer is compared with the PDN impedance result of measurement and 3D EM simulation. Using this RLGC model, the operation of the proposed on-interposer active PDN is verified with series of frequency and time domain simulations.

A. Verification of RLGC model of the proposed on-interposer active PDN

The self-impedance of the PDN is the most important parameter that shows the characteristic of the PDN. The self-impedance of the design of the proposed on-interposer active PDN obtained from the measurement, 3D EM simulation and RLGC model is showed in Fig. 9. From the results, the result of the RLGC model shows a good correlation with the result of measurement and 3D EM simulation.

B. Verification of the proposed on-interposer active PDN using simulations

The proposed on-interposer active power distribution network (PDN) scheme with switched on-interposer decoupling capacitors for an efficient SSN suppression was

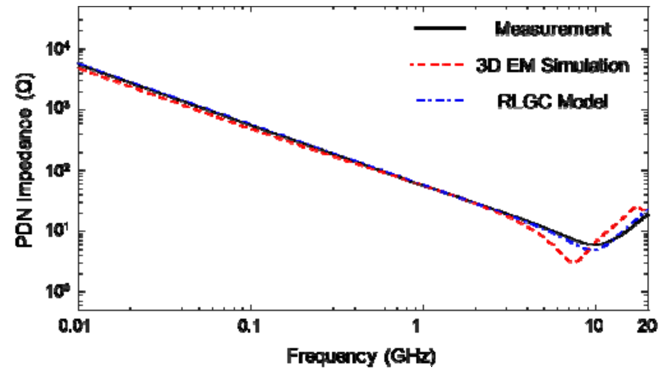

Fig. 9. Self-impedance of the test interposer obtained from the measurement, 3D EM simulation and RLGC model. The PDN impedance of the RLGC model is well-matched with the PDN impedance of measurement and 3D EM simulation.

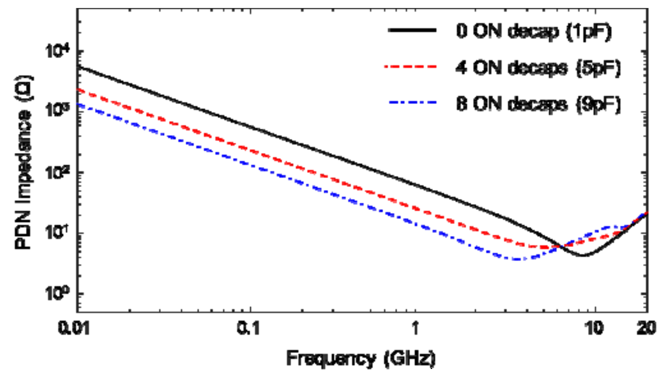

Fig. 10. Measured self-impedance of the test interposer with respect to the variation in the number of switched-on decaps on the test interposer.

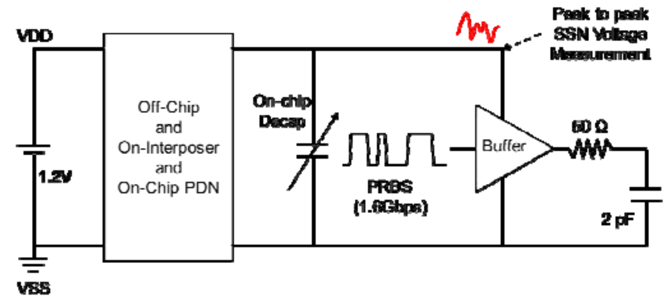

Fig. 11. ADS simulation setup of On-interposer Active Power Distribution Network for an Efficient Simultaneous Switching Noise in 2.5D/3D-IC.

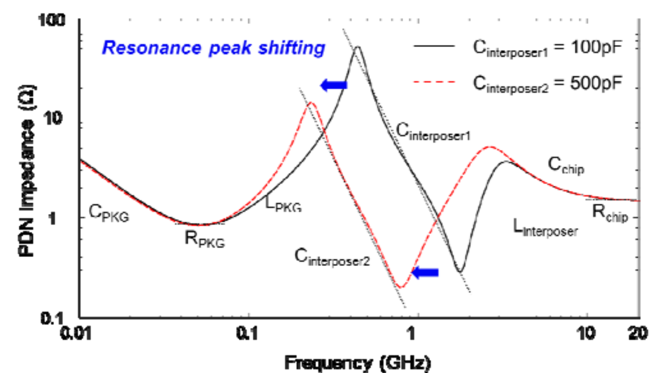

Fig. 12. Measured self-impedance of test vehicle of the proposed on-interposer active PDN as switching condition of on-interposer decap array.

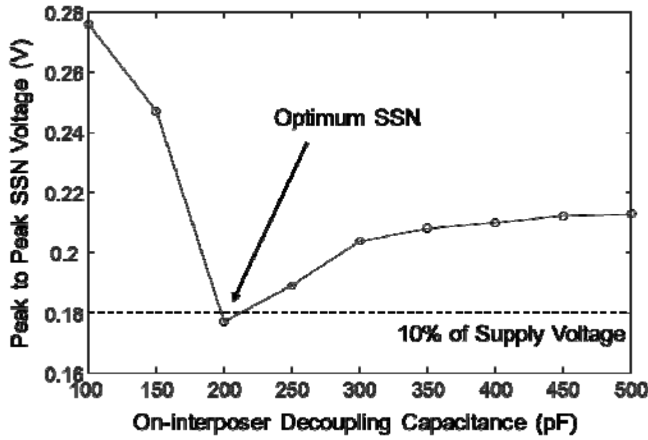

Fig. 13. Pk-to-pk SSN voltage variation according to on-interposer decoupling capacitance. The optimum SSN point is shown when the on-interposer decoupling capacitance is 200pF.

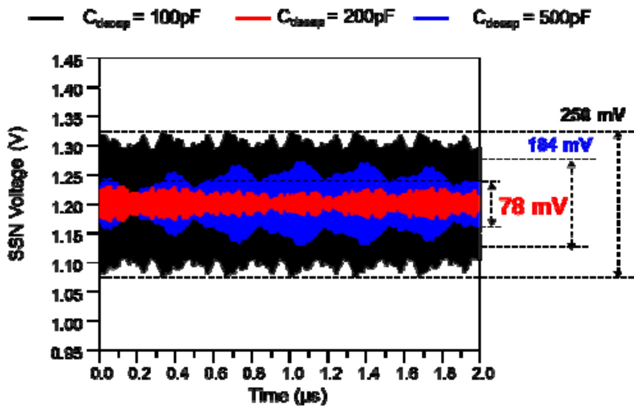

Fig. 14. Simultaneous switching noise voltage waveform generated by on-chip inverter array according to on-interposer decoupling capacitance.

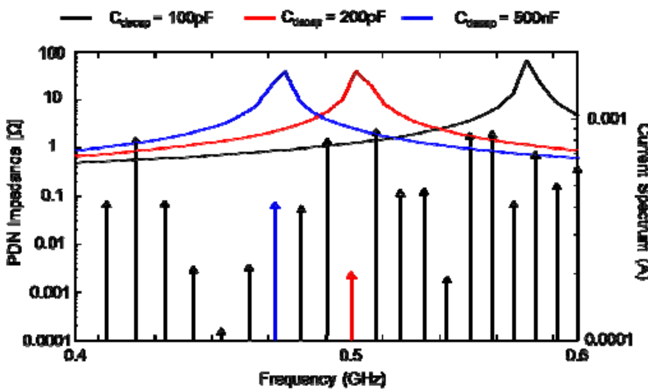

Fig. 15. Power distribution network impedance of designed 3D-IC and current spectrum of input signal of inverter array.

simulated and analyzed. We simulated the PDN impedance and simultaneous switching noise (SSN) voltage waveform right on the switching circuits. When the on-interposer decoupling capacitance varied, the PDN impedance curve also changed as shown in Fig. 12. The frequency at $L_{off_chip}C_{on\text{-}interposer}$ resonance shifted as increased on-interposer decoupling capacitance (C_{decap}).

Peak to peak (Pk-to-pk) SSN voltage which is fluctuation of supply voltage on switching circuits was simulated and measured by varying the on-interposer decoupling capacitance from 100pF to 500pF. The frequency of input clock of switching circuits was set to 400MHz, and the rising and falling time of input clock was set to 10% of its period. As shown in Fig. 13, The Pk-to-pk SSN voltage changed with the variation of on-interposer decoupling capacitance. The worst Pk-to-pk SSN voltage is occurred at 100pF, and the optimum value of the on-interposer decoupling capacitance is 200pF where shows the least Pk-to-pk SSN voltage. For 400MHz of clock frequency, the on-interposer decoupling capacitance should have been 200pF to supply stable VDD.

Fig. 14 shows the supply voltage waveforms of VDD with the worst case and optimum case of the on-interposer decoupling capacitance. When the on-interposer decoupling capacitance was 100pF, the Pk-to-pk SSN voltage was 280mV which is 15.5% of VDD. For the 200pF of on-interposer decoupling capacitance, the SSN voltage waveform was optimized so that the Pk-to-pk SSN voltage was under 10% of VDD. This result can be analyzed in Fig 15. Both of self-impedance of PDN and the switching current spectrum are depicted in Fig. 15 together. The current spectrum at the resonance peak of each PDN curve has the largest value when the C_{decap} is 100pF, and the smallest value when the C_{decap} is 200pF, respectively. This means that the resonance peak of PDN impedance curve should avoid the large current spectrum to suppress the SSN.

Using this on-interposer active PDN, an optimum on-interposer decoupling capacitance for each clock frequency can be achieved. It can make the PDN be able to respond actively to varying clock frequency. With a limited budget of decap, a conventional PDN has limitations to suppress a broadband SSN. But the active PDN can suppress the broadband SSN in 2.5D/3D IC efficiently compared to the conventional PDN.

IV. CONCLUSIONS

In this paper, an on-interposer active PDN was proposed for an efficient SSN suppression. The proposed on-interposer active PDN was successfully verified through the simulated results in frequency and time domain. The proposed on-interposer active PDN operated adaptively based on frequency-domain analysis of switching current and PDN. It is confirmed that the on-interposer resonance, caused by the off-chip inductance and the on-interposer decoupling capacitance, is shifted by changing the proposed externally controllable on-interposer decoupling capacitance. We have demonstrated that the on-interposer decoupling capacitance for the optimum SSN Pk-to-pk voltage is successfully obtained by using the proposed on-interposer active PDN. In the future, SSN sensing circuit and on-interposer decoupling capacitor controller will be implemented to operate the on-interposer active PDN adaptively and automatically.

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His current research interests include power integrity issues in power distribution network (PDN) in 3-D IC and on-interposer adaptive PDN design.

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