Dual-Mode Noninverting DC-DC Buck Converter for Wearable AMOLED Display

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Abstract **− This paper proposes a highly integrated dual-mode noninverting DC-DC buck converter for wearable AMOLED display panels. The DC-DC buck converter is designed to increase power efficiency under light load using PWM-SPWM (set-time variable pulse width modulation) dual-mode. The major role of the PWM-SPWM controller is to switch frequency according to the load current by changing only the set signal using the VCO (voltage controlled oscillator) in the conventional PWM control signal. The converter generates variable output voltages by changing reference voltage of error amplifier. The proposed circuit has been designed using a 0.35 μm standard CMOS process and its core area of 1.2 mm x 1.3 mm. The measurement results show that the proposed circuit has power efficiency of 65% ~ 75% with output voltage of 2.0 V ~ 2.7 V for a load current range of 5 mA ~ 50 mA and input voltage 3.3 V ~ 4.2 V.**

Keywords**— AMOLED, buck converter, DC-DC converter, dual-mode, PWM**

I. INTRODUCTION

The market of portable devices such as cellular phones, PDAs, video game consoles, and wearable watches has been rapidly expanding and this trend has led to a large emerging market for switching power ICs [1]. Because of the switching power IC's high efficiency, small size, and low power consumption, it is suitable to be a power supply model for mobile devices [2-7]. Especially since mobile devices left in the standby mode have long usage time, the power efficiency of switching power IC under light load is a crucial factor for selecting the power supply circuit. [6-7]. An AMOLED display panel requires two supply voltages, a positive voltage and a negative voltage [8]. High power efficiency and being able to vary output voltage in the DC-DC converters are the two most important aspects for positive voltage.

In this paper, a noninverting DC-DC buck converter is proposed to increase power efficiency in PWM-SPWM dual-mode. The converter has variable output voltages by changing reference voltage of error amplifier. This paper is organized as follows. Design methodology of a DC-DC buck converter is presented in Section II. Measurement results of the proposed DC-DC converter are described in Section III. Conclusions are finally drawn in Section IV.

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II. DESIGN OF DC-DC BUCK CONVERTER

We design a PWM-SPWM dual-mode DC-DC buck converter with variable positive output voltage for low power wearable AMOLED display panel. The dual-mode DC-DC converter operates in the PWM mode under heavy load, and in the SPWM mode under light load in which the switching frequency of the set-time is changed in proportion to the load current in the PWM mode. Table I shows the major design specifications of the proposed DC-DC buck converter. For an input voltage of 3.3 V to 4.2 V, the DC-DC buck converter has an output voltage of 2 V to 2.7 V. Figure 1 is the block diagram of the proposed DC-DC converter for a positive voltage V_{POS} of wearable AMOLED display panel. In the DC-DC converter for V_{POS}, a PWM-SPWM dual-mode is adopted to achieve high power efficiency. The converter operates in the current mode control (CMC) when the output voltage and the inductor current are fed back and the output voltage is constant. The converter includes an error amplifier that compares the feedback voltage with the reference voltage to amplify the error with the target output voltage, a current

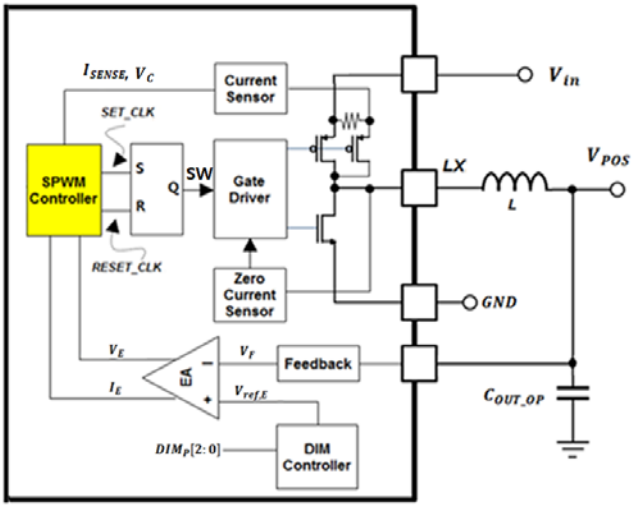


Fig. 1. Block diagram of the proposed DC-DC buck converter

sensor that detects the inductor current, a zero current detector that detects the reverse current of the inductor and a PWM-SPWM controller that adjusts switching frequency or pulse width according to load current, as well as a gate driver that controls on/off of the power switching transistors.

TABLE I
Specifications of the proposed DC-DC buck converter.

Item	Specification
Process	0.35 μm CMOS
Input voltage	3.3 V ~ 4.2 V
Output voltage	2 V ~ 2.7 V
Load current	5 mA ~ 50 mA
Frequency	0.15 MHz ~ 1.4 MHz
Output voltage ripple	< 5 mV
External inductor	4.7 μH

A. PWM-SPWM controller

The major role of the PWM-SPWM controller is to switch frequency depending on the load current by changing only the set signal through the VCO in the conventional PWM control signal. This controller is a switching control circuit to reduce the power loss under light load by generating a switching frequency proportional to the load under light load. Fig. 2 illustrates the proposed PWM-SPWM controller. The VCO generates a set signal V_{VCO_ref} whose frequency is varied by an error voltage V_E that changes with the load current. Also, a set signal V_{comp_set} generates a fixed switching frequency. A mode selector composed of two flip flops chooses a signal with a low frequency, and a set signal V_{setclk} is generated. The current comparator compares the inductor current I_{SENSE} with the sum of the ramp waveform I_{RAMP} and the error voltage V_E to generate the reset clock $V_{resetclk}$. Set clock V_{setclk} and reset clock $V_{resetclk}$ are applied to the SR latch to generate the control signal for the power switching transistor.

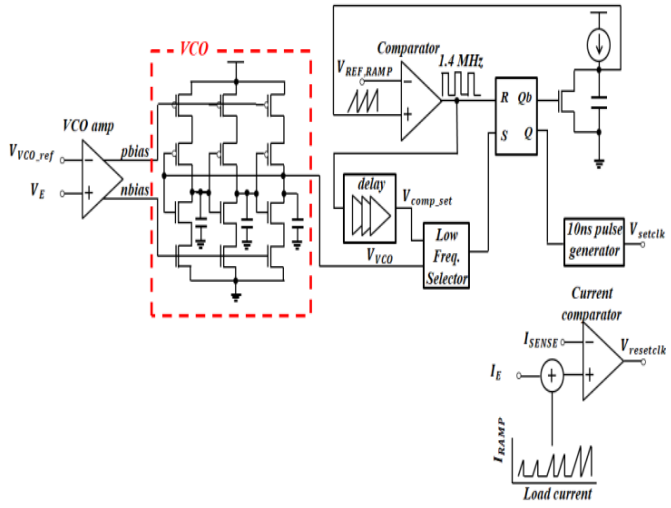


Fig. 2. Proposed SPWM controller.

The proposed PWM-SPWM controller requires only a simple low frequency selector to operate dual-mode. So, it can be implemented in a small area, and since it has a set signal periodically, its ripple voltage is smaller than PSM.

Fig. 3 shows the SPWM waveform of the buck converter. Under a light load of less than dual- mode switching load current I_{MC} (max current), the set clock V_{setclk} senses the output voltage V_E of the error amp, and the reset clock $V_{resetclk}$ senses the inductor current through the current sensor so that the switching frequency is modulated in proportion to the load current. Under a heavy load larger than load current I_{MC}, the set clock V_{setclk} is generated with a constant maximum frequency irrespective of load current, so that the switch signal SW operates in the PWM mode with constant frequency.

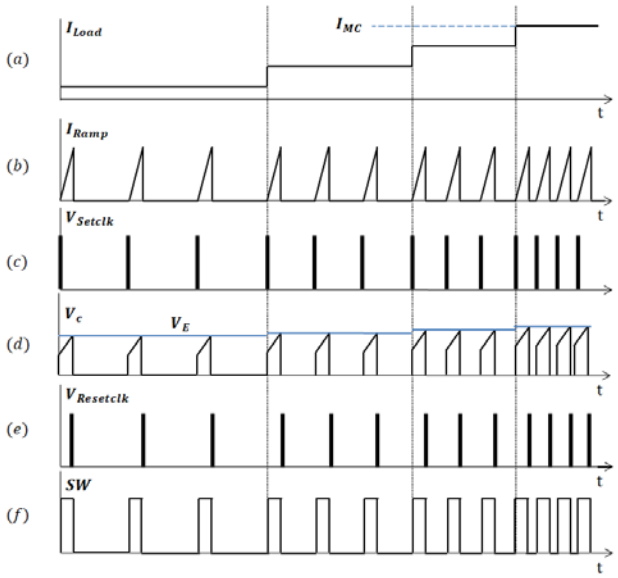


Fig. 3. Waveform of SPWM method (a) Load current I_{MC} , (b) Ramp current I_{Ramp}, (c) Set clock signal V_{setclk}, (d) Current sensing voltage V_C and error amplifier voltage V_E, (e) Reset clock signal $V_{resetclk}$, (f) Switching pulse SW.

B. Variable output voltage

Fig. 4 shows a variable output voltage circuit for V_{POS}. The V_{POS} is determined by the ratio of the feedback resistor and reference voltage VREF_P as shown in equation (1).

$$V_{POS} \times \frac{R_B}{R_A+R_B} = \text{VREF\_} \quad (1)$$

The output voltage is adjustable by changing the reference voltage VREF_P of the error amplifier with resistors and a multiplexer according to external control signals DIM_P[2:0]. According to external control signals, 8 reference voltages are generated as shown in TABLE II to determine output voltage.

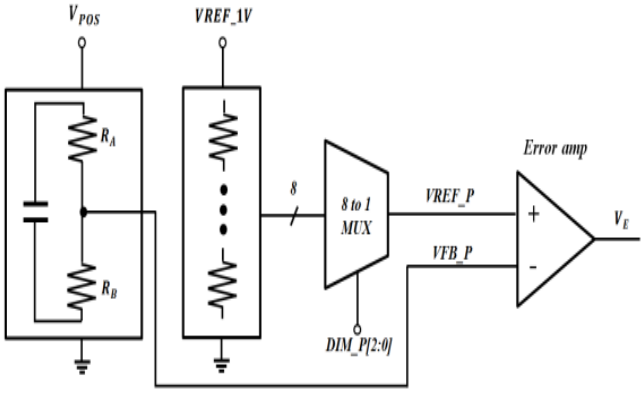


Fig. 4. Variable output voltage circuit for V_{POS}.

TABLE II. Variable output voltages by external control signals DIM_P[2:0].

DIM_P[2:0]	V_{POS} [V]
000	2.0
001	2.1
010	2.2
011	2.3
100	2.4
101	2.5
110	2.6
111	2.7

III. MEASUREMENT RESULTS

DC-DC buck converter which proposed in Section II has been designed through a 0.35 μm CMOS standard process. Fig 5 shows the chip photograph of the proposed converter whose chip area is 1.2 mm × 1.3 mm.

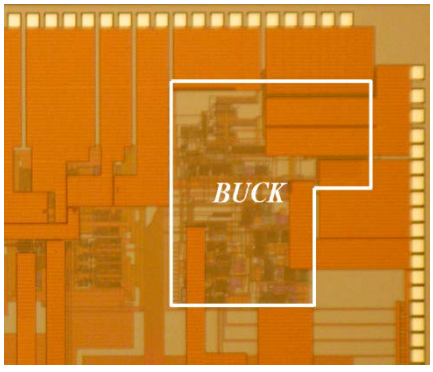
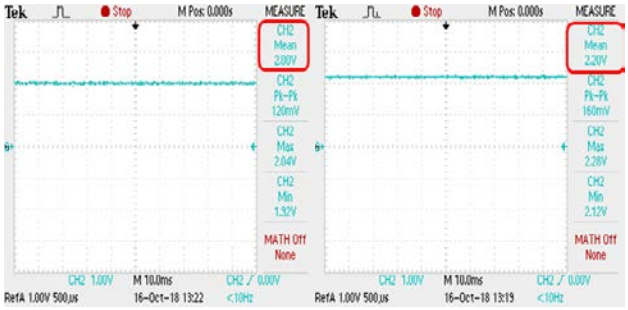
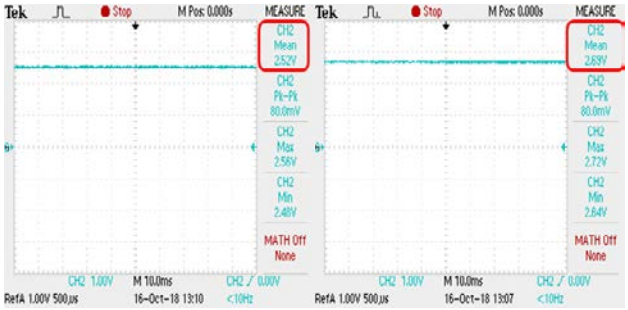


Fig. 5. The photograph of the proposed DC-DC buck

Fig. 6 demonstrates the output voltage of buck converter by external control signals DIM_P[2:0]. It can be seen that the output voltage varies from 2.0 V to 2.7 V according to the external control signal as shown in TABLE II.

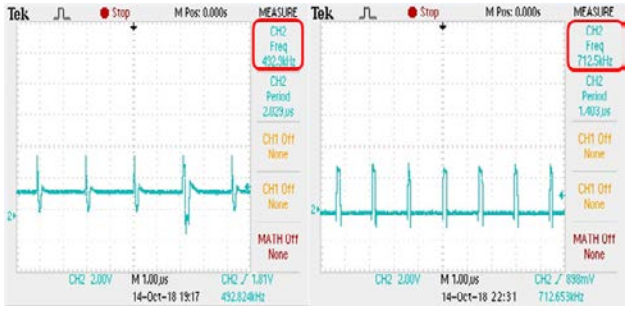


(a) 2.0V (b) 2.2V



(c) 2.5V (d) 2.7V

Fig. 6. Output voltage of buck converter by external control signal DIM[2:0]. (a) DIM[2:0] = 000, (b) DIM[2:0] = 010, (c) DIM[2:0] = 101, (d) DIM[2:0] = 110.



(a) 492 kHz @ 10 mA (b) 712 kHz @ 20mA

(c) 1.027 kHz @ 40 mA (d) 1.043 kHz @ 50mA

Fig. 7. The PWM-SPWM switching frequency according to load current.

Fig. 7 shows the PWM-SPWM switching frequency of external inductor LX according to load current. The switching frequency varied from 492 kHz to 1.04 MHz for load currents of 10 mA ~ 50 mA.

Fig. 8 shows power efficiency according to load current. (b) is a simulation result using only the previous PWM mode and (a) shows a simulation result on dual-mode. The result (a) has 8% more efficient than (b). (c) shows a measured result using dual-mode with power efficiency of 65.5% ~ 77.3% under loads of 5 mA ~ 50 mA. However, the power efficiency of (c) is 16% lower than that of (a) because of several factors of power dissipations. First one is latch-up phenomenon. It causes leakage current of parasitic BJT using a standard CMOS process. Leakage current increases the input current. The other is caused by a shoot-through current flowing through the CMOS power transistor being turned on simultaneously.

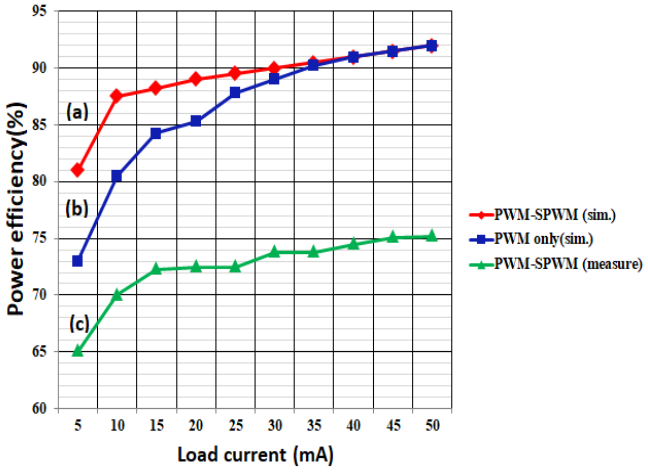


Fig. 8. Measurement results of power efficiency according to load current.

V. CONCLUSION

A dual-mode noninverting DC-DC buck converter for wearable AMOLED display has been designed. The converter uses a dual-mode with PWM-SPWM controller using the VCO, and has variable output voltages by changing reference voltage of error amplifier.

The converter has been implemented in a chip with 1.2 mm x 1.3 mm using a 0.35 μm standard CMOS process. Measurement results show that output voltage has 2.0 V ~ 2.7 V for input voltage of 3.3 V ~ 4.2 V. And the converter has a power efficiency of 65% ~ 75% under a load current of 5 mA ~ 50 mA. In simulation results, the dual-mode DC-DC converter is 8% higher in power efficiency than the previous converter using only the PWM mode.

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REFERENCES

[1] H. S. Jeon, “Power semiconductor market and technology development trends,” *Trend Analysis of Electronic Communications*, vol. 28, no. 6, pp. 206-216, Dec. 2013 (in Korean).

[2] G. A. Rincon-Mora, “A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications,” IEEE Trans. Power Electronics, vol. 19, no. 2, pp. 443–452, Mar. 2004.

[3] K. Nam, W. Seo, H. Ahn, Y. Hung, S. Hong, and O. Kwon, “A Highly Power-Efficient Single-Inductor Multiple-Outputs (SIMO) DC-DC Converter with Gate Charge Sharing Method,” *Journal of Semiconductor Technology & Science*, vol. 14, no. 5, pp. 549-556, Oct. 2014.

[4] C. Son and S. Byun, “A 82.5% Power Efficiency at 1.2 mW Buck Converter with Sleep Control,” *Journal of Semiconductor Technology &Science*, vol. 16, no. 6, pp. 842-846, Dec. 2016.

[5] C. Shi, B. C. Walker, E. Zeisel, B. Hu, and G. H. McAllister, “A Highly Integrated Power Management IC for Advanced Mobile Applications,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1723-1731, Aug. 2007.

[6] J. Xiao, A.V. Peterchev, J. Zhang, and S. R. Sanders, “A 4-μA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[7] W. R. Liou, M. L. Yeh, and Y. L. Kuo, “A high efficiency dual-mode buck converter IC for portable applications,” *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 667-677, Feb. 2008.

[8] S. Hong and G. Cho, “Inverting buck-boost DC-DC converter for mobile AMOLED display with real-time self-tuned minimum power-loss tracking scheme,” *in proc. of IEEE Custom Integrated Circuits Conference*, pp. 1-4, 2014.

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