Addressable Microstimulator Circuit for Neural Prosthesis

Ah Hyoung Lee[1], Jung Woo Jang, Chae Eun Lee, and Yoon Kyu Song[a]
Department of Nano Science and Technology, Graduate School of Convergence Science and Technology, Seoul National University
E-mail: [1]ahhyoung@snu.ac.kr

***Abstract* - Current state-of-the-art Brain-Machine Interfaces (BMIs) with multi-channel neural interfacing microsystem has been developed as the scale of CMOS process continuously miniatured. Further performance enhancement in BMIs relies on the ability to develop implantable integrated circuit system that would reduce the noise level and the power consumption to operate scalable thousands of channels. In this work, we describe a prototype of distributed wireless microimplants, which provide a high-density network of addressable neural stimulator system with an optical powering method. The proposed circuit built in a standard 0.18μm CMOS process, which include the rectifier, the binary phase-shift keying (BPSK) demodulator, the clock recovery, 9-bits metal fuses and the digital block to discriminate address for each chip. The circuit occupies 211×204 μm^2 of silicon area totally, which would be a reasonable size for micro implant. A photovoltaic cell is used to provide efficient power as BPSK modulated signal with the supply voltage 3 V. The designed circuit consumes ~77μW at a data rate of 20 Mbps at 20 MHz carrier frequency.**

***Keywords*—Brain-machine interface, implantable sensor, wireless microstimulator**

I. INTRODUCTION

Brain-machine interfaces (BMIs) is a technology that provides bidirectional communication between the external machine and the nervous system. With the neural information pathway through BMIs, it can provide solutions for neurological disabilities, which can be possible to monitor the neural activity and stimulate nervous system with input the specific signal to mitigate functional impairment through the use of multichannel electrode devices, either microelectrode arrays (MEAs) or Electrocorticography (ECoG). For the significant advantages, developing micro-implant systems in BMI are crucial for not only the neuroscience research but also the neural prosthetic systems enabling the treatment of neurological disease, the restoration of sensory and motor disabilities.

Among the several different approaches to neural implant system, wired microsensor system has been developed since its successful human clinical trials. It has facilitated the acquisition of neural data with high temporal and spatial resolution. However, the wired neural system requires cables that connect between the external device and brain for powering and data transmission penetrating skin and skull, which cause can cause neurological damage and the increasing risks of infection. As a result, the next-generation BMIs critically need to provide wireless powering and telemetry system across a range of brain tissue. Furthermore, individual implant volume is required to minimize less than sub-mm that can be inserted to the brain with minimum damage to tissue and located without any interruption biological function of the brain. Recently, small distributed sensors that remotely power controlled have been proposed as a way to measure the neural activity with a high spatial and temporal sampling (Fig. 1).

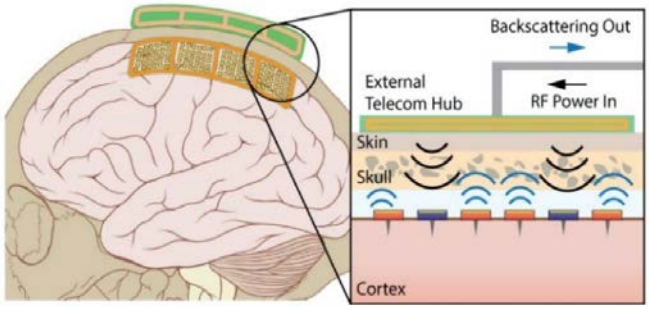

Fig. 1. The concept of a wireless neural implant('Neurograin') network.

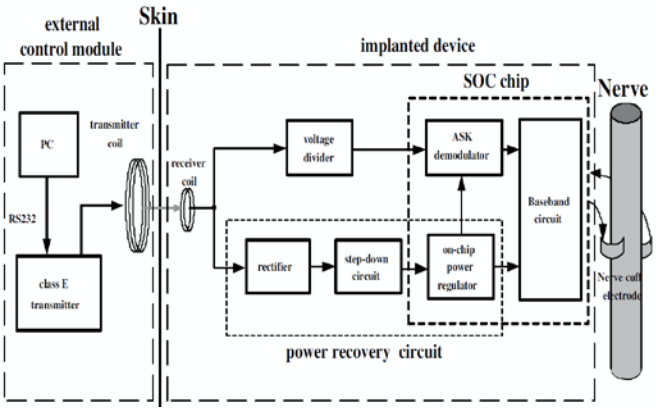

Fig. 2. Functional block diagram of wireless neural stimulating system [5]

Ultralow power consumption in biomedical implants is pursued so that some researches would be used for pre-clinical and clinical applications with RF wireless power transfer system [1, 2, 3, 4]. In present, the promising energy transfer method is inductive coupling using two pairs of coils depicted in Fig. 2 [5]. The external system consists of amplifier and transmitter coil. ASK modulation protocol is utilized to transfer power and data signal to the internal chip.

a. Corresponding author; yksong@snu.ac.kr

Manuscript Received May. 17, 2019, Revised Jun. 14, 2019, Accepted Jun. 22, 2019

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/bync/3.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

An on-chip low dropout (LDO) voltage regulator circuit works as power recovery from the induced RF signal, which drives a stable supply voltage 3.3V. However, the ASK modulation has the major drawback of relatively the low data transmission rate and the decreasing in amount of transferred power to implants. In this paper, we suggest low power, sub-millimeter, and individually addressable neural stimulation system. With the Manchester encoding technique, the system has downlink data communication with a high data rate and efficient power delivery.

II. FUNCTIONAL BLOCK OF SYSTEM

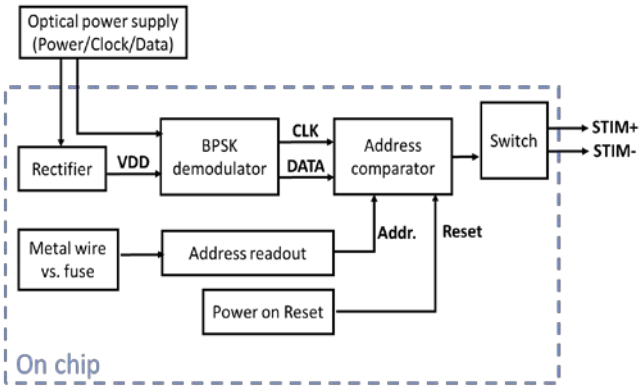

Fig. 3. Functional block diagram of neural implant system

A. Optical Power supply

For the optical power source, we have designed the photovoltaic cell that is based on a tandem structure pn-junction gallium-arsenide/aluminum-gallium-arsenide (GaAs/AlGaAs) hetero-structures [6, 7]. This optical power supply provides not only the power to operate the whole system on the chip but also the data and clock including specific sequence such as the 4-bits header, 9-bits address, and timing command. The photovoltaic cell is bonded with pads on chip, which can provide 3V input power for the internal circuit.

B. Clock recovery

The proposed clock recovery circuit extracts the clock signal from BPSK modulated input signal using a XOR gate. It is not necessary to have the implanted any modules to generate the clock within the chip, e.g., an on-board crystal oscillator, which can reduce the enormous total power consumption and chip area in layout. In addition, the clock signals are synchronized with the input BPSK modulated signal all the timing. The output of two-input XOR gate is fed to the digital block.

C. BPSK demodulator

BPSK demodulator is proposed without using any passive component in this work. Traditional BPSK demodulators in biological implanted devices need a large capacitor, which occupies a huge area on the chip. We use the diode-connected transistor in standard CMOS process that acts as a source-drain-shorted capacitor instead of a direct capacitor component. Based on the BPSK demodulator, it is an efficient way to be in synch with generated internal signals on chip such as clock, demodulated data, and the initial input signal.

D. Address Comparator

To make a form of distributed wireless sensor network, each chip is designed to have a unique ID, which is a 9-bits fuse using the top metal layer (aluminum) available in the CMOS process. A pad opening layer is used to eliminate any passivation layers on fuse area. The fuses exposed the top metal facilitate laser ablation process with the use of the green light laser (532 nm) for cutting the metal trace to set a bit. The address comparator compares the read-out address bits written by fuse on the chip and the incoming command signal through the BPSK demodulator in order to find the device that has matched addresses.

III. RESULTS AND DISCUSSION

A. Benchtop testing and validation

A bench top set up was created to test the performance of the stimulation source on the chip. The chip was wire-bonded to a PCB and a known resistor (50 kOhm) was connected across the terminal to figure out the output current (Fig. 4). For each block characterization, we connected SMA connectors with for each node. Since the chip is operated by 20MHz clock-frequency and its data rate is chosen at 20Mbps, we used a mixed signal oscilloscope with high sampling rate (Tektronix, MSO5204) and a 1 GHz probe (Tektronix, TPP1000) with low capacitance (3.9 pF/10 MOhm) to measure the chip performance accurately.

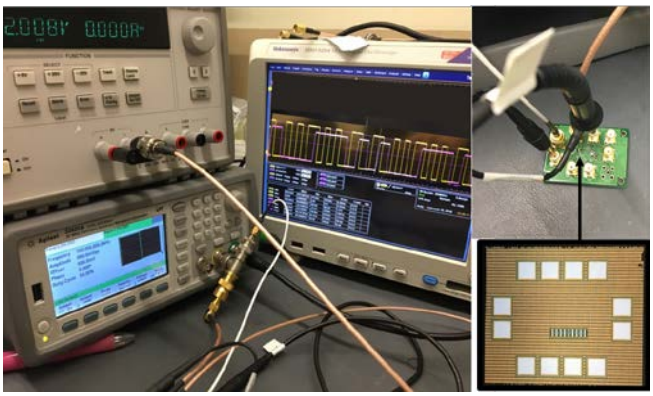

Fig. 4. Benchtop setup; The chip was wire-bonded on the PCB board and connected to a load resistance 50kohm.

B. Analog circuit

Fig.5 shows the block diagram of the analog circuitry in the chip, which is based on the data detection circuit. A pad (a part of the on the chip called 'Vin') is coupled to the external function generator, which simulates wireless implant system that operates by the photovoltaic cell. The input of BPSK modulated signal is fed to the rectifier, which then produces DC voltage to all on-chip circuits. The BPSK demodulator consists of a pulse-width measurement unit,

two identical Schmitt triggers and a NOR-based SR latch. In order to retrieve a clock signal, the demodulated data throughout the SR latch and the input BPSK signal are fed to a two-inputs XOR gate. The received input signal is slightly delayed via the demodulated data by using a buffer that consists of two cascaded CMOS inverters.

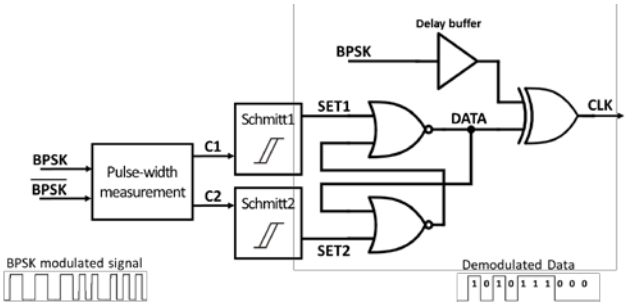

Fig. 5. Functional block diagram of analog circuitry

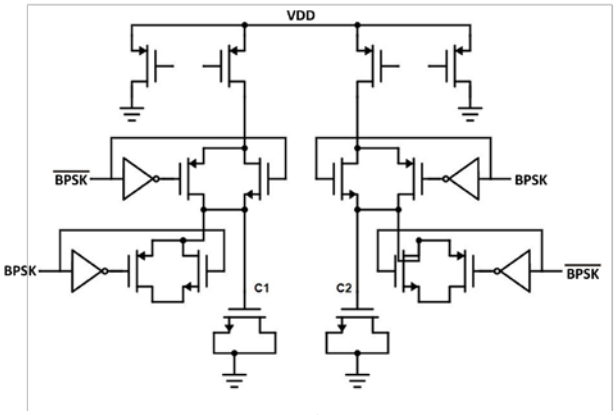

Fig. 6. Circuit schematic of Pulse-width measurement

Since we adapted the BPSK detector instead of the coherent demodulator that generally needs high power consumption COSTAS loop [8, 9], the analog circuit can be reduced the totally layout area of 44×47 μm^2 in Table 1 and the operating power level at ~77μW (Table 2).

As regards the rectifier circuit, maximizing the pulsed BPSK signal-to-dc power conversion efficiency has two challenges: (a) the received BPSK signal from the GaAs photovoltaic cell we have developed is not sinusoid signal but rectangular pulses, since the GaAs photovoltaic cell for the wireless power source is controlled by turning on and off the external light source. (b) As the high efficiency GaAs cell generates 3V output voltage, the rectifier requires a respond of voltage fluctuation from 0 to 3V. Therefore, the rectifier circuit is designed with the envelope detector structure that consists of two capacitors and a single diode. As a result, the rectifier produces 1.959V DC voltage and supplies it to all on-chip circuits.

For pulse-width measurement in the proposed demodulator, two capacitors are first charged with the same current and then the voltages across the capacitors are compared using a comparator. The process of charging and discharging of these capacitors are synchronized with the input BPSK signal. By applying the BPSK signals to be switched to each side of the pulse width measurement unit, the rectangular BPSK pulsed with longer time duration are interpreted as sawtooth waveforms in Fig. 6. In this design, as two capacitors used the diode-connected transistors, the demodulator is made of only transistors. Therefore, it not only provides a fast speed of charging and discharging but also reduces occupying total area on the layout. In the pulse width measurement, the integral form of BPSK signal is generated and then these signals are fed to the inputs of two Schmitt triggers. By choosing appropriate transistor aspect ratios, the upper trigger point of the designed Schmitt trigger is set to be 1.55V. If the signal from PWM circuit is higher than the trigger point, the Schmitt trigger makes signal goes to ′high′ state. Therefore, the output of the Schmitt triggers is a series of rectangular pulses, discriminating between the short and long BPSK carrier cycles. These pulses are fed into a NOR-based SR latch, which is used for a data decoder.

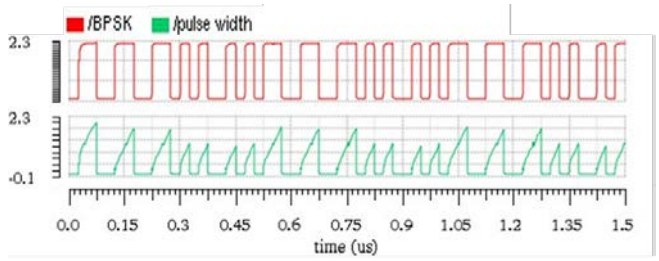

Fig. 6. Post-stimulated the voltage response across the capacitor in the pulse width measurement.

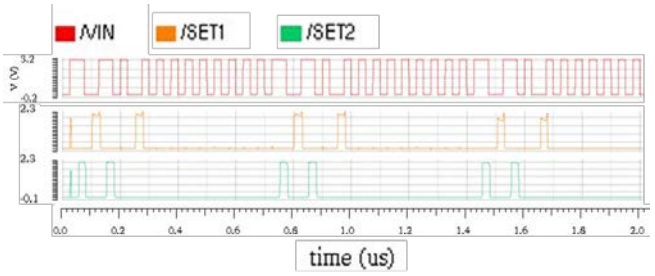

Fig. 7. Post-stimulated the rectangular pulsed voltage response of two Schmitt triggers (SET1, SET2) and BPSK input signal (VIN).

C. Digital circuit

The digital controller is a crucial component of the system related to address selectivity, which includes the serial input interface, the 9-bits address readout and a comparator. Serial data is delivered a 13-bits identification and the end-timing information 16-bits within a data packet structure described in Fig.6. When only the header detector detects the header sequence (′1011′), address comparator is active. The two-input serial data comparator compares the demodulated data and metal addresses. In order to assemble an addressable network, each chip is designed to have a unique device ID (Fig. 10). We have implemented a 9-bit fuse line using the top metal layer available in the CMOS process. Fuse-bits are set through laser ablation during post-processing and then read out in sequence from right to left. When two addresses both the demodulated data and read-out fuse bits are matched, the chip generates the current to stimulate the brain tissue. We designed that the chip operates with the load

impedance 50 kOhm that was calculated with low impedance electrode and it can be generated by ~36 μA at 1.8 V voltage. To control stimulation time, the chip is designed with a 4-bits counter. When all of bit in the 4-bits counter becomes ′1′, the generated stimulation current is stopped. We designed the 4-bits sequence header detector and the address comparator based on the Moore finite state machine (FSM). To control network with tens of addressable devices, it is noted that the digital output depends on only the current state of the FSM.

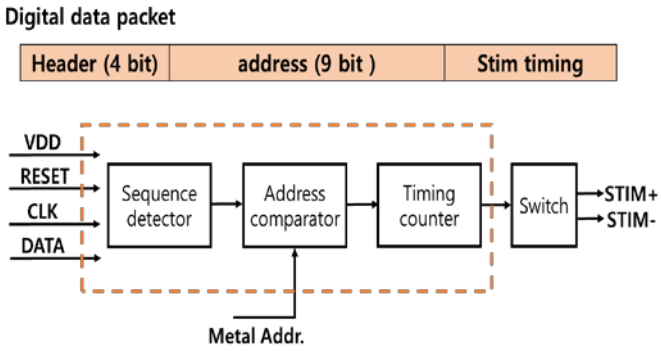

Fig. 8. A single data packet instructing stimulation current and the block diagram of the digital circuitry.

To test three important parts in the digital block for the initial prototype, we have designed three flags at the end of each part, which monitor them in sequence for each three output nodes: the header detector, the address comparator and the timing counter. Firstly, the header detector keeps detecting a specific binary sequence ′1011′ from the input of demodulated data and the its output is set to a high-level voltage only when the header is detected. Then, while the output of the header detector keeps setting the high voltage, the address comparator starts to compare the 9-bits demodulated address following the header bits and the read-out physically curved address. If two addresses are matched, the comparator output will be set to a high-level voltage, otherwise, it is set to a low-level voltage. The flags of the header detector and the address comparator are labelled ′detector_out′ and ′a′, respectively.

To validate discriminating address in the chiplet, the digital block that has a default address (10b’1) is tested in benchtop setup given two kinds of 20 MHz modulated BPSK input signal. One encoding sequence is all of the binary number ‘0’ and the other one is all of ‘1’. In Fig. 9(a), as two addresses are unmatched, the flag ‘a’ goes a low-level voltage during operating the address comparator and the stimulation current is not generated. On the other hand, in a case of matched addresses, ‘a’ keeps a high-level voltage after the header sequence detects and the switch to generate stimulation current turns on described in Fig. 9(b). We measured that the chip was able to source up to 33 μA, which is consistent with simulated values at nominal 1.66V across the 50 kOhm resistor (Fig. 9).

Ongoing work in our hand is the post-CMOS processing to make the electrode that has low impedance to deliver the stimulation current into brain tissue efficiently. We have used poly (3, 4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT: PSS), an organic material with demonstrated history of use for neural simulation applications as the planar structure stimulation electrode material [13]. The photolithographically fabricated 70 μm-sized PEDOT: PSS electrode brought impedance down to 4.33 kOhm at 1kHz.

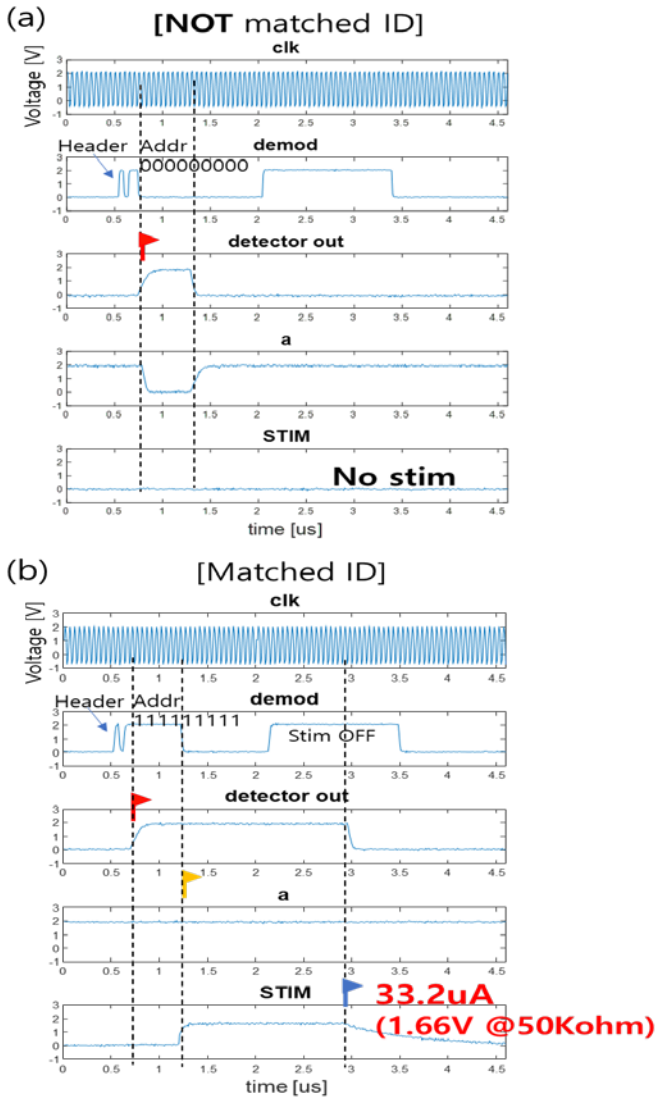

Fig. 9. Measured the digital block three outputs: the header detector ‘detector_out’, address comparator ‘a’, and stimulation current ‘STIM’; (a) when the addresses are not matched and (b) addresses are matched.

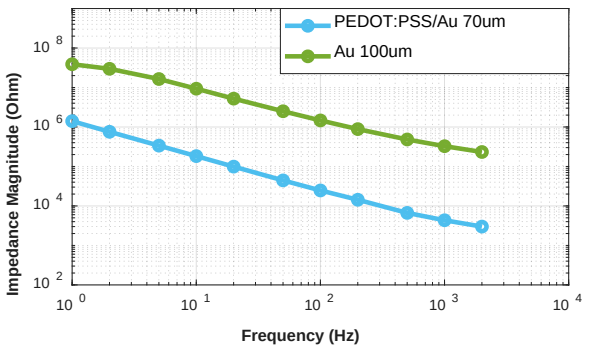

Fig. 10. Impedance spectra of Au and PEDOT: PSS/Au electrode

The total load resistance of the chip is twice the resistance of one electrode because stimulation current goes round-trip between two pads. One pad served as the working electrode and the other one served as the reference electrode. Based on this impedance result, we will target lower load resistance with PEDOT: PSS electrodes (< 10 kOhm) to get higher stimulation current via 1.8V supply voltage, which will be able to generate 150 μA approximately.

TABLE Ⅰ. The layout area for each block

Module	Area
BPSK demodulator	44×47 μm^2
Power on reset	14×65 μm^2
9-bits fuse	40×128 μm^2
Digital block	87×110 μm^2
Total layout.	211×204 μm^2

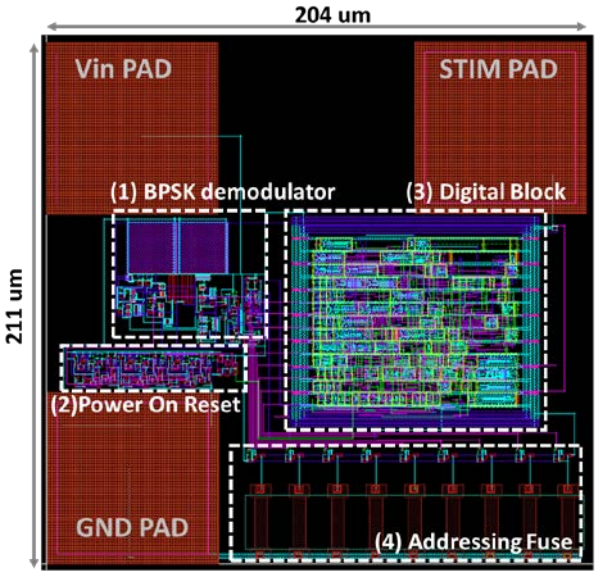

Fig. 11. Layout of the mixed mode chip in 0.18 μm CMOS process

TABLE II. Comparison of the BPSK demodulator

Ref.	Carrier Freq.(MHz)	Data Rate (Mbps)	DRCF Ratio	Power consumption(μW)
[8]	13.56	0.02	0.15%	3000 @ 3.3V
[10]	10	10	100%	77.9 @ 1.8V
[11]	10	10	100%	119 @ 1.8V
[12]	2	1	50%	82 @ 1.8V
This	20	20	-	77 @ 2V

The complete layout of the designed circuit is shown in Fig. 10, occupying the entire area of 204 x 211 μm^2, which is the ultra-small remotely powered stimulator. The area summary of the important blocks in the designed circuit is reported in Table I. Table II compares specifications of the demodulator and clock recovery circuit proposed in this work with some of the recently reported BPSK demodulators at the similar carrier frequency range.

IV. CONCLUSIONS

In this work, we have designed and demonstrated a prototype distributed neural implants for BMI applications. The entire chip was designed with 0.18μm Magnachip/SK Hynics general process using Cadence and tested by using chip-on-board process. Validation of the BPSK demodulator and addressable digital circuit have been demonstrated through the benchtop test. These are the first steps toward the micro-sized addressable neural implant system with the optical powering described in Fig. 3. In the future work, we will process the microfabrication of optical power source using the GaAs photovoltaic cell and its integration into the silicon chip that can be operated fully wirelessly.

REFERENCES

[1] J. Lee, F. Laiwalla, J. Jeong, C. Kilfoyle, L. Larson, and A. Nurmikko, “Wireless Power and Data Link for Ensembles of Sub-mm scale Implantable Sensors near 1GHz,” IEEE Biomedical Circuits and Systems Conference, Oct 2018.

[2] V. W. Leung, J. Lee, S. Li, S. Yu, C. Kilfoyle, L. Larson, A. Nurmikko, and F. Laiwalla, “A CMOS Distributed Sensor System for High-Density Wireless Neural Implants for Brain-Machine Interfaces,” IEEE 44th European Solid State Circuits Conference (ESSCIRC), Sept. 2018.

[3] L. R. Hochberg, M. D. Serruva G. M. Friehs, J. A. Mukand, M. Saleh, A. H. Caplan, A. Branner, D. Chen, R. D. Penn, and J. P. Donoghue, “Neuronal ensemble control of prosthetic devices by a human with tetraplegia,” Nature, 2006, vol. 442, pp. 164-171.

[4] P. Gao, E. Trautmann, B. M. Yu, G. Santhanam, S. Ryu, K. Shenoy, and S. Ganguli, “A theory of multineuronal dimensionality, dynamics and measurement,” bioRxiv, 214262, 2007.

[5] C.-C.Wang, Y.-H. Hsueh, U. F. Chio, and Y.-T. Hsiao, “A C-less ASK demodulator for implantable neural interfacing chips,” in Proc. IEEE Int. Symp. Circuits Syst., vol. 4, pp. 57–60, May 2004.

[6] Y.-K. Song, J. Stein, W. R. Patterson, C. W. Bull, K. M. Davitt, M. D. Serruya, J. Zhang, A. V. Nurmikko, and J. P. Donoghue, “A microscale photovolativ neurostimulator for fiber optic delivery of functional electrical stimulation,” J. Neural Eng., 4, pp. 213-219, 2007.

[7] S. Park, D. A. Borton, M. Kang, A. V. Nurmikko, and Y.-K. Song, “An Implantable Neural Sensing Microsystem with Fiber-Optic Data Transmission and Power Delivery,” Sensors, 13, pp. 6014-6031, 2013.

[8] Z. Luo, and S. Sonkusale, “A novel BPSK demodulator for biological implants,” IEEE Trans. Circ. Syst.-I, Vol. 55, No. 6, pp. 1478-484, Jul. 2008.

[9] N. Ghazal and M.-N. Mohammad, “Ultra-low power BPSK demodulator for bio-implantable chips,” IEICE Electronics Express, Vol. 7, No. 20, pp, 1592-1596, 2010.

[10] M. Karimi, M. H. Maghami, M. Faizollah and A. M. Sodagar, “A Noncoherent Low-Power High-Data-Rate BPSK Demodulator and Clock Recovery Circuit for Implantable Biomedical Devices,” IEEE Biomedical Circuits and Systems Conference, Oct 2014.

[11] F. Asgarian, and A.M. Sodagar, “A Carrier-Frequency-Independent BPSK Demodulator with 100% Data-Rate-to-Carrier-Frequency Ratio,” in Proc. of IEEE Biomed. Circ. Syst. Conf., pp. 29-32, Nov. 2010.

[12] B. P. Wilkerson, and J-K. Jang, “A low power BPSK demodualtor for wirelessly implantable biomedical devices,” in Proc. of IEEE Int. Symp. Circ. Syst., pp. 626-629, May 2013.

[13] Cogan, S.F., “Neural stimulation and recording electrodes,” Annu. Rev. Biomed. Eng., 10, pp.275-309, 2008.

Ah Hyoung Lee received the B.S. double degree in Electric engineering and Physics from Kwangwoon University, Seoul, Korea, in 2013 and is currently working toward Ph.D. degree in Nanoscience and Technology from Seoul National University, Seoul, Korea.

Her main interests are developing addressable neural microimplant system and low-power IC design with optical powering.

Jung Woo Jang received the B.S. degree in Electric engineering from Konkuk University, Seoul, Korea, in 2013 and is currently working toward Ph.D. degree in Nanoscience and Technology from Seoul National University, Seoul, Korea.

His main interests are BMI system for recording neural signal, wireless data and power transmission, especially ultra-low power low noise neural recording system.

Chae Eun Lee received the B.S degree in Electronics Engineering from Ewha womans University, Seoul, Korea, in 2013 and is currently working toward M.S. degree in Nanoscience and Technology from Seoul National University, Korea.

Her main interests are developing neural stimulator, especially for visual prostheses, and wireless bidirectional power transfer for implantable Brain Machine Interface.

Yoon Kyu Song received the B.S. and M.S. degree in Electric engineering form Seoul National University, Korea, in 1992 and 1994, respectively, and the Ph.D. degree in Electric engineering from Brown University, Providence, RI, in 1999.

His research interests include fundamental and applied Brain-Machine-Interfaces (BMIs), developing multichannel neural probe, wireless implant system, and semi-conductor optoelectronics.