A Low Power Capacitive Interface IC with Automatic Parasitic Offset Calibration using Dual-Range Digital Servo Loop

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Abstract **- Capacitive sensor interfaces are widely used for various micro-electro mechanical system (MEMS), however, capacitive sensor interface circuits suffer from severe parasitic capacitance problems. The parasitic capacitance, which is generally much larger than the sensing capacitance, results the large output offset variations. Thus an additional parasitic cancellation with external calibration equipment is required. This paper presents a low power capacitive interface IC with automatic parasitic calibration using dual-range digital servo loop for capacitive micro sensors without external equipment. The output offset with few hundreds fF parasitic capacitance of the capacitive sensor interface must be canceled to measure fF capacitance. To overcome the limitations of design rule and perform the wide compensation range, this paper proposed capacitor domain compensation (coarse range compensation) and charge domain compensation (fine range compensation). The chip is implemented using 0.18 μm complementary metal-oxide-semiconductor (CMOS) process. The input parasitic capacitances in the range from -10.6 pF to +10.6 pF can be cancelled out automatically, and the required calibration time is lower than 6 ms.**

I. INTRODUCTION

Various MEMS technologies, including accelerometers, gyroscopes, pressure sensors, touch-screen sensors, and so on, are designed using capacitive sensor interfaces [1-2]. Because the MEMS capacitive sensors are sensitive and have small size, the MEMS capacitive sensor interfaces require low offset, low noise, low power consumption and small active area. The capacitive sensing interfaces, however, result the large output offset variations due to mismatch problems with severe parasitic capacitances. The parasitic capacitances on the order of several hundreds of femtofarads to several picofarads are often much higher than sensing capacitance charges on the order of several tens of femtofarads. Therefore, additional offset calibration is needed to compensate the parasitic capacitance mismatch in capacitive sensing IC. An offset elimination is one of the most important problems in capacitive sensor interface IC. Some papers on calibration process have been reported for minimizing the parasitic capacitance. The dual compensation loop consisting of capacitor domain compensation (coarse range compensation) and charge domain compensation (fine range compensation) is proposed for capacitive MEMS sensors.

Since the output of the MEMS capacitive sensors is very small signal [2-4], the detected signal of MEMS sensors is necessary to remove the low-frequency noise and amplifier with high gain. For this purpose, the capacitive sensing chain with CDS (correlated double sampling) is used to reduce the flicker noise and the common mode interference.

To achieve the low power consumption and small active area, this paper presents new one way capacitor array in capacitive sensor interface. Contrary to the conventional sensor interface, the proposed capacitor arrays have about half active area and power consumption decreased by using the new one way capacitor array architecture.

This paper presents a low power capacitive interface IC with automatic parasitic calibration using dual-range digital servo loop. To achieve both the high resolution sub-fF capacitive calibration below physical design rules and the wide compensation range, capacitor domain compensation (coarse range compensation) and charge domain compensation (fine range compensation) are proposed. The previous capacitive ICs adopt manual capacitive calibration with coarse resolution. The presented capacitive interface IC with dual range digital servo loop can perform automatic parasitic cancellation and offset tracking. The proposed circuit can automatically compensate the offset variation, and additional calibration steps can be progressed without external test equipment.

II. EXPERIMENTS

A. Circuit description

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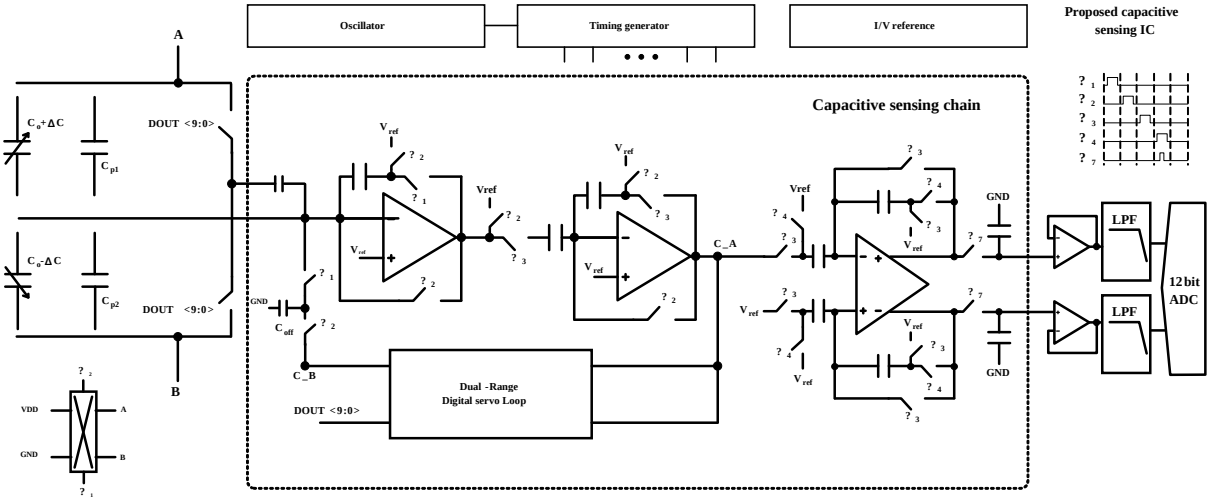

Fig. 1. The block diagram of the proposed capacitive sensing circuit with dual-range digital servo loop.

Fig. 1 illustrates the overall architecture of the proposed capacitive interface IC. The capacitive sensing chain adopts the correlated double sampling (CDS) technique to reduce the low frequency noise, including the 1/f noise [5-6]. The capacitive sensing chain is composed of three amplification stages. In the first amplification stage, capacitive sensing amplifier (CSA) converts the input capacitance charge to output voltage. Second amplification stage, the programmable gain amplifier (PGA), amplifies the output signal of CSA stage from 0 dB to 30 dB by using 6 bit gain registers. The amplified signal of the PGA output is compensated by the dual-range digital servo loop. Single to differential amplifier (SDA) of third stage converts the single-ended output signal of the PGA into the differential signal [7]. The output differential signals are converted to digital signals using the 12-bit successive approximation register (SAR) analog to digital converter (ADC) through low pass filters and buffers [8]. Dual-range digital servo loop adjusts the output offset to the desired value using binary search algorithm, and is implemented using a comparator, SAR logic, R-2R DAC, charge transfer switches, a charge-storing capacitor and switching cap DAC with 10-bit code.

B. Capacitive sensing chain

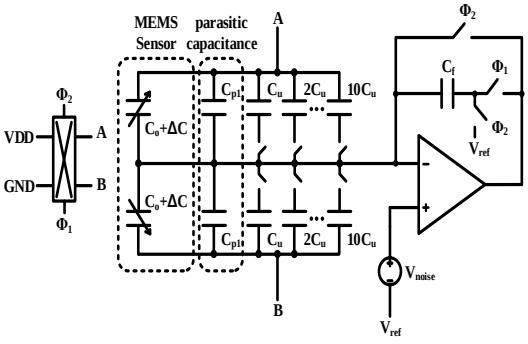

Fig. 2. Capacitive sensing amplifier (CSA): Conventional capacitor arrays calibration.

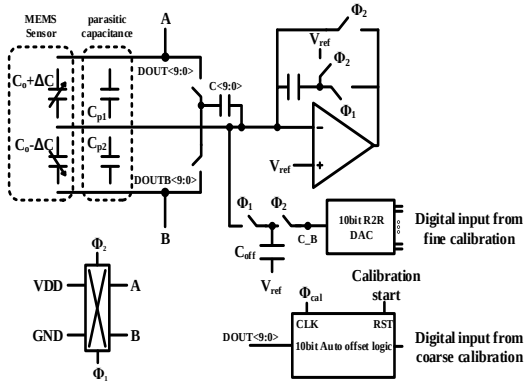

Fig. 3. Capacitor arrays with proposed charge-domain calibration.

Fig. 2 and Fig. 3 show the CSA with offset calibration using conventional capacitor arrays and proposed charge-domain fine calibration [1]. Binary-weighted capacitor arrays are used to cancel the input parasitic capacitance in the conventional CSA. Because of the minimum design rules of capacitors, the resolution of conventional offset calibration scheme using Binary-weighted capacitor arrays is limited. For example, in this process, the minimum capacitance of the metal-insulator-metal (MIM) capacitor is 20.8 fF (4 μm × 4 μm × 1.3 fF/μm2). The conventional offset calibration scheme cannot proceed calibration under the 20.8 fF. Also, the output amplification stage to obtain highly gain has large offset.

To achieve the high output offset accuracy and the high capacitance-to-voltage conversion gain, the fine offset calibrations with sub-fF steps are highly desired. To implement the calibration capacitance smaller than physical design rule, the coarse calibration and the charge-domain fine calibration scheme are designed, as show in Fig. 3.

The comparisons between the conventional capacitor array calibration scheme and the charge-domain calibration scheme are summarized in Table 1. The coarse calibration with DOUT<9:0> code can cancel the input parasitic capacitance in the range from -10.6 pF to 10.6 pF using one way binary-weighted capacitor arrays. This charge-domain calibration consists of switching cap DAC and control logic

adopting 10-bit successive approximation register (SAR). After the coarse calibration process, the fine calibration loop is progressed.

TABLE I.
Comparisons between capacitor arrays calibration and charge-domain calibration.

	Capacitor arrays calibration	Charge-domain calibration
Capacitor implementation	Physical capacitor (MIM or PIP)	Electrically equivalent capacitor
Minimum capacitor	Limited by physical design rules (in this design, 20.8 fF = 4 μm × 4 μm × 1.3 fF/μm^2)	LSB voltage*Coff/VDD (in this design, 0.224 fF = 1/1024*3.3/3.3*230 fF)
Size	Large (binary-weighted capacitor array)	Small (R-2R DAC, switches, and a charge- storing capacitor)
DC current	0	DC current consumption in R-2R DAC (1.2 μA in this design)

The output voltage using charge-domain calibration (Vo) and charge-domain equivalent capacitance (Ceq) can be expressed as (1).

$$V_O = -\frac{V_{DD}(2\Delta C + C_{p1} - C_{p2}) + C_{eq})}{C_f} + V_{ref}$$
$$C_{eq} = \frac{(V_{ref} - V_{DAC})}{V_{DD}} \times C_{off} \quad (1)$$

In this scheme, the charge storing capacitor, Coff, is about 200 fF, and the 10-bit R-2R DAC generates voltage from GND to VDD in 1024 steps. Therefore, the fine calibration loop can generate an electrically equivalent offset capacitance in the range from -110 fF to 110 fF with resolution of 0.224 fF.

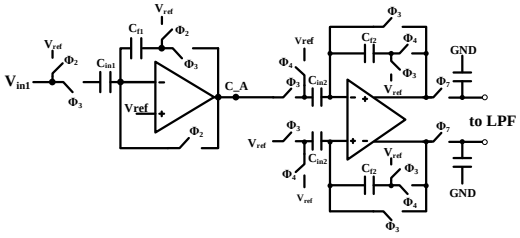

Fig. 4. Programmable Gain Amplifier (PGA) and Single to Differential Amplifier (SDA) circuit.

Fig. 4 shows the PGA and SDA circuit. The PGA and SDA employ correlated double sampling technique to reduce the low-noise components. The Φ2 and Φ3 are non-overlapping clocks. In PGA, an input coupling capacitor (Cin1) stores the input voltage signal and noise in Φ2 phase, and the stored charge is dumped in a feedback capacitor in Φ3 phase. The gain of PGA can be adjusted from 0 dB to 30 dB by programming Cf1, as expressed in (2). SDA works with the opposite phase of PGA, and the differential gain of SDA can be adjusted from 0 dB to 36 dB by programming Cf2, as expressed in (3). The output signal from the SDA is sampled on Φ7 phase.

$$V_{PGA} = V_{ref} + V_{in1}\frac{C_{f1}}{C_{in1}} \quad (2)$$

$$V_{S2D} = V_{ref} + 2V_{in2}\frac{C_{f2}}{C_{in2}} \quad (3)$$

C. Dual range digital servo loop

The proposed dual-range digital servo loop is illustrated in Fig. 5. The output voltage of PGA is sampled in Φ4 phase. In the 10-bit binary search successive approximation register (SAR) logic, actuation signal Φcal and calibration start signal is needed for calibration logic start. The shift registers (D-flip-flops) in the first row sequentially point towards the registers in the second row, which update the data to the comparator output.

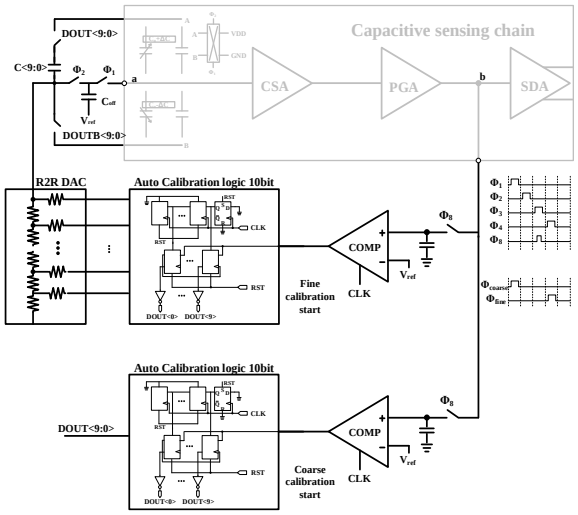

Fig. 5. The proposed dual-range digital servo loop.

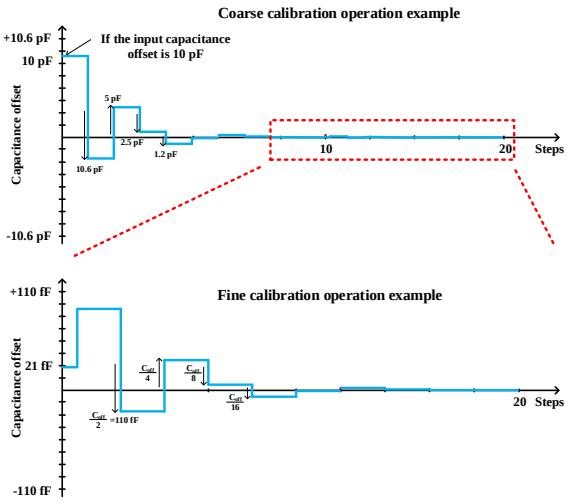

Fig. 6. Operation example of dual-range digital servo loop.

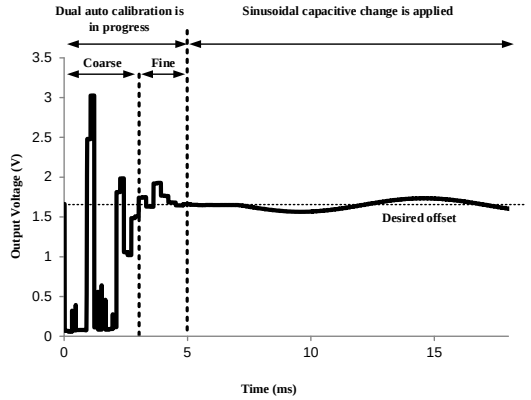

Fig. 7. Simulation result of the proposed circuit.

An operation example of dual-range digital servo loop is shown in Fig. 6. The operation principles of the circuit are as follows. If the input offset capacitance is 10pF, the sampled voltage and V_{ref} are compared in the comparator. Initial value of DOUT<9:0> is set to "1000000000". The PGA output voltage is compared to V_{ref} in Φ_4 phase. If output voltage of PGA is lower than V_{ref}, the MSB of DOUT<9:0> is replaced with "L". If output voltage of PGA is higher than V_{ref}, the MSB of DOUT<9:0> is maintained in "H". The analog output of R-2R DAC is determined by DOUT<9:0>. The R-2R DAC generates an electrically matched offset capacitance. Subsequently, the next lower bit of DOUT<9:0> becomes "H", and DOUT<9:0> becomes "X100000000", where X means the results of the previous step. The PGA output voltage is compared to V_{ref}, and the second bit of DOUT<9:0> is decided by comparator output. For ten cycles, output voltage of PGA is calibrated to V_{ref}, as shown in Fig. 7.

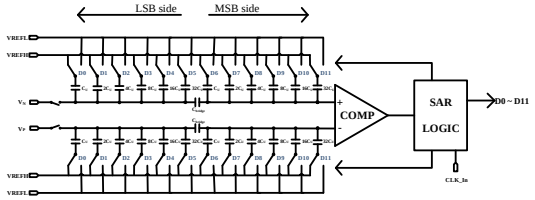

Fig. 8. Implemented successive approximation register (SAR) ADC circuit.

12-bits successive approximation register (SAR) ADC circuit is shown in Fig. 8. The SAR ADC consists of DAC, comparator, and SAR logic to control the DAC. When the start of conversion signal is applied on the SAR logic, fully differential analog signal is stored in both capacitive DAC and output of the comparator is sequentially updated to DOUT<11:0> of the SAR logic. The updated DOUT<11:0> of the SAR logic controls the capacitive DAC to track the analog signal.

The DAC adopts a split capacitive array DAC to reduce the capacitive array area. Although the split capacitive array DAC has a mismatched problem due to CMOS fabrication variations of bridge capacitor, the using DAC area is smaller than a thirtieth of conventional DAC array area, and the size of capacitors is as expressed in (4).

$$\begin{aligned} &C_0 = 2^0 C_u,\ C_1 = 2^1 C_u,\ C_2 = 2^2 C_u \cdots,\ C_5 = 2^5 C_u \\ &C_6 = 2^0 C_u,\ C_7 = 2^1 C_u,\ C_8 = 2^2 C_u \cdots,\ C_{11} = 2^5 C_u \end{aligned} \tag{4}$$

The conventional 12-bits capacitive DAC is required for 2^{12} multiple of unit capacitor. To acquire ideal linearity in split capacitive DAC, the total capacitance of LSB side including bridge capacitance (C_{bridge}) should be exactly matched with unit capacitance. The size of bridge capacitor is as follows in (5).

$$\begin{aligned} &\frac{1}{\frac{1}{xC_u}+\frac{1}{64C_u}} = C_u \quad (C_{bridge} = xC_u) \\ \Rightarrow\ &\frac{64x}{x+64} = 1 \\ \Rightarrow\ &64x = x + 64 \\ \therefore\ &x = \frac{64}{63} \end{aligned} \tag{5}$$

The unit capacitor C_u must be larger than kT / C noise and satisfies as expressed (6).

$$C_u \geq 10^{\frac{6.02n+1.76}{10}} \cdot 4k_B T \left(\frac{1}{V_{fullscale}}\right)^2 \approx 152.789\, fF \tag{6}$$

By the (4), Cu is determined to be larger than 152.789 fF and has 250 fF in this circuit.

III. RESULTS AND DISCUSSION

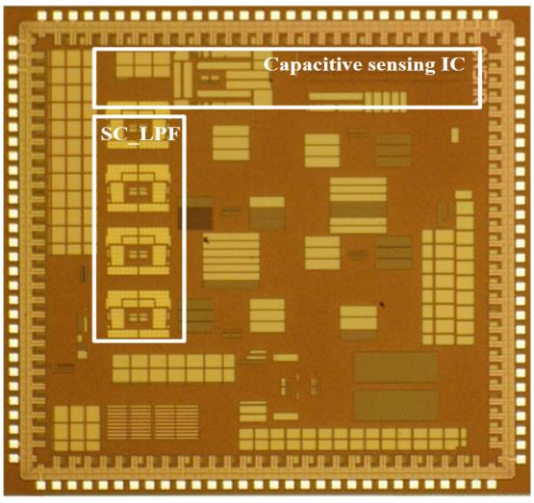

Fig. 9. The micrograph of the proposed capacitive sensing.

A die photograph of the fabricated capacitive sensing IC is shown in Fig. 9. The IC is fabricated using a 0.18 μm single-polysilicon six-metal complementary metal-oxide-semiconductor (CMOS) process with an active area of 1.76 mm^2.

Fig. 10 shows the measured analog output waveform with the dual-range digital servo loop operation. The yellow line and blue line show the differential output of the low pass filter. The green line is enable signal of dual-range digital servo loop, and the dual-range digital servo loop is activated at the falling edge of enable signal. After the operation of dual-range digital servo loop, the initial offset is removed automatically. The required calibration time is lower than 6 ms with 1 kHz calibration clock. Because the dual-range digital servo loop is operated before the low pass filter, the calibration clock for dual-range digital servo loop can be faster than cut-off frequency of the low pass filter. The frequency of calibration clock and cut-off frequency of the low pass filter are also programmable. The default cut-off frequency of the low pass filter is about 200 Hz.

To evaluate the performance of the fabricated IC, the IC and MEMS Z-axis capacitive accelerometer are rotated on 360 degree, as shown in Fig. 11. The detailed design and specification of the Z-axis accelerometer is described in [9].

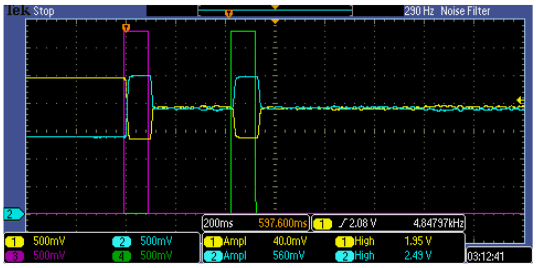

Fig. 10. The measured analog output waveform with dual-range digital servo loop operation.

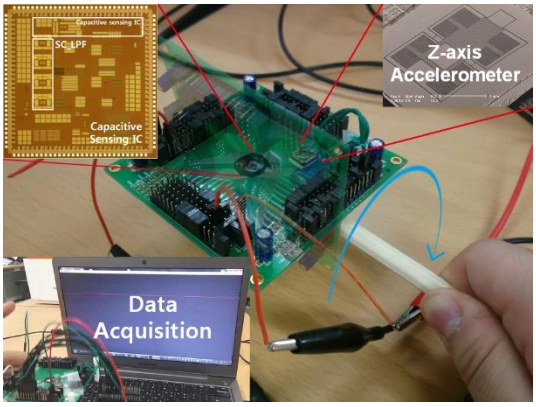

Fig. 11. The measurement setup with capacitive accelerometer.

The measurement results of the output noise are presented in Fig. 12. The input referred capacitance noise density, and integrated noise with 200 Hz bandwidth are 1.71 aF/√Hz and 24.2 aF_{RMS}, respectively. The input-output characteristics with MEMS Z-axis accelerometer are presented in Fig. 13. The scale factor, input range and, non-linearity are 0.1892 V/g, ±7.5 g, and 0.81 %FSO, respectively.

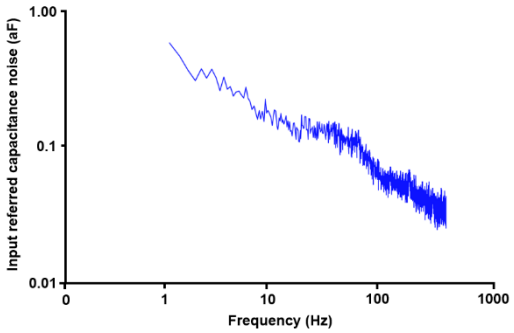

Fig. 12. Output noise Measurement results

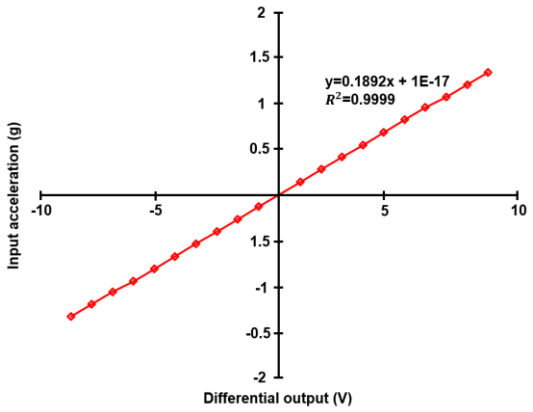

Fig. 13. MEMS Z-axis accelerometer input-output characteristics.

IV. CONCLUSIONS

A low power capacitive interface IC with automatic parasitic calibration using dual-range digital servo loop has been presented. The output offsets of the capacitive sensing chain due to the parasitic capacitances and process variations were automatically removed using the dual-range digital servo loop. The dual-range digital servo loop cancels offset variation by binary-search algorithm based on 10-bit SAR logic and charge-domain calibration circuits. The chip was implemented using 0.18 μm 1P6M CMOS process with an active area of 2.39 mm^2.

The simulation results of the proposed IC are as follows. The power consumption was 756 μW with 3.3 V supply. With the dual mode parasitic cancellation loop, the input parasitic capacitance in the range from -10.6 pF to 10.6 pF can be cancelled with the resolution of 0.224 fF. The required calibration time is lower than 6 ms. The input referred capacitance noise density and integrated noise with 200 Hz bandwidth were 1.71 aF/√Hz and 24.2 aF_{RMS}, respectively.

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