# A reconfigurable ultrasonic analog front-end IC for medical imaging applications

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***Abstract* - An ultrasonic analog front-end (AFE) interface IC for capacitive micro-machined ultrasound transducer (CMUT) in medical imaging systems using 0.18-$\mu$m standard CMOS process is presented in this work. The proposed AFE IC operating at 2.6 MHz is comprised of 15-Vpp high-voltage reconfigurable pulser/switch for transmit mode and low-noise preamplifier followed by a low-power time-gain compensation (TGC) amplifier with accurate programmable gain on receive mode. A total input referred current noise density of 415 fA/√Hz at 2.6 MHz is obtained in the receiver front-end IC while consuming 1.28 mW at 1.5-V supply. The AFE IC occupies 0.086 mm$^2$ of layout area.**

***Keywords*—Analog front-end (AFE), Capacitive micro-machined ultrasound transducer (CMUT), Ultrasound medical imaging system**

## I. INTRODUCTION

Ultrasound imaging has become a popular tool for low-cost point-of care diagnostic medical applications due to some of its favorable characteristics such as harmlessness to the human body, low cost, real-time monitoring capability, and small form factor [1]-[9]. Ultrasound imaging is used in various medical areas such as in fetus monitoring, biomicroscope, and so forth. To meet the demand for three-dimensional imaging with higher resolution, multi-transducer-array-based systems are being introduced to the market. Recently, much research is being carried out on the integration of multi-array capacitive micromachined ultrasound (CMUT) transducer [1] ever since its introduction to possibly replace the widely used piezoelectric transducers in commercial ultrasound system. The interface IC of ultrasound system consists of high-voltage (HV) signaling in the transmit (TX) mode and low-voltage (LV) circuits in the receive (RX) path. HV pulsers are needed when driving the transducer for large acoustic pressure generation while a switch is required for safe isolation between the HV and LV circuits assuming the same transducer element is used for both TX and RX. On the other hand, low supply voltage is preferred for RX circuits to reduce the power consumption. To effectively process reflected ultrasound echoes converted into an electrical signal by the transducer, the interfacing front-end of the analog signal processing system should be designed carefully, with low-noise, large gain, and sufficient dynamic range while consuming low-power and small area.

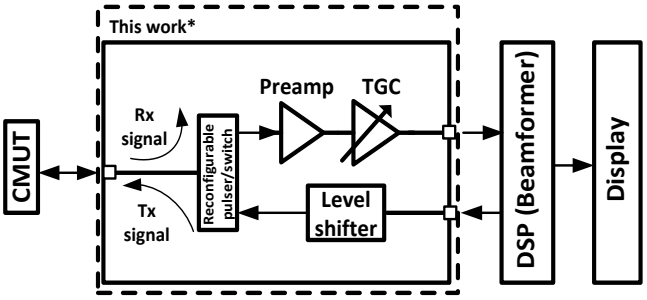


Fig. 1. Block diagram of proposed ultrasonic interface AFE IC for medical imaging applications.

To implement a highly integrated AFE IC with such advantages, we propose a bidirectional integrated AFE that includes an HV reconfigurable pulser in the TX path which also acts as an isolation switch [2], an LV preamplifier with low-power consumption and low noise performance in the RX path to amplify the small returning ultrasound echo signal, and a time-to-gain compensation (TGC) amplifier [3] with programmable gain which is robust to process variations. Section II discusses the AFE architecture and Section III describes each circuit block in detail. Section IV presents the simulation and measurement results followed by the conclusion in Section V.

## II. ARCHITECTURE

Figure 1 shows the block diagram of the proposed ultrasound medical imaging system which includes a signal processing IC for bidirectional operation. The reconfigurable pulser/switch drives the capacitive transducer with 2.6 MHz, 15 Vpp unipolar signal to interface a CMUT. As the generated acoustic waves propagate through the medium, some of the signal is reflected back as echo signals due to the difference in the acoustic impedance levels of tissue boundaries. The reflected echo is converted back into weak electrical signal by the transducer element and is routed through the turned-ON switch of the reconfigurable pulser. After the switch, the signal is processed by the following blocks in the RX path. RX path operating on 1.5-V supply comprised of a low-noise

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Manuscript Received Mar. 05, 2018, Revised Mar. 13, 2018, Accepted Mar. 27, 2018

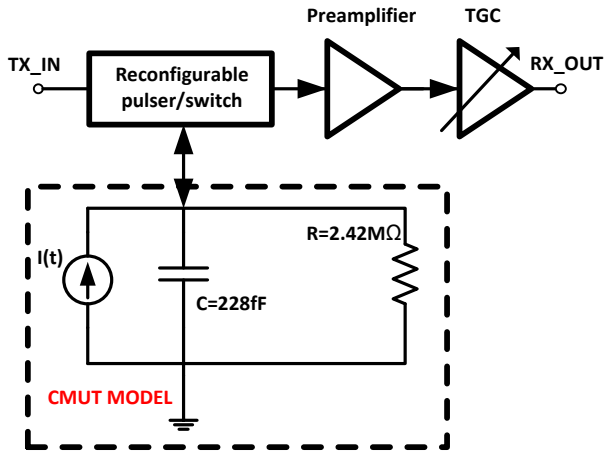


Fig. 2. Simplified equivalent electrical model of CMUT device.

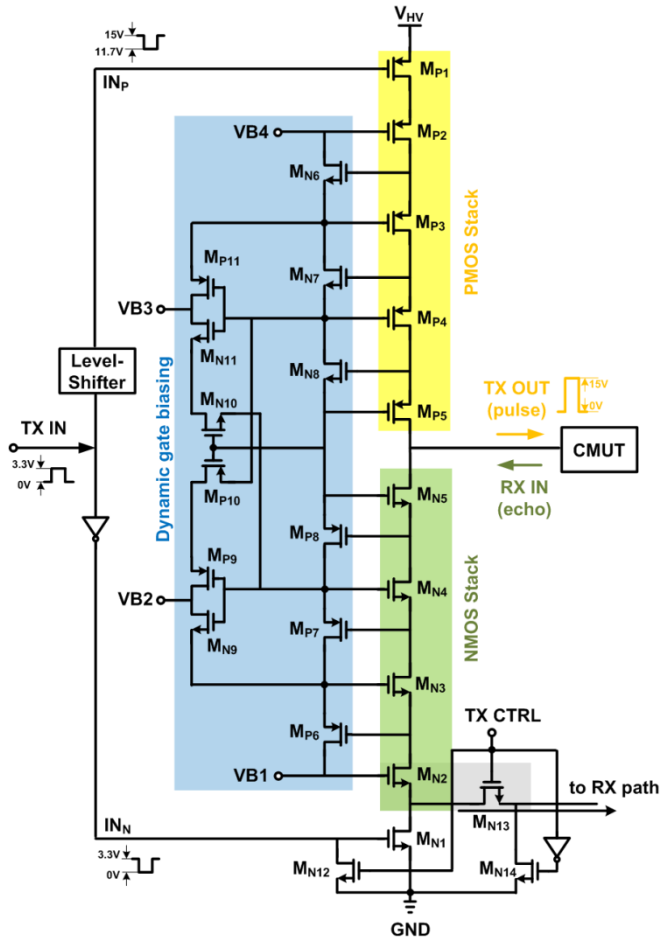


Fig. 3. Circuit schematic of proposed reconfigurable pulser output driver and isolation switch [2].

preamplifier for first stage amplification followed by the TGC amplifier for further processing of the signal at 2.6 MHz CMUT frequency. A beamformer is used to generate delayed trigger pulses to the multi-channel HV pulsers in the TX mode, while it is used for digitization and to further process the received signals in the RX mode. An equivalent electrical model of the CMUT operating at 2.6 MHz of frequency is shown in Figure 2 [4]. The model represents a DC bias

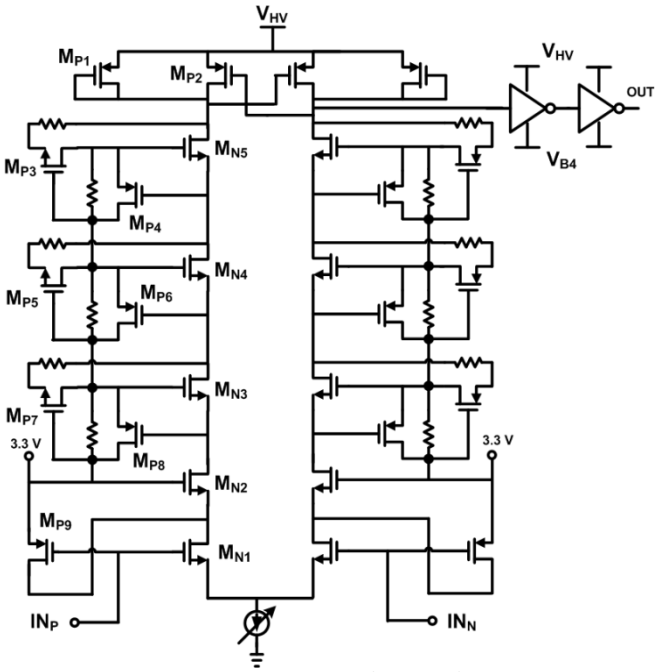


Fig. 4. Circuit schematic of level-shifter [4].

voltage of 10–15 V with element capacitance calculated to be 228 fF and additional parasitic parallel capacitance in the pF range is added in simulation.

## III. CIRCUIT DESIGN

### A. *Transmit (TX) Path*

The HV pulser in the TX path is used to generate up to 15-Vpp unipolar signal from a 3.3-Vpp input trigger signal. Previous pulser implementations usually use HV MOS transistors in the level-shifter and output driver blocks in order to enable large voltage operation without device breakdown [5]. In this work, stacked standard CMOS transistors [4] are used to replace the HV transistors, providing a low-cost design solution.

Figure 3 shows the proposed HV output driver circuit of the reconfigurable pulser/switch used in TX path. The transistor stacking approach with dynamic gate biasing enables the circuit to generate 15 Vpp pulse reliably. The biasing circuit, which acts as a resistive divider, ensures the voltage difference between the terminals of the transistors in the stacks are within 3.3 V during ON-OFF and OFF-ON transitions. $V_{B1}$ to $V_{B4}$ are bias voltages which are applied externally. Five stacks of 3.3-V PMOS and NMOS transistors are used in the design. The usage of deep-nwell NMOS transistors allows all body terminals, omitted in the figure, to be tied to their respective source terminals and prevent voltage stress between the body and other terminals. To briefly explain the operation for the NMOS stack, when the NMOS input terminal $I_{NN}$ changes from LOW to HIGH, $M_{N1}$ transistor is turned ON, which turns ON $M_{N2}$. As the drain node of $M_{N2}$ is also discharged, $M_{P6}$ turns ON, and the gate of $M_{N3}$ is shorted to $V_{B1}$ which is at 3.3 V, and turns ON $M_{N3}$. The same reasoning can be applied to $M_{P7}$, $M_{N4}$, $M_{P8}$, and $M_{N5}$. During the time the NMOS stack is all turned ON, the

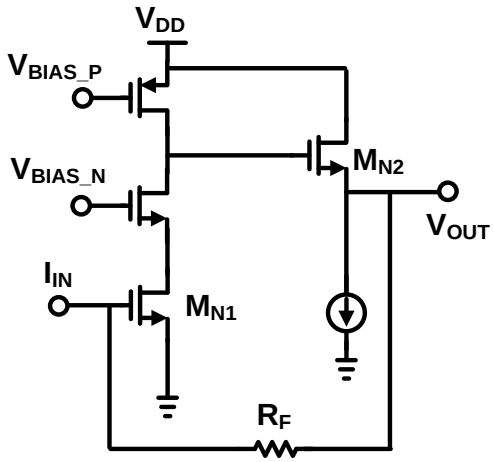


Fig. 5. Circuit schematic of low-noise preamplifier.

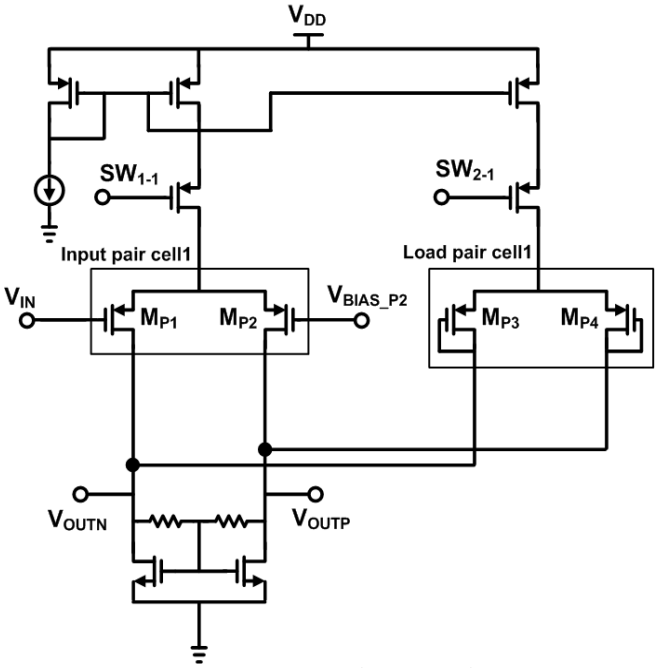


Fig. 6. Circuit schematic of TGC amplifier [3].

PMOS stack is turned OFF, and vice versa.

Thanks to the reconfigurable approach, significant die area consumed by the isolation switch can be reduced [2]. Embedded within the reconfigurable output driver, the transistors $M_{N2}$ to $M_{N5}$ and $M_{N13}$ are used as the isolation switch. The combination of this NMOS stack with control transistors forming the isolation switch prevents HV affecting the RX circuits during the TX mode. During the RX mode, the NMOS stack is turned ON allowing the received current signal to be routed to the transimpedance preamplifier with negligible voltage drop and degradation in noise performance. The upper PMOS branch ($M_{P1}$ to $M_{P5}$) is turned OFF during the RX mode.

A level-shifter, shown in Figure 4, is included to convert the 0 to 3.3 V swinging input trigger signal to the 11.7-to-15 V trigger signal which drives the PMOS transistor in the output driver. Similar stacking approach is used for the level-shifter, which allows reliable HV operation using standard 3.3-V transistors.

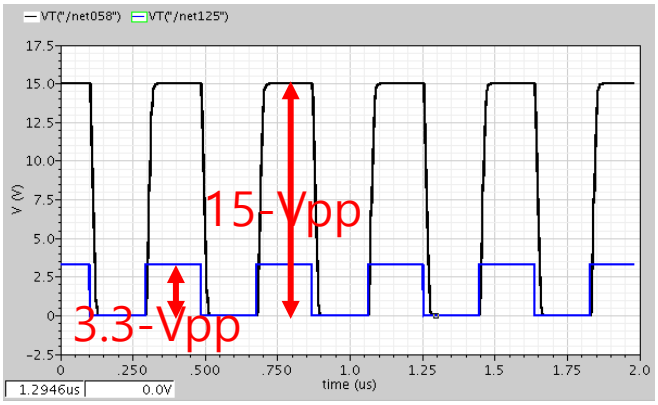


Fig. 7. Simulated pulser input (3.3-Vpp) and output (15-Vpp).

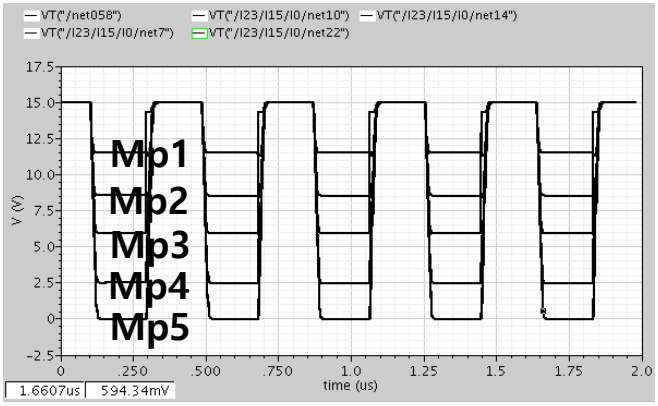


Fig. 8. Drain voltages of PMOS stack.

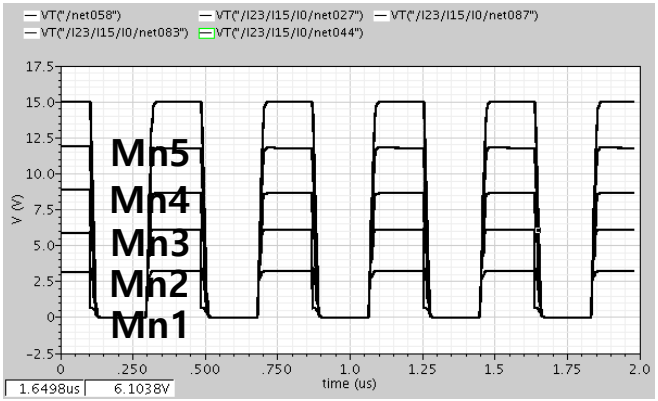


Fig. 9. Drain voltages of NMOS stack.

## B. *Receive (RX) Path*

Figure 5 shows the circuit schematic of the designed low-noise preamplifier and Figure 6 shows the 4-bit programmable TGC amplifier. Both are operating at 2.6 MHz CMUT frequency and 1.5-V supply. For the design of the current signal input preamplifier, several topologies such as common-gate, current-reuse inverter type, and resistive-feedback TIA have been considered. As the operation frequency is only several megahertz and since the resistive-feedback TIA offers ease of DC biasing, low input impedance and good noise performance, this topology was chosen. The preamplifier is designed using cascode stage and source

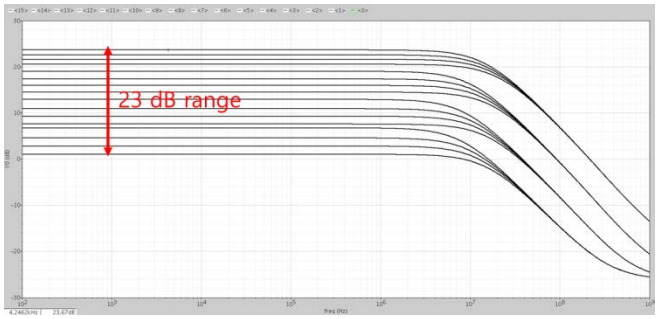


Fig. 10. Simulated gain response of TGC amplifier.

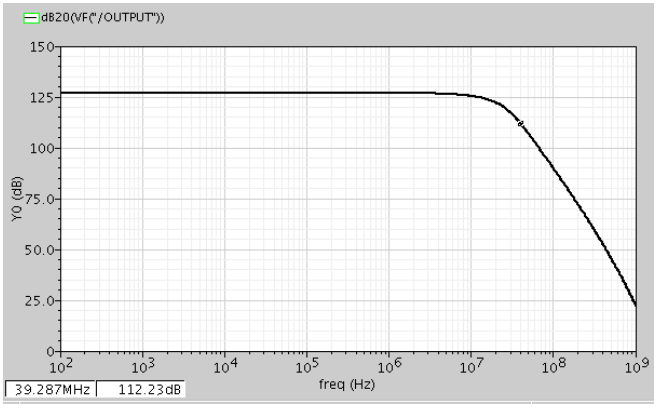


Fig. 11. Simulated gain response of RX front-end at max. gain setting.

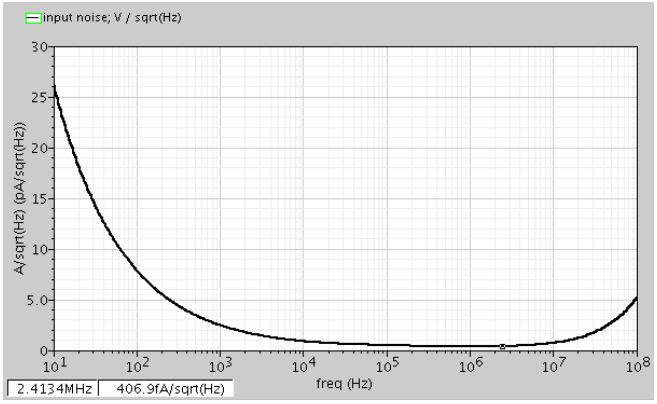


Fig. 12. Simulated input referred current noise of RX front-end.

follower amplifier. Large feedback resistance of 150 kΩ allows high closed-loop transimpedance gain and low-noise performance despite consuming low power [6]. The preamplifier is designed to provide 103 dBΩ of gain and the input referred current noise is simulated to be 377 fA/√Hz at 2.6 MHz while consuming 355 $\mu$W at 1.5-V supply. The TGC amplifier is used to provide variable gains according to the signal strengths reflected from different distances [7]. The proposed TGC amplifier is designed as a single-to-differential amplifier using PMOS input differential pair and diode-connected load [3]. The TGC gain is decided by the ratio of the transconductance of the input pair to the load pair, thus shows robustness to process variations. Several input pair and load pair unit cell branches with different transistor sizing and bias current are added to the circuit and its gain is varied by discrete switching using 4-bit digital control

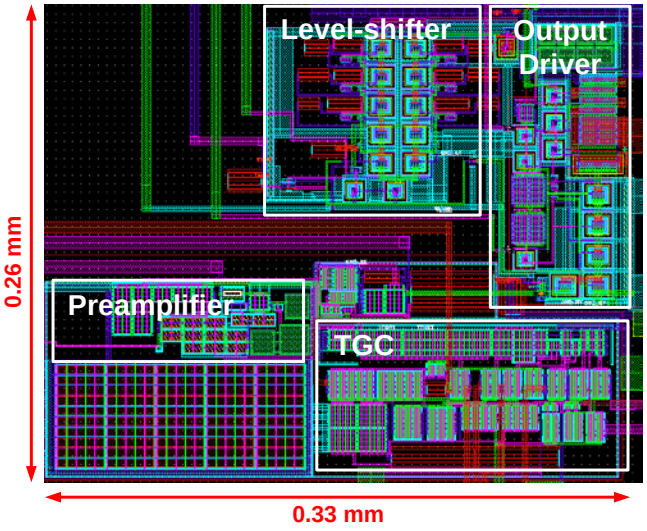


Fig. 13. Layout capture of AFE IC

TABLE I.

Performance summary of TGC amplifier IC

| Parameters | This Work | [7] | [9] |
|---|---|---|---|
| Supply voltage | 1.5 V | 3 V | 0.5 V |
| Operation frequency | 2.6 MHz | 1 MHz | 5 MHz |
| Gain range | 1~24 dB | 14~36 dB | -1~21 dB |
| Gain step | 16 | adaptive | 7 |
| Input noise | 5.5 nV/√Hz | 7.41 nV/√Hz | 7 nV/√Hz |
| Power | 923 µW | 12.6 mW | 54 µW |
| Load | CMUT | N/A | PZT |
| Technology | 180 nm CMOS | 130 nm CMOS | 65 nm CMOS |

ON/OFF signal which is applied externally to turn ON or OFF the respective branches. The input and load pair branch number can be adjusted to adequately comply with required performance of the system. This work realized 16 gain steps of TGC with the maximum gain at almost 24 dB. The simulated input referred voltage noise is 5.5 nV/√Hz while consuming less than 925 µW at 1.5-V supply voltage.

## IV. SIMULATION RESULTS

Figure 7 shows the simulated 2.6-MHz, 15-Vpp pulser output generated by the reconfigurable pulser during the TX mode. Figure 8 and 9 shows the transient voltages of the drain terminals of PMOS and NMOS transistors in the stacks, respectively. It can be seen that the voltage difference between the source and drain of each transistor is within 3.3 V. This similar simulation is checked for all terminals of all the stacked and control transistors to make sure the reliability of the devices are not compromised.

TABLE II.
Performance summary of AFE IC

| Parameters | This Work | [2] | [4] |
|---|---|---|---|
| **Integrated blocks** | Reconfig. Pulser/Preamp/ TGC | Reconfig. Pulser/ Preamp | Pulser/SW/ Preamp |
| **Pulser output voltage** | 15 V | 15.6 V | 15 V |
| **RX Supply voltage** | 1.5 V | 1.65 V | 1.1 V |
| **Operation frequency** | 2.6 MHz | 2.6 MHz | 2.6 MHz |
| **Preamp gain** | 103 dBΩ | 103 dBΩ | 95.1 dBΩ |
| **TGC gain range** | 1~23 dB | N/A | N/A |
| **BW at max gain** | 20 MHz | 5 MHz | 12 MHz |
| **Input noise** | 415 fA/√Hz | 2.1 pA√Hz | 3.5 pA/√Hz |
| **Power** | 1.28 mW (preamp+TGC) | 0.18 mW (preamp only) | 0.38 mW (preamp only) |
| **Area** | 0.086 $mm^2$ | 0.052 $mm^2$ | 0.15 $mm^2$ |
| **Technology** | 180 nm CMOS | 180 nm CMOS | 180 nm CMOS |

Figure 10 shows the simulated gain response of the TGC amplifier for 16 gain steps. The gain range is from 1 dB to 24 dB and sufficient bandwidth is achieved for all gain steps. The overall simulated gain response of the RX front-end at maximum TGC gain setting is shown in Figure 11. Figure 12 presents the input referred current noise of RX front-end where less than 415 fA/√Hz of noise density is achieved at 2.6 MHz frequency. Figure 13 shows overall AFE IC layout capture which includes the reconfigurable pulser, preamplifier, TGC amplifier, current bias circuits, and decoupling MOS capacitors. The overall layout area is 0.086 $mm^2$.

Table I presents the performance summary of the proposed TGC amplifier and compares to recent similar works. This work provides 16 gain steps with good frequency response and noise performance while consuming low-power. Table II compares the overall AFE IC with similar works. In comparison to our previous works in [2] and [4], the proposed work has TGC capability in the RX mode to perform wide and accurate programmable gain range while maintaining sufficient bandwidth. The addition of the TGC block allows the AFE to process wide dynamic range of returning echo signals, and reduces the burden of the following ADC block in the signal processing chain. In addition, this work achieves improved noise performance while consuming low power with small increase in overall area.

## V. CONCLUSION

A highly-integrated bidirectional interface analog front-end IC for ultrasound medical imaging systems is designed using 0.18 μm CMOS process. A high voltage reconfigurable pulser which can also operate as an isolation switch is proposed to enable much reduction in die area while maintaining good performance and reliability. In addition, a robust time-to-gain compensation amplifier is designed for wide and accurate programmable gain.

## ACKNOWLEDGMENT

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT, (NRF-2018R1C1B6003088). This work was supported by IDEC for EDA Tool and MPW support.

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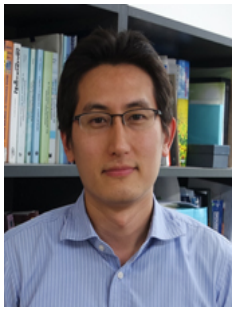

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