A Zero Current Detector with Low Reverse Current by Forcing Freewheel Switch Operation in Buck Converter

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Abstract – At light load condition, buck converter usually requires a zero-current detector (ZCD) to prevent reverse current flowing back to the source to improve conversion efficiency. This paper presents a ZCD with enhanced time response of the freewheel switch operation. The proposed ZCD was simulated using a 0.18-μm CMOS process in a PWM voltage mode control type-III compensation buck converter, to convert a DC input voltage of 3.3V to a DC output voltage of 1.8V. The buck converter was designed to work in CCM at heavy load, PFM at light load, and DCM in a short transient between CCM and PFM. The PWM switching frequency is 2MHz, and the output load current range is from 20mA up to 300mA. The proposed ZCD was tested as compared to the conventional one for the same condition, showing maximum improvement of 6.9% in efficiency in PFM, making the overall conversion efficiency greater than 89.7%.

I. INTRODUCTION

The concept of PWM control is being known for forty years; yet until now, PWM controlled buck converter is still widely used for its simple structure. PWM can be operated in two modes: (1) continuous conduction mode for heavy load; and (2) discontinuous conduction mode for light load. However, in light load condition, there is a disadvantage of PWM control: The discontinuous conduction mode shows a low conversion efficiency. Therefore, normally another control method, which is pulse-skipping mode (PSM), or pulse frequency modulation (PFM) is often used instead [6], to improve conversion efficiency at light load. Regardless of which light load control method is used, it is necessary to use a zero current detector to block the negative inductor current flowing back to the source in order to reduce the root mean square (RMS) current. In this way, conduction loss is reduced, and as a result, conversion efficiency can be improved at light load.

Fig. 1 shows the overall structure of the PWM voltage mode control type-III compensation buck converter, in which, the main switching component are the high side switch HSW and the low side switch LSW. These power switches intersect with the LC low pass filter at LX crossing point. When the HSW conducts, current flows from VIN to VOUT via HSW and inductor Lo.. When the LSW conducts, current flows from ground to VOUT via LSW and inductor Lo.. Therefore, by using a relevant control method, this structure can convert a DC voltage VIN to a lower DC voltage VOUT, which is the average of LX voltage, and can supply enough current to the load RL.

Considering the period that LSW conducts, LX node voltage potential should be negative for the current can flow from ground to LX. With the present of negative inductor current during this period, when the inductor current flows from VOUT to ground, LX node voltage potential changes to positive. Therefore, when the inductor current crosses zero, LX node's potential is also ground. Hence, by comparing LX voltage node with ground, zero inductor current crossing point can be detected [2][7][8]. The process described above is illustrated in Fig. 2 (b).

The conventional method for zero inductor current detection is to track the zero crossing point of the LX node. However, there is a difficulty in this detection method: At light load current condition when reversed inductor current often occurs, the change in LX voltage potential is also very small:

$$-LX = R_{ON} * I_L \quad (1)$$

in which RON is the ON resistance of the LSW, and IL is the inductor current.
Usually this small voltage potential change of LX node cannot overcome offset voltage of comparator; hence, usually a preamplifier stage is required before the comparator stage to alleviate this difficulty [2].

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Using the conventional ZCD method, the error of the ZCD is assumed to be only the incorrectness of the LX crossing zero detection time. Therefore, until now, the studies of ZCD circuit only focus on increasing the speed of the ZCD comparator to enhance the correctness of the detection time of the zero inductor current crossing point [2][7][8].

Also based on the assumption of incorrect ZCD detection time, a PID loop circuit for ZCD is also studied to reduce reversed inductor current as in [8]; however, an absolute negative inductor current of about 8mA still presents, according to the simulation results in the study. The explanation for the non-negligible negative inductor current (even when using PID control) cannot just the PID error. There must be another important cause as well: For the correctness of freewheel switch function during the present of negative inductor current, the voltage potential of LX node should be larger or equal to that of the output voltage. However, since the LX node voltage is attached to a large parasitic capacitance of the two power switches, while the inductor current at this time is very small (near zero), it is difficult to raise LX voltage potential from below ground (before ZCD event occurs) to VOUT (stable operation under ZCD condition) instantaneously. Therefore, a finite charging time is required for inductor current to charge LX voltage up to its designed voltage potential. During this required time, the freewheel switch is unable to perform its designed function.

Recognizing this fact, in [10], a proposed ZCD circuit is implemented using the conventional zero current crossing detection method based on LX crossing ground voltage detection, with a proposed forced operation for freewheel switch to re-direct negative inductor current back to the load. In addition, a positive rising edge SR flip-flop is also proposed and used in the proposed ZCD circuit to avoid false zero current detection due to deadtime control, noise and possible oscillation of LX voltage node. This paper is the extension of [10].

II. Overall PWM voltage mode type III compensation buck converter

The overall architecture of the test system can be seen in Fig. 1 (a). The basic buck converter system is designed with PWM control using voltage mode [3] compensation type III [4] as shown in Fig. 1 (b). The error amplifier gain corresponding to the compensation structure in Fig. 1 (b) is:

$$\frac{V_{error}}{V_{OUT}} = -\frac{(1+sR_{C1}C_{C1})(1+sC_{C3}(R_{fbu}+R_{C3})}{sR_{fbu}(C_{C1}+C_{C2})(1+sR_{C1}(C_{C1}//C_{C2})(1+sR_{C3}C_{C3}))}$$

The gain from error amplifier Verror to output voltage VOUT can be calculated as:

$$\frac{V_{OUT}}{V_{error}} = \frac{V_{IN}}{V_{SAW}} \frac{R_L(1+sC_oESR)}{s^2L_oC_o(R_L+ESR)+s(L_o+R_LC_oESR)+R_L}$$

The loop gain of the system can be obtained as the multiplication of the two mentioned gain above. According to the current load condition, the circuit can operate mainly in two modes: CCM at heavy load or PFM at light load.

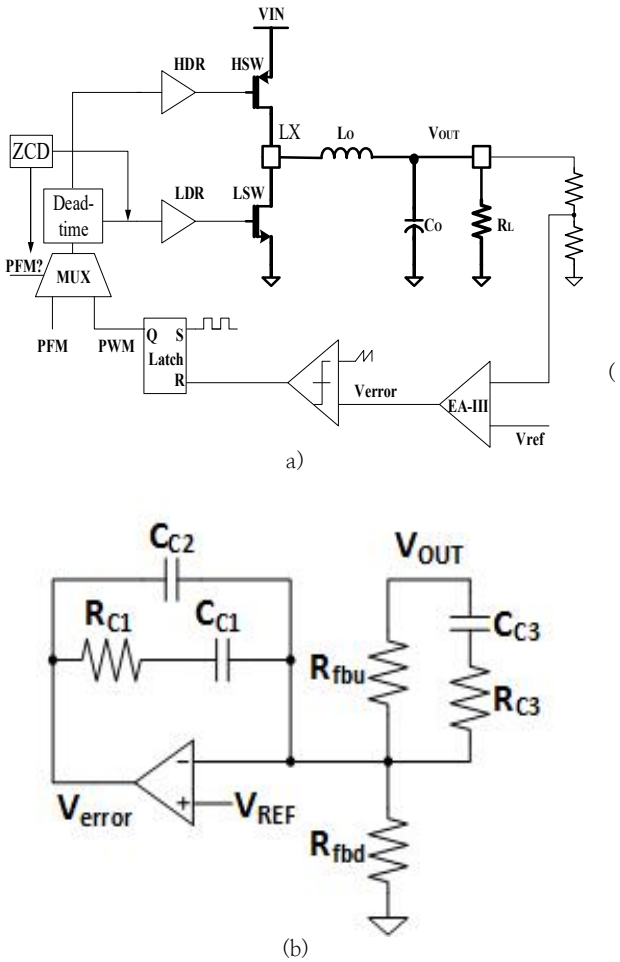


Fig. 1. (a) Overall Voltage Mode Type III Buck Converter Architecture. (b) Compensation Type III structure.

In order to reduce output voltage drop when load current changes from low to high, usually the output voltage level of PFM is designed a little higher than the designed one of PWM. When the load condition is in between heavy load and light load, there is a potential of continuous changing mode between PWM and PFM. This effect causes more ripples to the output voltage due to voltage droop effect when load condition changes. To reduce the number of mode-switching events, a counter is implemented to make decision of changing mode: The counter counts the number of detected zero-current events to make decision of changing mode.

III. Zero current detection operation

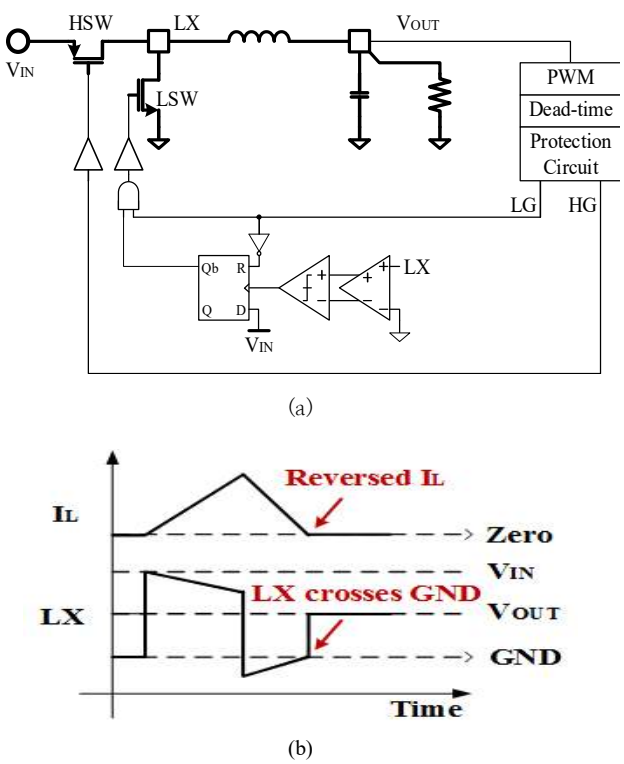
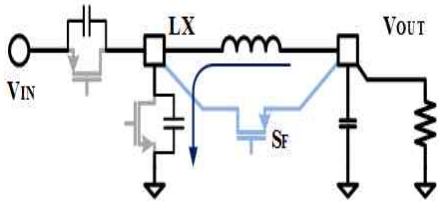


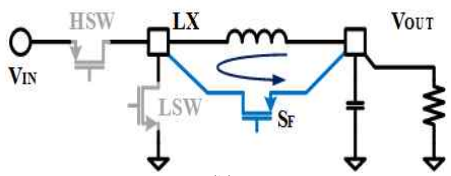
Fig. 2. Conventional ZCD circuit: (a) ZCD architecture, (b) Timing diagram when the ZCD event occurs

Shown in Fig. 2 is the architecture of the conventional ZCD, which is based on the detection of zero voltage potential of LX node as described in part 1. Because the inductor current is a continuous function, after ZCD event, even when the two power switches are turned off, absolute negative inductor current still presents and will be diminished via the parasitic capacitor paths of the power switches as shown in Fig. 3 (a). In order to reduce the absolute negative current flowing back to the power source, which indicates a power loss, and to suppress EMI due to LX oscillation, a freewheel switch is usually used as in Fig. 3 (b) [2][5][7][8]. The operation of this freewheel switch also can be seen in Fig. 3 (b): After zero inductor current is detected, both two power switches will be turned off, and the freewheel switch is turned on, providing a current path for the negative inductor current to flow back to VOUT. By doing so, the negative inductor current can be reduced; thus, lowering the power loss.

The proposed ZCD circuit will also employ these two important ZCD circuit parts in its design.



(a)



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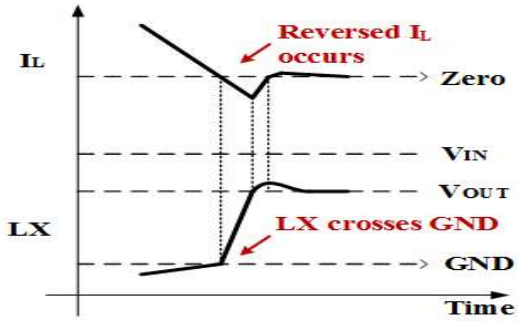


(c)

Fig. 3. Effect of using freewheel switch to re-direct negative inductor current back to load side: (a) When VLX < VOUT, (b) When VLX > VOUT, (c) Timing diagram

A. The proposed zero current detection

Shown in Fig. 4 is the overall architecture of the proposed ZCD circuit. The main detection circuit is based on the conventional ZCD, in which zero inductor current crossing point is detected by comparing LX voltage node to ground. In order to avoid false ZCD detection at node LX, a proposed positive rising edge SR flip-flop is added to mask the zero current detection noise and to avoid conflict function with adaptive dead-time control using LX information such as in [12]. Detailed of the proposed structure for the positive rising edge SR flip-flop will be discussed in section 3. 2. Detailed of the ZCD comparator and its preamplifier are also shown in section 3. 3.

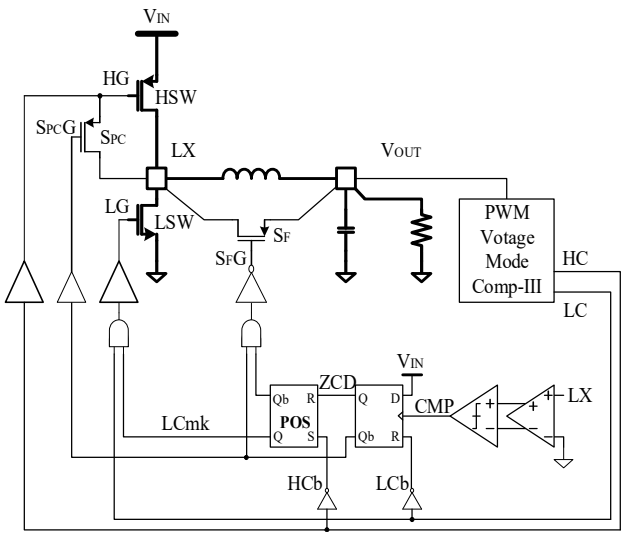


Fig. 4. The proposed ZCD circuit tested in PWM voltage mode buck converter with on-chip compensation type III.

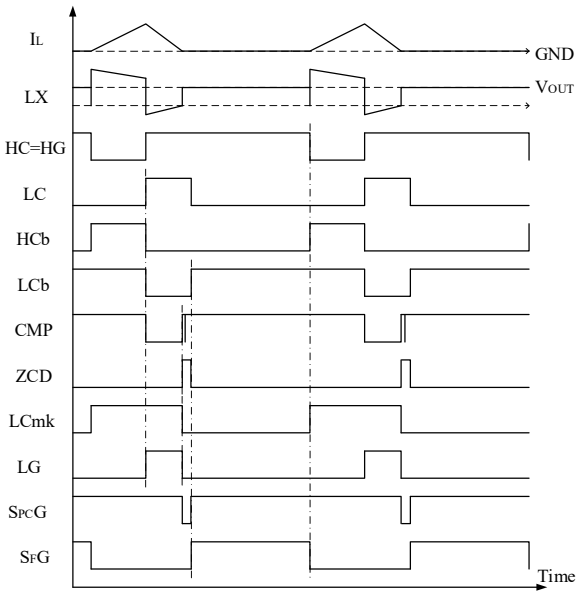


Fig. 5. Waveform of the ZCD control signals at light load in two DCM/PFM periods.

In order to enhance the time-response of the freewheel switch to operate correctly, i.e. to conduct and re-direct negative inductor current back to the load side, a proposed pre-charged switch SPC will be used to pre-charge for node LX to rise faster after the zero inductor current event is detected. The gate control for this switch SPC is also shown in Fig. 4.

Shown in Fig. 5 is the waveform of the ZCD control signals generated from the proposed circuit in Fig. 4. According to the ZCD control scheme, a noisy ZCD detection signal will be masked until the beginning of the next switching period, using a proposed positive rising edge SR flip-flop. The high side switch conduction period is decided by the PFM duty detection. Then the low side switch conducts until the ZCD signal is triggered. Pre-charged switch SPC will work for a short time period to pre-charge LX voltage node to increase from ground voltage potential to VOUT level; then, free-wheel switch SF will conduct to re-direct negative inductor current flowing to the supply power side back to the load side. Hence, the absolute negative inductor current can be diminished.

B. The proposed SR flip-flop used in the proposed ZCD and the SR latch for the PWM and PFM control

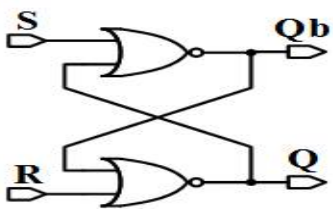
The simple structure of SR latch for PWM and PFM detection and the proposed positive rising edge SRFF for the proposed ZCD circuit are shown in Fig. 6 (a) and (b) respectively. Because the period of PFM can be long in order to save energy, positive feedback loops M1-IV1 and M2-IV2[9] are necessary to compensate for the discharged charge loss at latch phase of the positive rising edge flip-flop. The reference transistor size is given in TABLE 1. To diminish transistor mismatch during manufacturing, an SR flip-flop with a larger scaling size according to this table is still able to work, with expected slower speed due to larger parasitic capacitors.

TABLE I.
Transistor parameters of the proposed positive rising edge SR flip-flop

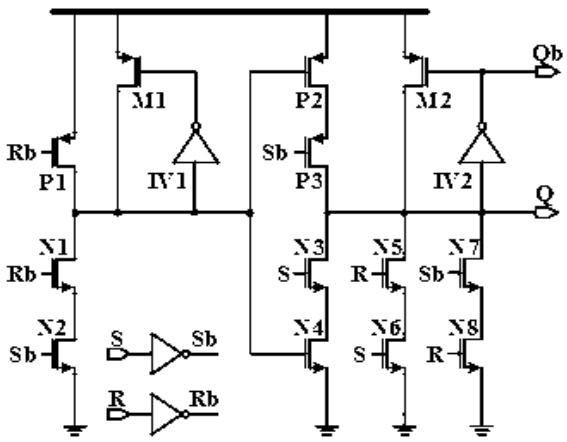
Transistor name	Transistor size W/L[um/um]
P1	1.2/0.5
P2, P3	2.4/0.5
M1, M2	0.6/1.0
N1~N8	1.2/0.6
IV1 PMOS, IV2 PMOS	1.2/0.5
IV1 NMOS, IV2 NMOS	0.6/0.6

TABLE II.
Timing characteristics of the proposed positive rising edge SR flip-flop and the conventional SR latch

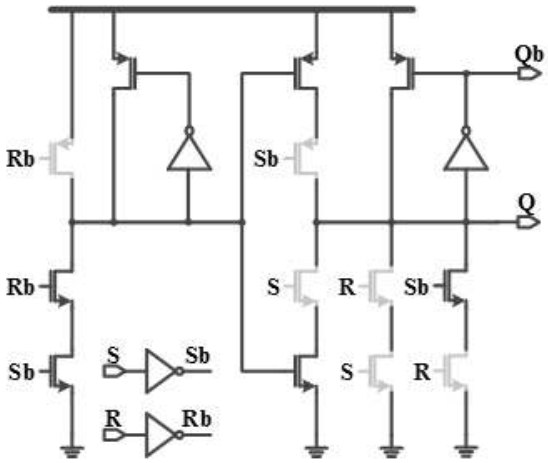
Positive Rising Edge SRFF	00	Q_{prev}	Hold
	0↑	0	Reset
	↑0	1	Set
	↑↑	-	Not allowed
Conventional SR Latch	00	Q_{prev}	Hold
	01	0	Reset
	10	1	Set
	11	-	Not allowed



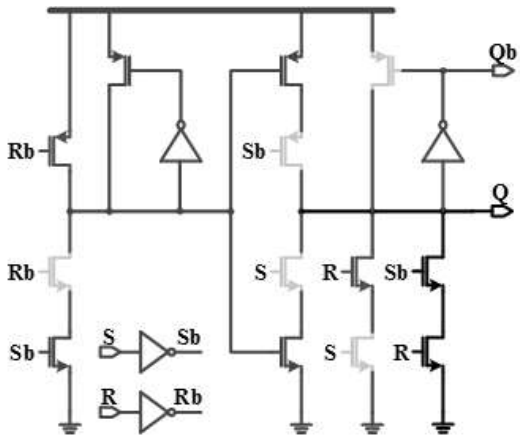
(a) Conventional SR latch



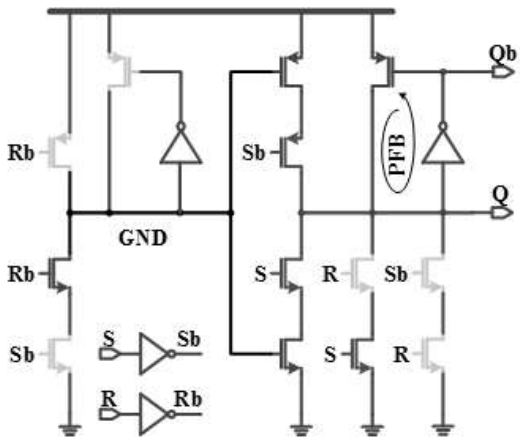
(b) Proposed Positive Rising Edge SR flip-flop



(c) Proposed Positive Rising Edge SR flip-flop: SR = 00



(d) Proposed Positive Rising Edge SR flip-flop: SR = 0↑



(e) Proposed Positive Rising Edge SR flip-flop: SR = ↑0

Fig. 6. (a) Conventional SR latch used in PWM control, and (b)~(e) Proposed Positive Rising Edge SR flip-flop used in ZCD circuit.

The operation of the proposed SRFF is illustrated in Fig. 6 (c) ~ (e), and the timing characteristics of the proposed positive rising edge SRFF and SR latch are summarized in TABLE 2.

C. The ZCD comparator with pre-amplifier

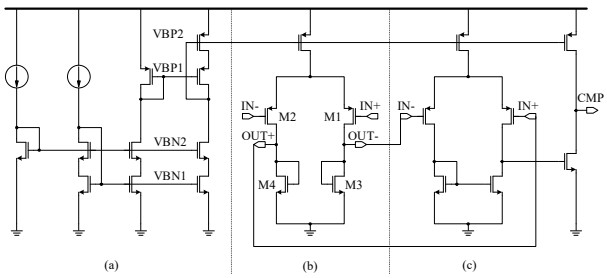


Fig. 7. ZCD comparator with pre-amplifier: (a) Wide-swing bias circuit; (b) pre-amplifier; (c) comparator.

Fig. 7 shows the schematic of the ZCD comparator with a simple preamplifier structure. Fig. 7 (a) is the bias voltage circuit used for the ZCD comparator and the pre-amplifier. The bias circuit uses the wide-swing constant transconductance bias circuit structure [1] for the converter to be able to work in a wide range of input voltage supply. This bias circuit is also used for bias voltage supply for the other circuit block of the converter such as the error amplifier, and other comparator. Fig. 7 (b) shows a simple preamplifier which is usually used in high-speed ADC/DAC comparator. The gain of this preamplifier is:

$$A_V = \frac{g_{m1}}{g_{m3}} \tag{2}$$

Finally, Fig. 7 (c) shows the main structure of the comparator. For manufacturing consideration, one may consider to implement offset voltage cancellation to reduce offset variation of the comparator comes from transistor mismatch.

IV. SIMULATION RESULTS

A. The proposed zero current detection

The proposed ZCD circuit is simulated for a PWM voltage mode buck circuit, with input voltage from 2.2V to 5.5V, to get output voltage from 1V up to 90% of input voltage, using a 0.18μm CMOS process. The PWM switching frequency is 2MHz, using converter switches with ON resistance RON of 300mΩ, inductor filter with inductance value of 1.1μH and capacitor filter with capacitive value of 10μF and equivalent series resistance of 20mΩ, for load current below 300mA. For design under higher load current condition, reducing ON resistance of the switches, decreasing switching frequency and increasing filter inductance are necessary to get the conversion efficiency of higher than 90% (typical acceptable conversion efficiency of DC-DC converter). For the comparison purpose between the proposed ZCD's performance and the conventional ZCD's performance, forced DCM operation at 2MHz switching frequency is simulated to get the

simulation results as shown in Fig. 8 and Fig. 9. In addition, the normal operation of the converter using both PFM and PWM is also simulated to obtain the simulation results in Fig. 10 and Fig. 11, with input voltage of 3.3V and output voltage of 1.8V.

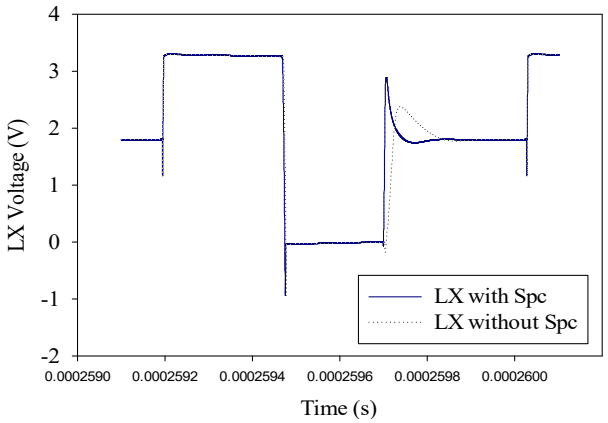


Fig. 8. Simulated DCM LX voltage node in a period for the PWM switching frequency of 2MHz.

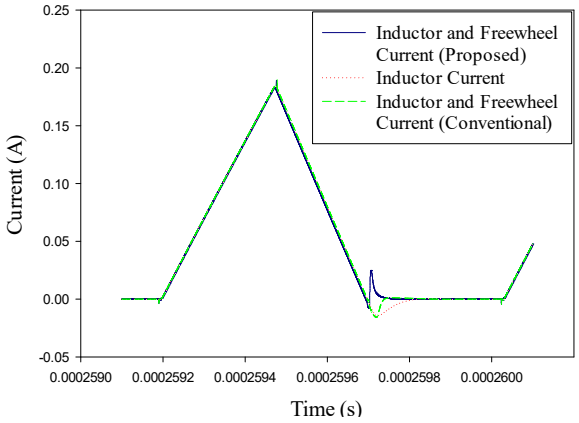


Fig. 9. Simulated DCM inductor current curve in a period for the PWM switching frequency of 2MHz.

Fig. 8 and Fig. 9 show comparisons between the proposed ZCD and the conventional ZCD under the same test condition: The conventional ZCD is implemented using the same detection circuit including comparator type, flip-flops and latches type, and buffer type, except the part related to the pre-charging switch SPC compared to the proposed ZCD. The solid line and the dot line shown in Fig. 8 are the LX voltage waveform using the proposed ZCD and the normal ZCD, respectively. At the zero current crossing point detected, using the proposed ZCD with the pre-charged switch SPC, rising time of LX node is faster compared to that from the normal ZCD without the pre-charge switch SPC. Shown in Fig. 9 are: (1) the inductor current in dot red waveform; (2) the summation of the inductor current and freewheel switch current for the proposed ZCD in solid blue line; and (3) the one for the conventional ZCD in dashed green line. With the help of the pre-charge switch SPC as in the proposed ZCD, the LX voltage node rises faster. Therefore, the freewheel switch can operate faster, and the corresponding total current of inductor current and freewheel switch current from the proposed ZCD is much smaller: The maximum absolute negative inductor current reduces from 18mA to 8mA. Furthermore, peaking inductor current at the ZCD detected can be brought down by reducing size of the pre-charged switch SPC, with the price of increasing the maximum absolute negative inductor.

Shown in Fig. 10 is the simulation result of maximum absolute negative inductor current under different load conditions from 20mA to 120mA, when the system works in PFM mode, using the proposed ZCD. The simulation shows that the maximum absolute negative inductor current value is quite stable when the load current varies.

Finally, shown in Fig. 11 is the simulated conversion efficiency of the proposed ZCD compared to that of the conventional ZCD: The simulation result indicates an overall improvement of efficiency in PFM, and almost the same efficiency in CCM. Maximum efficiency improvement is 6.9% at 40mA load current. There is an abnormal high efficiency point from the conventional ZCD due to low PFM switching frequency required for very light load of 20mA. Contradictorily, not much efficiency improvement coming from the proposed ZCD compared to the conventional one at this current load point is due to additional power consumption for the additional components (the pre-charged switch SPC and the pre-charged switch's driver). For this reason, there is no benefit of obtaining lower than 8mA of maximum absolute negative inductor current because the efficiency will be worse. Table 3 shows the performance summary of the proposed ZCD as compared to the previous report. The simple proposed ZCD shows better conversion efficiency, despite the absolute reversed current is implemented as lower.

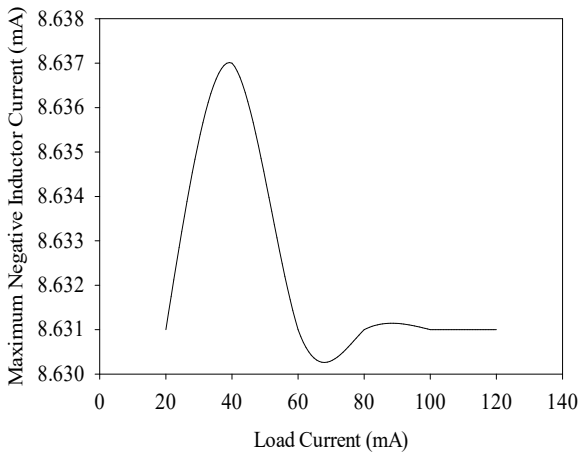


Fig. 10. Simulated maximum absolute of the negative inductor current by the proposed ZCD when load current varying.

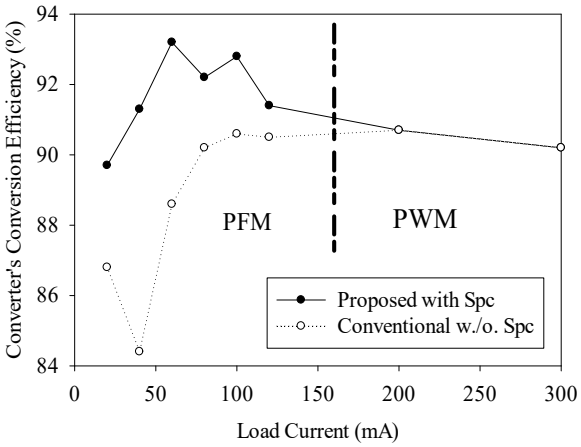


Fig. 11. Simulated efficiency of the converter using the proposed ZCD: PFM is detected under load condition below 120mA; PWM with switching frequency of 2MHz is detected under load condition above 200mA.

TABLE III.

Perfomance summary

	[8]	[10] This work
Year	2012	2014
Technology	0.18um CMOS	
Absolute Reversed Current	8.1 mA	8.6 mA
Efficiency for load current from 20mA to 120mA	max 92.87%	max 93.2%
	min 85%	min 89.7%

B. The overall buck converter operation

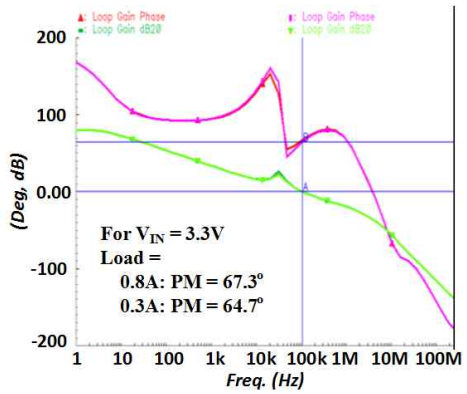
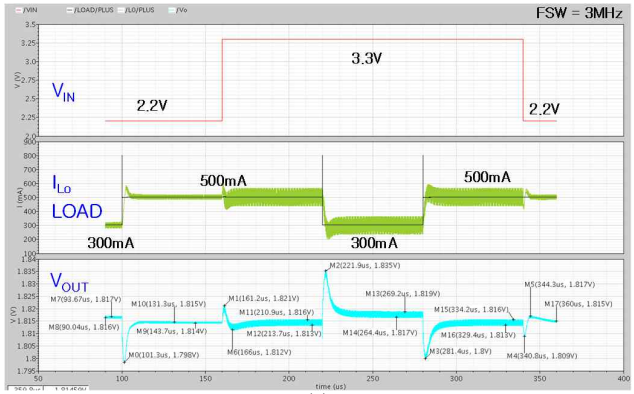
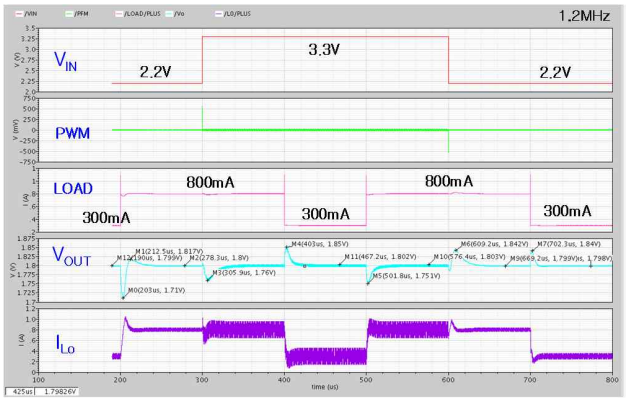


Fig. 12. Simulated loop gain of the buck converter.

In addition to the typical operation specified in section 4.1, the buck converter is designed to be able to work well for a wide range of DC input voltage, a wide range of output load current, and a wide range of switching frequency. The compensation components for error amplifier (Fig. 1 (b)) is designed according to the guideline in [4] The corresponding simulated loop gain is shown in Fig. 12. According to the simulation results, for VIN = 3.3V and VOUT = 1.8V, phase margin is 67.3o and 64.7o, corresponding to the load current of 800mA and 300mA.



(a)



(b)

(c)

Fig. 13. Load line regulation of the buck converter: (a) For switching frequency of 3MHz, (b) For switching frequency of 1.2MHz, (c) For switching frequency of 800kHz

For the PWM operation, load line regulation is implemented for VIN changing from 2.2V to 3.3V, and load current change from 300mA to 800mA as shown in Fig. 13 (a) ~ (c). Considering about DC operation, lower frequency gives more correct regulation for this implementation. For the load line changes, higher frequency gives lower voltage droop, which is preferred in converter. In addition, high switching frequency gives smaller inductor current ripple for the same operation condition.

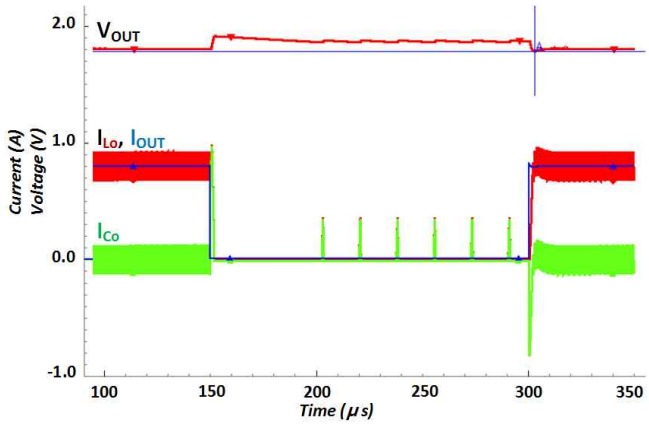


Fig. 14. Ideal implementation of PWM, PFM mode change.

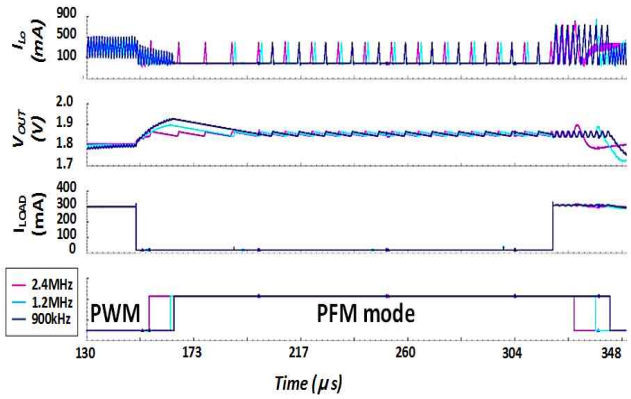


Fig. 15. Counter implementation of PWM, PFM mode change.

The operation of PWM and PFM changing mode was implemented as described in section 2. According to this implementation, VOUT at PFM mode is raised up about 60mV compared to the target of PWM, so that the output voltage drops when mode changes from PFM back to the normal condition PWM is negligible. Shown in Fig. 14 is the ideal mode change according to this implementation, in which "ideal" means mode when current changes to defined value, mode also changes immediately.

However, also described in section 2, at the margin condition of changing mode, the converter will continuous switching from PWM mode to PFM mode and vice versa, resulting a large irrelevant output voltage ripple. In order to ease this effect, a counter is implemented to set up a prerequisite time to determine if the converter should change its mode or not. Shown in Fig. 15 is the simulation results for the mode change with the counter implementation, with the PWM switching frequency of 2.4MHz, 1.2MHz, and 900MHz. According to the simulation result, although the PWM switching frequencies are different in three cases, when mode changes to PFM, the steady-state operation for the same load condition has the same PFM switching frequency in all three cases, with the same output voltage ripple. However, with the counter operation, lower PWM switching frequency change mode slower compared to higher PWM switching frequency, resulting higher output voltage droop which is undesigned in common converter operation.

For the soft-start implementation, the buck converter uses the same concept of fast soft-start as described in [11]. Shown in Fig. 16 is the simulation result of this implementation.

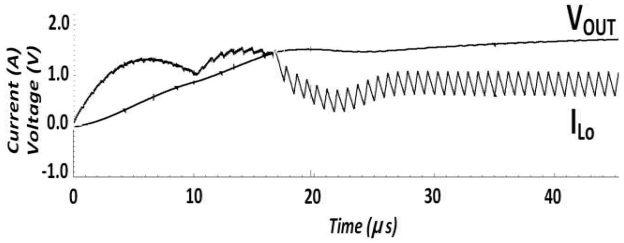


Fig. 16. Implementation of fast soft-start.

V. Conclusions

A zero current detector with forced freewheel switching operation by pre-charging LX node was proposed and simulated for a voltage mode compensation type III buck converter, using a 0.18μm CMOS process. According to the simulation result, the proposed ZCD scheme does not affect the stability of the PWM compensation at heavy load in CCM, and shows an absolute overall power conversion efficiency improvement in PFM, with a maximum efficiency improvement of 6.9% at 40mA. The overall efficiency is higher than 90% for load current from 40mA to 300mA, and 89.7% for load current of 20mA. The buck converter uses PWM switching frequency of 2MHz, with 1.1μH filter inductor, 10μF filter capacitor, and two power switches each with ON resistance of 300mΩ. For design with heavier load current (above 300mA), lower switching frequency with higher filter inductor's value, and lower ON resistance of the power switches should be considered to get higher efficiency.

In addition to the designed ZCD testing purposed, the buck converter used in this paper is also stable and is able to work under a wide range of VIN from 2.2V to 3.3V, a wide range of load current below 800mA, and a wide range of switching frequency from 3MHz to 800kHz.

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