

A hysteretic buck converter with fast transient response

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Abstract - A current-mode hysteretic buck converter is described in which inductor current is sensed by an RC network. The inductor current sensing RC network is reset multiple times per switching clock period. The multiple reset allows the RC network to have time constant much smaller than switching clock period and therefore occupy small silicon area. The multiple reset also removes DC-output offset which is dependent on load current and improves the load transient property. The current-mode hysteretic buck converter is implemented in a 65-nm CMOS process and the converter operates in 0.6~2.0-V output from 3.3-V input with 1.5-A maximum load current. The recovery time for step-up load transient is 3.4- μ s under 0.9-A/0.1- μ s load change and the measured peak power efficiency is 96.3-%.

Keywords – Current-mode hysteretic buck converter, DC-out offset dependent on load current, Multiple reset operation

I. INTRODUCTION

Recently, as the demand for portable devices increases, the various applications including RF circuit, LED display and memory are integrated on a single chip. Each application requires reliable supply voltage for its performance. Thus, the power management IC (PMIC) is required for providing reliable supply voltage to the each application with high power efficiency and high transient speed.

The switched-inductor DC-DC converter is known to provide the best possible power efficiency among various types of DC-DC conversion topologies. The control scheme of the converter determines its general property such as transient response, regulation accuracy and chip-area. The PWM control scheme usually shows slow transient response and requires large chip-area due to its frequency compensation network. Whereas the hysteretic control scheme has area-effective and immediately respond property when a step-up load transient or step-down load transient occurs because it operates only with a hysteretic comparator and no passive frequency compensation network is required. However, for voltage-mode hysteretic control, the output ripple of a DC-DC converter must be large enough, and the

output capacitor requires large equivalent series resistance (ESR). To ensure that the converter doesn't have large output ripple, hysteretic control can be performed with the ramping inductor current waveform of a DC-DC converter. [4]. This type of control technique, called current-mode hysteretic control, is typically implemented with an inductor current sensor, which is usually realized an RC network across inductor. In the current-mode hysteretic converter, the time-constant of inductor current sensing RC network determines the switching frequency and require large silicon area for the switching frequency below 1-MHz. Also, the series resistance $R_{DCR,L}$ of the inductor causes a large DC output error dependent to load current.

Several hysteretic converters have been studied in [1]-[3]. But the converters do not fully resolve those problems. In [1], by adding AC-coupling capacitor, DC-offset is mostly removed. However, the converter requires large chip-area for AC-coupling capacitor and has slow transient response due to the low-pass filtering of βV_O by R_C and C_C . In [2] and [3], based on error voltage feedback control, DC-offset is removed. But, the converter also has slow transient response due to the integrator for error voltage feedback, especially in large load step change.

This paper discusses a current-mode hysteretic buck converter where the inductor current sensing RC network is reset multiple times per switching clock period. With the multiple reset operation, the inductor current sensing RC network could have much smaller time constant for achieving the same switching frequency. Section II describes architecture of the proposed current-mode hysteretic converter. The circuit implementation and the experimental results are given in section III and IV, respectively. Finally, Section IV concludes this paper.

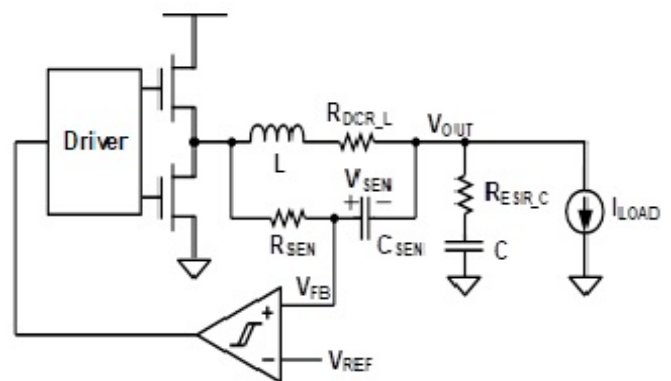


Fig. 1. Structure of conventional hysteretic buck converter with current-mode control

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Manuscript Received Mar. 06, 2018, Revised Mar. 15, 2018, Accepted Mar. 29, 2018

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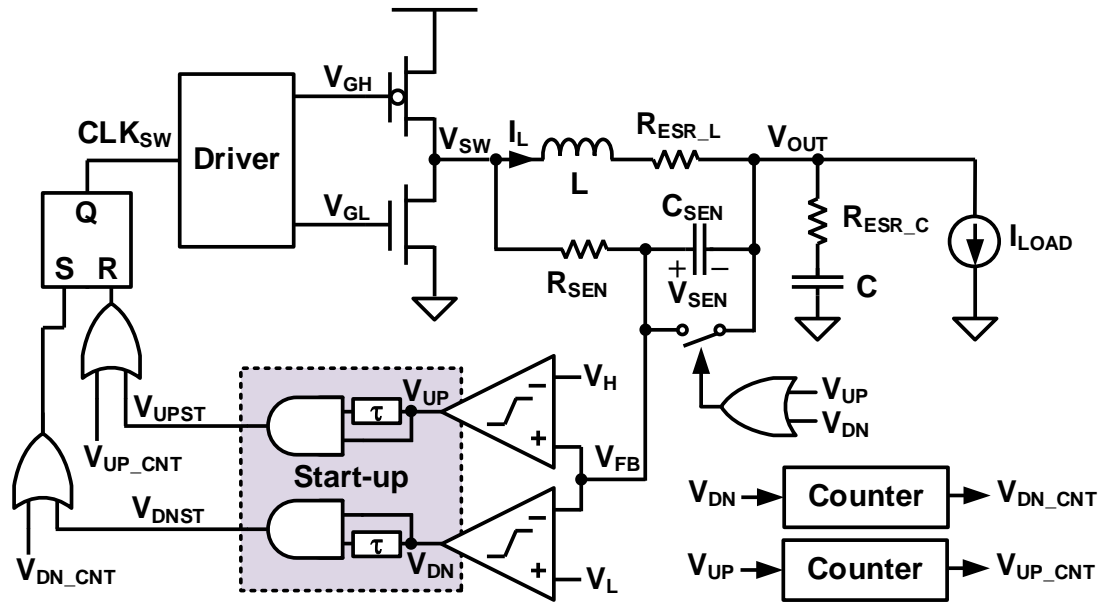


Fig. 3. Proposed current-mode hysteretic buck converter

II. THE PROPOSED CURRENT-MODE HYSTERTIC CONVERTER

Fig. 1 shows the block diagram of the conventional hysteretic buck converter with current-mode control. Its controller is composed of one hysteretic comparator, RC network and the drivers. The feedback signal V_{FB} is locked between hysteretic reference levels V_H and V_L shown in Fig. 2. The converter switches power transistor when V_{FB} touches either V_H or V_L . The current-mode hysteretic structure was adopted in Fig.3, which is block diagram of the proposed current-mode hysteretic converter. Unlike the previous works [1]-[3], the power transistors of the proposed hysteretic converter are switched after V_{FB} touches V_H or V_L three times consecutively as shown in Fig. 4. The inductor current sensing RC networks is reset three times by V_{UP} to turn on the nMOS power transistor M_N and reset three times by V_{DN} to turn on the pMOS power transistor M_P . When the

feedback signal V_{FB} touches either V_H or V_L , the capacitor C_{SEN} of the inductor current sensor is shorted and reset, removing the DC-offset problem of RC-network caused by R_{DCR_L} . In addition, the multiple-reset of the inductor current sensing RC network would occupy a smaller silicon area, with the time constant $R_{SEN} \times C_{SEN}$ of the inductor current sensor to be much smaller than the switching clock period $T_{SW}(=T_{ON}+T_{OFF})$. The simulated steady-state waveforms of the proposed hysteretic buck converter are shown in Fig. 5 when input voltage $V_{IN} = 3.3\text{-V}$, output voltage $V_{OUT} = 2\text{-V}$ and load current $I_{LOAD} = 0.5\text{-A}$. The power transistors of the converter are switched after V_{UP} or V_{DN} is generated three times consecutively. With the multiple-reset operation, the DC-offset which is proportional to load current is removed.

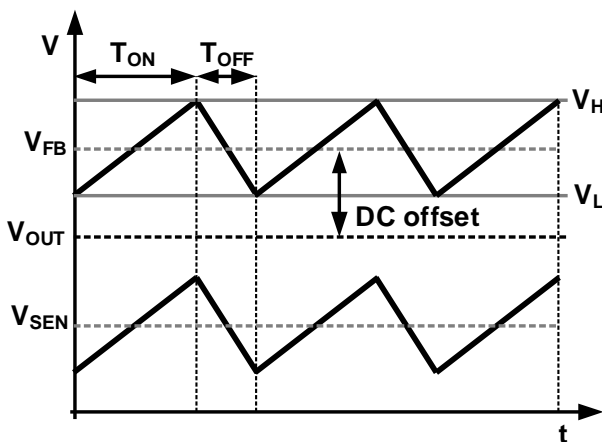


Fig. 2. Waveforms of the conventional hysteretic buck converter with current-mode control.

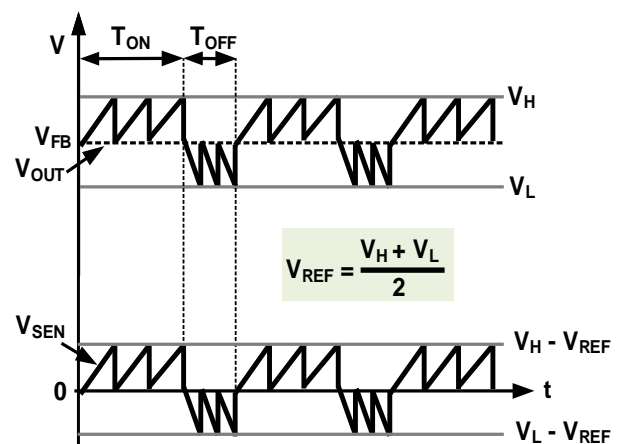


Fig. 4. Waveforms of the conventional hysteretic buck converter with current-mode control.

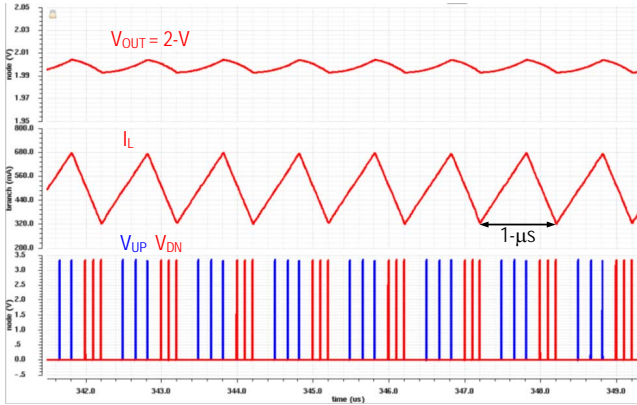


Fig. 5. Simulated steady-state waveforms of the proposed hysteretic buck converter.

III. CIRCUIT IMPLEMENTATION

A. Driver.

The schematic of driver is shown in Fig. 6. To prevent the short through current in the synchronous converter, the dead-time circuit split the duty cycle signal CLK_{SW} into two non-overlapping signal V_N and V_P , which control nMOS power transistor and pMOS power transistor respectively. The dead-time is controlled by capacitance C_1 and C_2 . Charging time and discharging time of which determines non-overlapping time between V_N and V_P . The dead-time is long enough to ensure that there is no turn on of the nMOS power transistor and pMOS power transistor simultaneously. The inverter chain is used for driving the large gate capacitance of the nMOS power transistor and pMOS power transistor and generates gate driving signal V_{GL} and V_{GH} .

B. Comparator

The schematic of the comparator is illustrated in Fig.7. The performance of the comparator dominantly effects to the output voltage of the hysteretic converter. The comparator adapts two-stage amplifier structure for the fast comparison between two inputs, V_{INN} and V_{INP} . In addition, the input transistor for the comparator is based on pMOS that support the input range of the comparator from 0.6-V to 2.0-V in the supply voltage of 3.3-V.

C. Start-up

When the output voltage V_{OUT} is outside the window defined by V_H and V_L at start-up, for example, either one of the comparator outputs V_{UP} and V_{DN} is HIGH for a long time but neither V_{UP_CNT} nor V_{DN_CNT} is generated, meaning no switching of the power transistors. To ensure the switching of the power transistors even at this condition, the start-up block in Fig. 3 generate the pulses V_{UPST} and V_{DNST} with the comparator outputs V_{UP} and V_{DN} , respectively when the pulse widths of V_{UP} and V_{DN} are larger than τ . The magnitude of τ has to be larger than the pulse widths of V_{UP} and V_{DN} generated during normal operation to avoid the false switching of the power transistors.

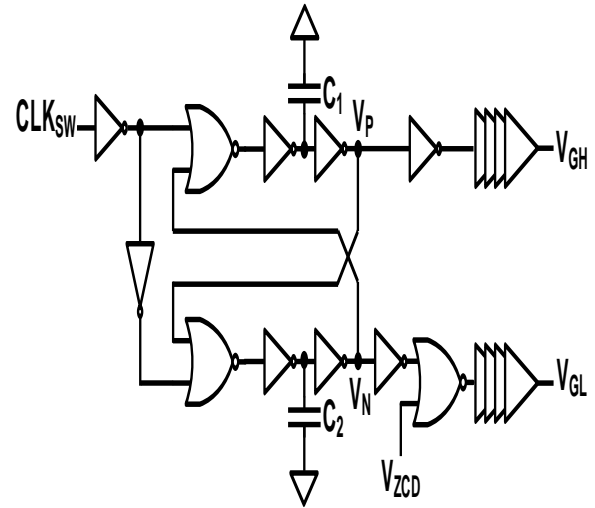


Fig. 6. The schematic of driver

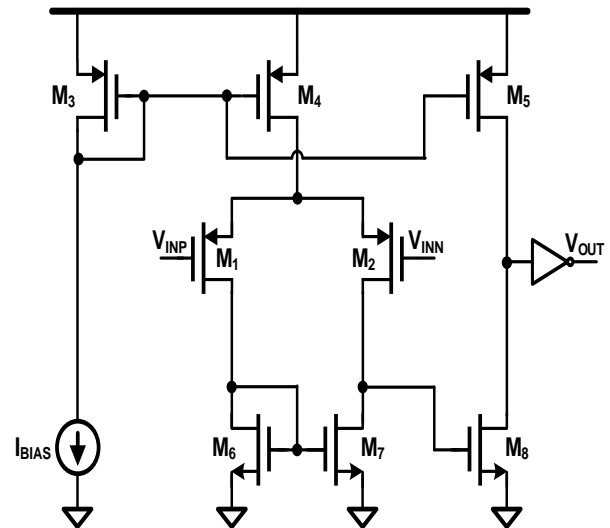


Fig. 7. The schematic of comparator

IV. EXPERIMENTAL RESULT.

The proposed current-mode hysteretic buck converter has been implemented in a 65-nm CMOS process. The inductor and output capacitor are 2.2- μ H and 10- μ F, respectively. The converter operates at a 3.3-V input voltage. The output voltage ranges from 0.6-V to 2.0-V with 1.5-A maximum load current. At the step-up load transient from 200-mA to 1.1-A and inclination of 900-mA / 0.1- μ s, the output voltage is recovery to desired level in less than 3.4- μ s as shown in Fig.8. The measured power efficiency is plotted versus the load current in Fig. 9. The peak power efficiency is 96.3-% when the load current is 300-mA and the output voltage is 2.0-V. The performance of the proposed converter is summarized and compared with other hysteretic converters in Table I.

Table I. Performance summary

	[1]	[2]	[3]	This work	
Technology	130-nm CMOS	350-nm CMOS	350-nm CMOS	65-nm CMOS	
Control scheme	Hybrid-mode hysteretic	Quasi-V ² hysteretic	Quasi-V ² hysteretic	Current-mode hysteretic	
Active area [mm²]	0.7	-	0.884	0.78	
Input voltage [V]	2.5	2.7~3.3	2.7~4.2	3.3	
Output voltage [V]	0.7 ~ 1.8	0.9~2.1	1.2	0.6~2.0	
Inductor [μH]	1.8	2.2	2.2	2.2	
Output capacitor [μF]	10	4.4	10	10	
Controller capacitor	50	50	10	-	
	None	None	330	-	
Max. load current [A]	0.9	0.5	0.7	1.5	
Peak efficiency [%]	93.0	93.0	95.65	96.3	
Load transient	Current step [mA]	600	450	300	
	Step-up/step-down recovery time [μs]	< 10 @ V _{OUT} =1.2-V	2.4/2.8 @ V _{IN} =3-V, V _{OUT} =0.9-V 10/7.2 @ V _{IN} =3-V, V _{OUT} =2.1-V	3.0/5.0 @ V _{IN} =3.3-V	3.4/3.6 @ V _{OUT} =2-V
	Undershoot/overshoot [mV]	61/72 @ V _{OUT} = 1.2-V	38/45 @ V _{IN} =3-V, V _{OUT} =0.9-V 72/40 @ V _{IN} =3-V, V _{OUT} =2.1-V	48/30 @ V _{IN} =3.3-V	106/87 @ V _{OUT} =2-V

IV. CONCLUSION

This paper describes a current-mode hysteretic buck converter in which the inductor current is sensed by an RC-network. The multiple-reset of the inductor current sensing RC network reduces silicon area, with the time constant of the inductor current sensor to be much smaller than the switching clock period. In addition, the reset operation removes DC-out offset dependent on load current. The hysteretic buck converter is implemented in a 65-nm CMOS process. The converter operates at a 3.3-V input voltage. The output voltage ranges from 0.6-V to 2.0-V with 1.5-A maximum load current. The peak power efficiency is measured to be 96.3-%.

ACKNOWLEDGMENT

The CAD tools were provided by the IC Design Education Center (IDEC), Korea

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linear RF transmitters.