16-PSK baseband Modem Design for Data Communication

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***Abstract* – This paper shows the design of low-power 16-PSK modem that requires high-speed data transmission with limited bandwidth and power. The proposed structure is comprised of modulator and demodulator. In order to reduce the error between neighboring phase symbols in the detection process of symbol, bits of each phase symbol are converted into Gray coded bits. And in order to reduce the interference effect on the adjacent channel, the rectangular signal of 16-PSK modulated symbol is smoothed as rounded shape through the LPF. The LFP consists of 33 taps through simulation which shows the approximation with low truncation error. The modem with the above-mentioned design is implemented by the MagnaChip/SK Hynix 0.35μm process. The supply voltage and the maximum operating frequency in modem is respectively 3.3V and 20MHz.**

I. INTRODUCTION

In the data communication system, the modulator and the demodulator transmit and receive data processed in the embedded system. It is required to make an optimum design of modem with low BER under the limited condition with bandwidth as well as power.

M-ary PSK modem is adopted as the modem which is suitable for the transmission media which does not have enough bandwidth. In the fading environment, M-ary PSK modem is preferred as better robust transmission method than M-ary QAM.

In this paper, a 16-PSK modem designed, which consists of (1) modulator with Gray code module, symbol mapping and wave-shaping filter (2) demodulator with symbol decision, symbol demapper and Gray decode module. The designed modem has baseband modulator and demodulator, where DA, AD and RF circuit part is not included. And for high-speed data transfers, parallel processing will be used. In addition, the multiplier used in the modulator occupies a lot of areas, resulting in circuit delays and degraded operations. To solve this problem, the solution with more simple design is proposed.

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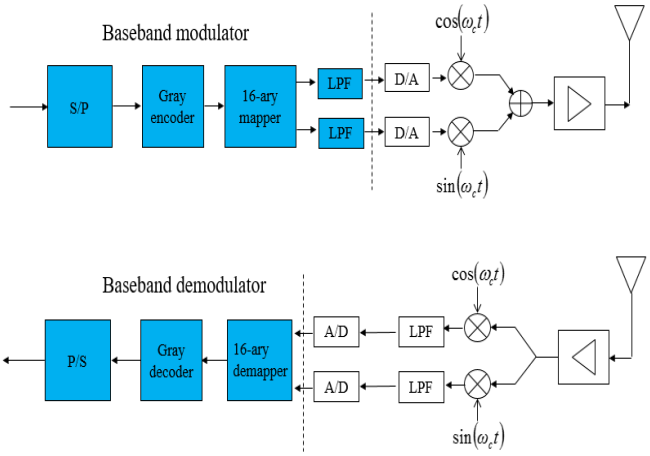

Fig. 1. 16-PSK baseband modem structure.

The structure of the proposed 16-PSK modem consists of baseband modulator and baseband demodulator as shown in Fig. 1.

If serial data continuously enters into the baseband modulator, every group of 4 consecutive serial bits data is converted into 4 bits parallel data bus in serial to parallel conversion circuit. In order to reduce errors between the neighboring phase symbols, 4 bits in each phase symbol are Gray coded in the Gray encoder. The 4 bits in the Gray coded symbol is mapped to one of 16 symbols whose in-phase magnitude and quadrature magnitude with 8 bits are in memory. And each in-phase magnitude and quadrature magnitude is filtered respectively through wave-shaping LPF in each in-phase/quadrature branch for reducing the interference effects to adjacent channel.

The received symbols should be decided correctly in demodulator for restoring data transmitted from the baseband modulator. Because DA and AD are not included in this design, those 8 bits data processed in LPF at modulator are connected directly to decision device at demodulator. The decision device in in-phase branch as well as quadrature branch discriminates respectively every received in-phase signal as well as quadrature signal with 3 threshold values and sign bit. The determined data in each in-phase branch and quadrature branch is combined and decoded through Gray decoder. And those decoded parallel 4-bits data converted into serial bits stream in parallel to serial converter. The bit error rate (BER) varies depending on the environment and the modulation method used during the PSK transmission. Therefore, the modulation methods have to be determined with this in mind. The M-ary PSK performance can be judged based on the probability of bit

errors. The probability of M-ary bit error is expressed by the following equation [1].

$$M-ary\ \ BER\ \ = \frac{1}{\log_2 M}\sum_{i=1}^{\frac{M}{2}}(w_i')p_i \qquad (1)$$

Equation (1) represents the probability of M-ary bit error. It is $w_i' = w_i + w_{M-i}$, $w_{\frac{M}{2}}' = w_{\frac{M}{2}}$ and w_i is the hamming weight value assigned to i [1], [2]. If there is error in symbol with 4 bits, one bit or 4 bits in worst case in symbol may be error. Because there is probability that symbol can be mistaken as neighboring symbol, 4 bits in each symbol is encoded using Gray coding rule. This Gray encoding makes error reduced to be compared with transmission without Gray encoding process.

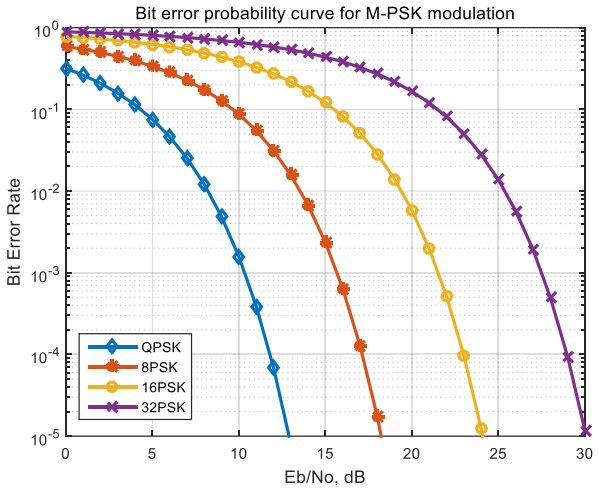

Fig. 2. M-ary PSK bit error rate.

Fig. 2 shows the bit error probability according to M for Equation (1) using MATLAB. When a larger PSK is used for M, there is a higher probability of error than when a smaller PSK is used [3], [4]. From these results, it is required to increase more the magnitude of symbol in higher M-ary PSK than lower M-ary PSK. In the design of 16 PSK baseband modem, LPF with arithmetic process such as multiplication includes more complexity than other logical block. Therefore, it is necessary to select the number of bits which represents the design parameter such as LPF coefficients and taps.

In this paper, the 33 taps of LPF are used. And for reducing complexity, the appropriate truncation process is selected. By comparing the repeated simulation results with theoretical result, the design parameter which satisfies the performance requirements could be selected. This paper describes the detailed structure of 16-PSK modem in chapter II. The chapter III explains the simulation results and the conclusion is written on chapter IV.

II. EXPERIMENTS

A. Baseband modulator

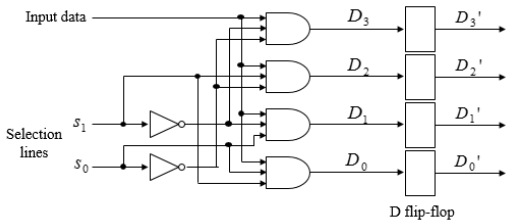

Fig. 3. Serial to parallel converter.

Fig. 3 shows a serial to parallel converter that converts serial data to parallel data. When continuous signals are entered, the selection line makes input serial data to be converted into parallel data. Converting serial bits into 4-bit parallel data makes it possible more high-speed data to be transmitted with the given limited bandwidth [5].

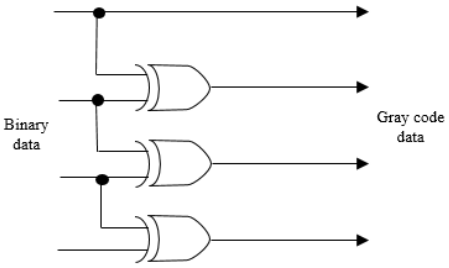

Fig. 4. Gray encoder.

In Fig. 4, shows a Gray encoder that converts the output from Fig. 3 into Gray code. As mentioned in introduction, the probability of decision error between neighboring symbols is higher than other case. Therefore, it is optimum to assign bits with one bit difference between neighboring symbols, which makes at most 1-bit error even though there is symbol errors between them [6]. In order to solve such problems, we will produce Gray code using a XOR gate as shown in Fig. 4. It is possible to improve the performance of 16-PSK by using the produced Gray code.

Gray coded data is entered to the stored address of the 16-ary mapper composed of in-phase data and quadrature data. The phases value allows the symbol to be mapped to the corresponding data represented according to the position of the phase. The represented data consists of 8 bits and is stored in the memory. When the encoded data are entered to the address bus in the memory, the stored value is produced. Considering the conditions for constructing an 8-bit data used in the 16-ary mapper, floating-point and fixed-point operations can be used when calculating decimal points in the hardware. To improve the accuracy of this design, a floating-point hardware design has to be implemented. However, accurate calculations consume a lot of power because they consume more hardware than fixed ones [7]. Fixed points are used in the 16-ary mapper in order to solve the problems mentioned. And in 16-ary mapper, the position where the 16 symbols are formed will be converted and saved as fixed points. By carrying out this method for processing data, the design area can be reduced.

When the in-phase data and quadrature data output from the 16-ary mapper are directly transmitted to the receiver, side-lobe spectrum may be overlapped with the adjacent channel's spectrum which causes error to be generated.

Because the data with rectangular waveform has high-frequency signal which is side-lobe spectrum, it is necessary to make rectangular form rounded form with wave-shaping filter. Therefore, the input data is passed through the LPF to remove the side lobe which is a noise component.

$$h(t) = \frac{cos(2\pi\beta t)}{1-(4\beta t)^2} \times sinc\left(\frac{t}{T}\right) \quad (2)$$

Equation (2) represents the filter's impulse response signal of the LPF [8]. The filter's performance will vary on β. β with 0 is not used because the impulse response of filter shows a sinc function with long side-lobe in frequency domain. In this paper, we used $\beta = 0.25$, which has a small side lobe [1]. When MATLAB simulation is performed, errors occur when t is 0, so sampling was performed at intervals of 0.25 with a difference of -0.000001 between -4 and 4, which is the range of t. Thus, the filter factor result is 33 taps.

In a general LPF, the number of bits increases during a convolution. As the number of bits increases, the area of the hardware increases and much power is consumed.

In this paper, we propose an LPF structure that minimizes noise using the 33 taps and adds lower bit truncation processes during the intermediate convolution operation.

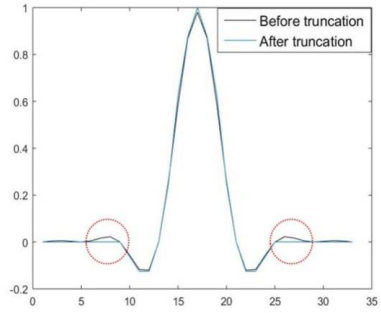

Fig. 5. Before and after truncation process.

Fig. 5 shows the MATLAB simulation results before and after the truncation process for equation (2). The marked areas show differences in the process. In Fig. 5 shows that there is not a big difference in the peak value but only a slight difference in the side lobe when the results before and after the truncation operation are compared. Based on the results of the process using the truncation, it can be applied to the LPF by applying it to the intermediate calculation process of the convolution.

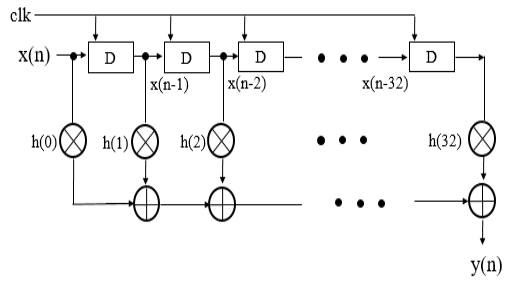

Fig. 6. LPF.

Fig. 6 shows the proposed LPF. The 8-bit data output from the 16-ary mapper is sequentially inputted to the D flip-flop by a clock and is then configured to transmit data to the next D flip-flop.

The input data is multiplied by a filter coefficient and a multiplier, and then truncation is performed to produce 8-bit data. The filter coefficients are composed of data converted to 8-bit fixed point data using the data calculated by MATLAB in equation (2). The computed data is additionally computed with the data truncated by the multiplier through the adder. Since carry can occur during this process, truncation process is performed on the output data of the adder to produce 8-bit data. If the process is repeated until the 33 taps are reached, y(n) is produced as 8-bit data.

B. Baseband demodulator

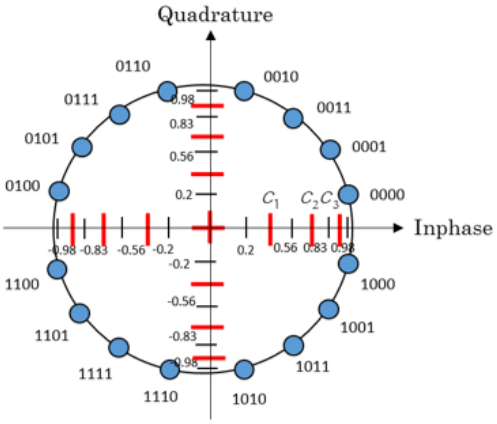

Fig. 7. 16-PSK constellation.

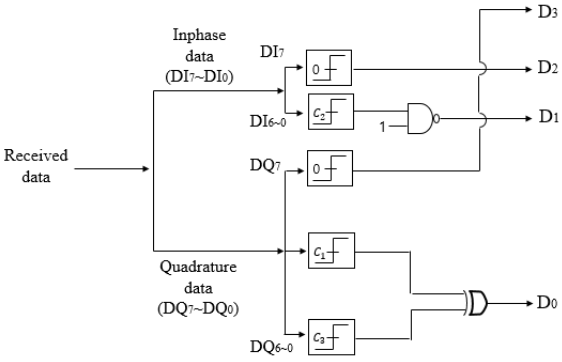

Fig. 8. Decision device.

TABLE I.
Threshold parameters of the decision device.

	Values	Fixed point
C_1	0.905	01001110
C_2	0.605	01001011
C_3	0.38	00101100

Fig. 7 shows the constellation of the proposed 16-PSK. The received data is mapped to recovered symbols by determining the phase of data in the baseband demodulator

according to the constellation expressed by the Gray code. The received data, according to the constellation shown as Gray code, is mapped as recovered symbols after determining the data's status in the baseband demodulator.

Fig. 8 shows a decision device that converts 8-bit in-phase data and quadrature data received from the baseband modulator into 4-bit data. When the received data is input, a threshold value composed of fixed points is determined as shown in Table I, and data is output. D_3 is the sign bit of the received quadrature magnitude. D_2 is the sign of the received in-phase data and compares the received data value excluding the sign bit with the threshold value C_2 among the received 8-bit in-phase magnitude. When the remaining data value is larger than C_2, 1 is output. When the remaining data value is smaller than 0, 0 data is output D_1 through the operations with the NAND gate. The received quadrature data, excluding the sign bit, are determined through threshold values C_1 and C_3. The determined data is output via D_0 through operation with XOR gate.

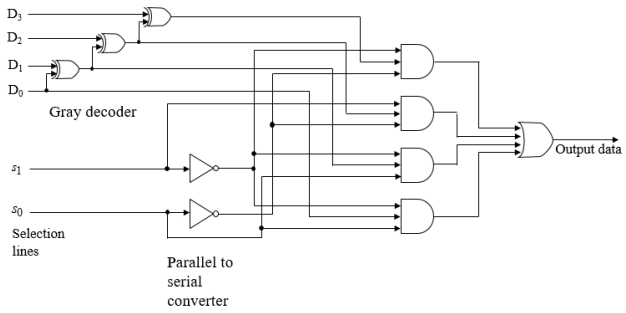

Fig. 9. Gray decoder and parallel to serial converter.

Fig. 9 is a block diagram of the structure that receives the data output from the structure in Fig. 8 as input data, converts it into binary data and outputs it as serial data. Since 4-bit data recovered from the structure is composed of Gray codes, it is necessary to convert the data into original binary data. The structure shown in Fig. 9 is converted into binary data, receiving converted 4-bit binary data as input, and allowing serial data to be sequentially output by s_1 and s_0.

C. Implementation and verification process

The baseband modulator and the baseband demodulator of the proposed 16-PSK modem are implemented by Verilog-HDL coding. Then, the code described is verified by RTL simulation using ModelSim of Mentor Graphics. We also modeled the proposed 16-PSK modem using MATLAB and compared it with the results of 16-PSK in Fig. 2.

The verified simulation is synthesized using Synopsys' Design Compiler. After pre-simulation of the generated netlist and backend process using Synopsys' Astro, we have verified the 16-PSK modem implemented through STA and post-simulation.

FPGA verification is carried out using SoC board with ALTERA's Excalibur device and modulation and demodulation process using TFT-LCD and LED built in board.

III. RESULTS AND DISCUSSION

A. Simulation verification result

The simulation verification process is verified by using MATLAB, modeled after the result, and the output value of module unit of RTL simulation of 16-PSK modem described by Verilog-HDL using ModelSim is checked.

In the simulation result of the baseband modulator, when serial data is inputted, it is confirmed that 4-bit parallel data is outputted according to the selection line. And check that it is output as the Gray code. The output Gray code confirms the 8-bit data output value which determines the position between phases through 16-ary mapper. The output 8-bit data becomes the input of the LPF and confirms the operation result value 33 taps.

In the baseband demodulator simulation results, the 8-bit data received from the baseband modulator is received and restored to the original data signal. In-phase data and quadrature data are received, and the 4-bit data determined according to the threshold value, is checked and output data converted into binary data is confirmed. Then the value converted to serial data was checked. Through this process, the input waveform of the baseband modulator was compared with the output waveform of the baseband demodulator.

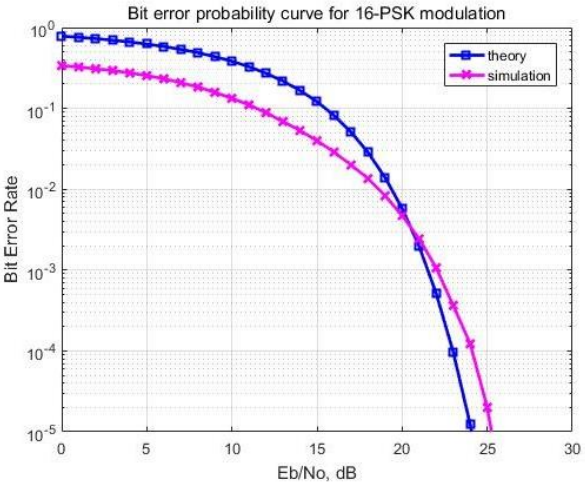

Fig. 10. BER curve.

Fig. 10 shows the BER of the proposed 16-PSK modem modeled using MATLAB. Compared with the 16-PSK BER generated by equation (1) in the same WGAN conditions, the BER characteristic was improved when it was below 20dB as shown in Fig. 10.

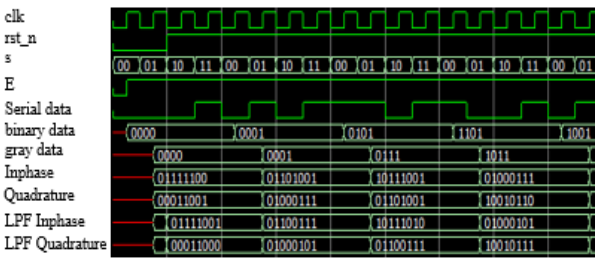

Fig. 11. Baseband modulator result.

Fig. 11 shows the simulation results of the baseband modulator. When the serial data is input, the binary data can be converted into parallel data, and the phase symbol shown in Fig. 7 can be confirmed by comparing the Gray data in Fig. 11. And the output value from 16-ary mapper can be confirmed using the results from in-phase and quadrature. The computation result using the proposed LPF structure can be confirmed in LPF in-phase and LPF quadrature.

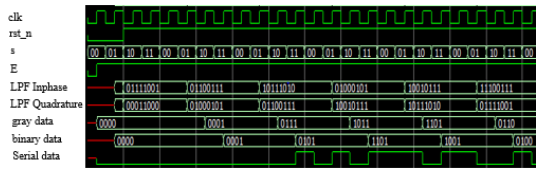

Fig. 12. Baseband demodulator result.

Fig. 12 shows the simulation results of the baseband demodulator. It can be confirmed that 4-bit Gray data is converted by receiving the data transmitted from the baseband modulator. Also, binary data and serial data can be found in Fig. 12.

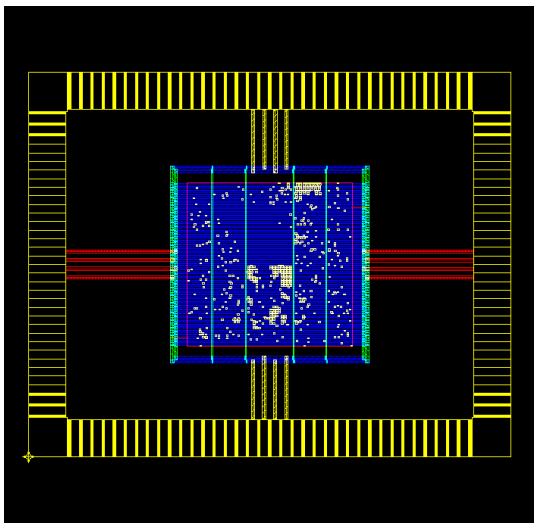

Fig. 13. Chip layout.

Fig. 13 shows the chip layout generated as a result of place and route process using Astro. As a result of Verilog-HDL coding and implementation using CMOS 350nm process, the operating frequency is 20MHz, the size is 2.74mm^2, and it is implemented with about 30K gate count.

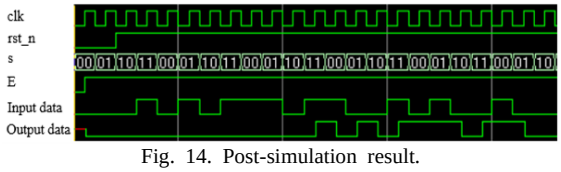

Fig. 14. Post-simulation result.

Fig. 14 shows the post-simulation results of the implemented 16-PSK modem. The input data waveform of the baseband modulator matches the output data waveform of the baseband demodulator.

B. FPGA verification result

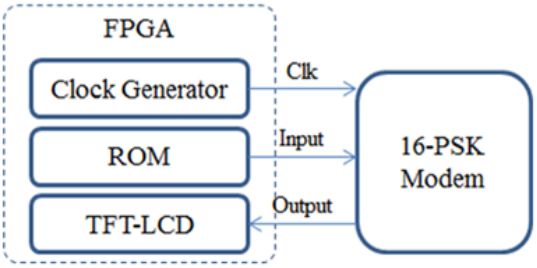

Fig. 15. Chip test diagram.

Fig. 15 shows the environment for FPGA verification. The environment is constructed based on the results that are sufficiently verified by simulation.

In the FPGA verification process, the input data is implemented as a look-up table through ROM in consideration of the number of cases. Then, the clock division is used to divide the frequency generated by the device into the frequencies at which the TFT-LCD can operate.

According to the clock operation, the data output from the ROM is input to the implemented 16-PSK modem, and the output data of the baseband modulator of the modem is input to the TFT-LCD and the baseband demodulator. The data output value of the baseband demodulator is output to the LED.

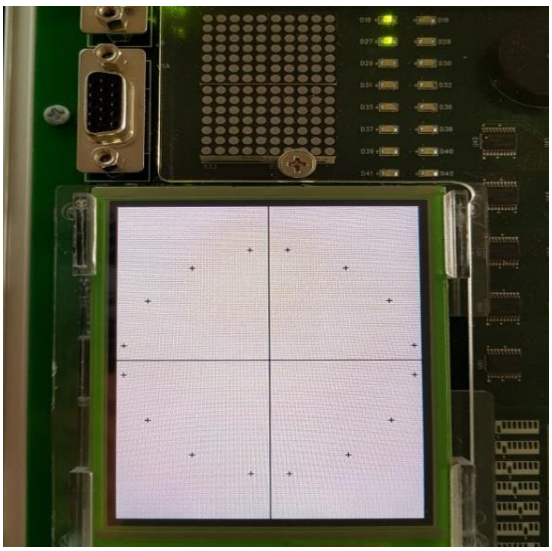

Fig. 16. Chip test result.

Fig. 16 shows FPGA verification and chip test results. The first LED lighting in Fig. 16 shows that data 1 is input to the baseband modulator. The second LED lighting shows that data 1 is output through the demodulation process in the baseband demodulator. The third LED is turned off when the input data matches the output data and lights up when the output data does not match.

The result modulated through the input data is formed near 16 symbols of the TFT-LCD. In order to confirm the additional performance of the 16-PSK modem, noise was added in the modulation process using PN codes.

The dip switch of the equipment was used to determine the intensity of the noise, and the noise was constituted in

level units to add noise of five levels. In each step, the noise data added to the bits are added to the vector unit. In the implemented 16-PSK modem, when the noise of level 4 of higher is added, the input data and output data are inconsistent and the third LED is turned on.

IV. CONCLUSIONS

In this paper, we made a design of the 16-PSK baseband modem with bandwidth efficient communication under the limited bandwidth condition. Before implementing 16-PSK baseband modem with FPGA, the design parameters with low HW complexity and the required performance are selected through MATLAB simulation. The BER simulation results of modem with the selected design parameters satisfied the required performance and lower areas with reducing HW complexity. The designed 16-PSK modem employs the error reduction method using the Gray code and LPF using truncation. The overall modem design was implemented using more simple structure. By using the simpler structure of the 16-PSK baseband modem, it is expected to make an efficient design of more complex M-ary PSK modem requiring limited bandwidth and high-speed data transmission.

ACKNOWLEDGMENT

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