1-13GHz Wideband LNA utilizing a Transformer as a Compact Inter-stage Network in 65nm CMOS

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Abstract - **A low power wide-band low noise amplifier (LNA) is presented in 65 nm CMOS. A compact inter-stage network utilizing one transformer and a resistor is proposed to obtain ultra-wide bandwidth. The designed LNA achieves 1 - 13 GHz bandwidth with > 10 dB of power gain. The simulated noise figure ranges from 9.6 to 10.5 dB over 1-13 GHz with power consumption of 11mW at 1.2 V of power supply.**

I. INTRODUCTION

Recently, growing research on reconfigurable multi-band-standard and ultra-wideband (UWB) systems has increased interest in broadband low-noise amplifier (LNA) design. A broadband LNA must have good input matching and low noise figure over a multi-GHz bandwidth (BW), while consuming low power. The primary objective in the design of the LNA is to suppress the additive noise at the subsequent stages and to achieve sufficiently large gain. In most systems, this objective should be achieved while constraining the LNA input to 50 Ω for impedance matching with external components such as an antenna or filter.

In order to achieve wideband impedance matching, a multiple-section bandpass filter with inductively generated common-emitter (CE) SiGe or common-source (CS) CMOS LNA have been proposed in [1] and [2], respectively. If the noise requirement is not that critical, a resistive shunt-shunt feedback or simply a resistive termination in parallel at the input of the amplifier can be considered with an improved linearity. The bandpass-filter-based UWB CG-LNA proposed in [3] reduces power consumption and improves the linearity compared to the UWB CS-LNA. However, the large number of inductors consumes large amount of area and also increases the noise figure. Using a common gate (CG) transistor for input matching is reported in [4]-[6], but the additional CS stage degrades the linearity and consumes more power. A differential UWB CG-LNA employs capacitive cross-coupling to reduce the noise figure [7], but this cross-coupling also increases the quality factor of the parallel RLC input network, which causes the decrease of the bandwidth. In addition, the presence of the resister has an adverse effect on the amplifier`s noise figure in either way and suffers from potential instability though it has slightly better noise performance.

A big design challenge for UWB LNAs is wide bandwidth and the stringent linearity requirement over a wide frequency range due to the large numbers of in-band interferences in UWB system, and the cross-modulation/inter-modulation caused by blockers or transmitter leakage in a reconfigurable receiver. Furthermore, while f_T increases with technology scaling, linearity worsens due to lower supply voltage and high-field mobility effects. Therefore, wideband linearization in deep-sub-micron CMOS process is a new trend. However, most of the linearization methods reported so far are aimed at the narrow band applications.

In this paper, we present a 1 – 13 GHz wideband LNA consisting of five stages. We propose a compact transformer-based inter-stage network which has comparable bandwidth enhancement ratio (BWER) compared with the π-type inductor peaking (PIP) network with much smaller area consumption. The five stages are cascaded, each of which utilizes drain and gate parasitic capacitances and a transformer with series resistor. A CG configuration with a biasing inductor at the source is used as the first stage to provide a wideband 50 Ω matching at the input while achieving a good linearity and a moderate noise figure. The LNA has three cascode amplifiers followed by the common drain (CD) buffer at the output stage. The designed LNA achieves a wide enough bandwidth to cover the whole 1 – 13 GHz frequency range, a 14.3 dB of maximum gain, and 9 dB of minimum NF having less than 11 mW of power consumption.

The paper is organized as follows. Section II presents the topology for 5-stage LNA. Simulation and measured results are presented in Section III. Conclusions are drawn in Section IV.

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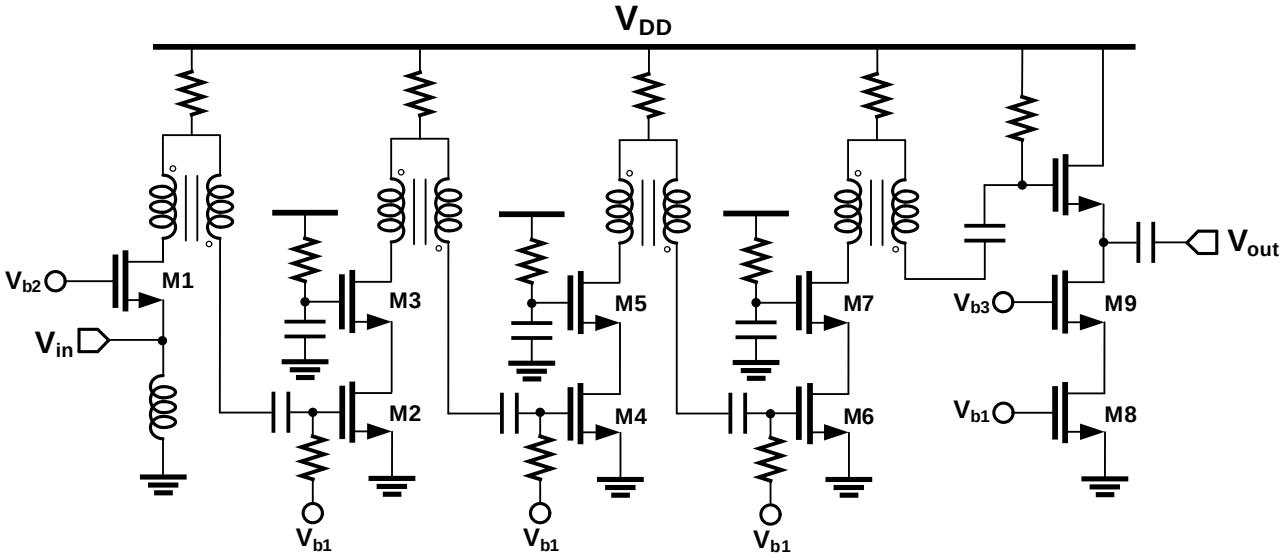

Fig. 1. Schematic diagram of the designed wideband LNA.

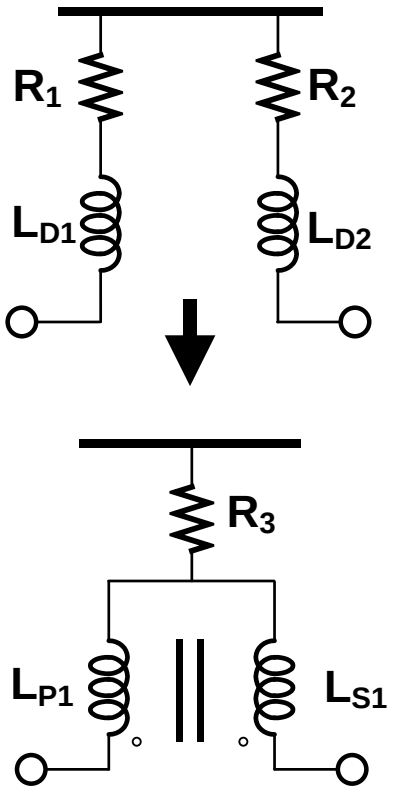

Fig.2 Transformation of PIP to single Transformer with a resistor.

II. PROPOSED 5-STAGE LNA

A. Design consideration of the proposed CG-LNA

The general block diagram of front stage for the LNA is shown in Figure 1, where a compact inter stage network utilizing only one transformer and a resistor is formed. A CG amplifier with a source inductor is used as the first stage. Since a source inductor is used to provide the bias current, the noise contribution is much lower than using a resistor. The inductor at the source of M1 is designed to resonate out the node capacitance at the center frequency. With a desired 1 - 13 GHz bandwidth, the LC resonant frequency should be higher than this frequency to ensure stable circuit operation. However, a large inductor can lead to over-peaking of gain, and hence, circuit instability. As suggested by simulation, the circuit becomes unstable when the inductor exceeds ~ 1 nH.

B. Transformer based Inter-stage Network

A π-type inductor peaking (PIP) method has been proposed which can achieve a bandwidth enhancement ratio (BWER) more than 3. While PIP can greatly enhance the bandwidth of the cascaded amplifier, it requires three different inductors and two resistors for each inter-stage of the cascaded amplifiers which makes the multistage amplifier quite bulky. This bulky PIP can be approximately transformed into a compact single transformer with a small resistor with conversion equations as below. Figure 2 shows the conversion of PIP into a compact transformer based inter-stage network.

$$k = \frac{L_{D1}}{L_{S0} + L_{D1}} \tag{1}$$

$$L_{P1} = \frac{L_{S0} L_{D2}}{(1-k)(L_{S0} + L_{D1} + L_{D2})} \tag{2}$$

$$L_{S1} = \frac{L_{S0} L_{D1}}{(1-k)(L_{S0} + L_{D1} + L_{D2})} \tag{3}$$

$$R_3 = R_1 \parallel R_2 \tag{4}$$

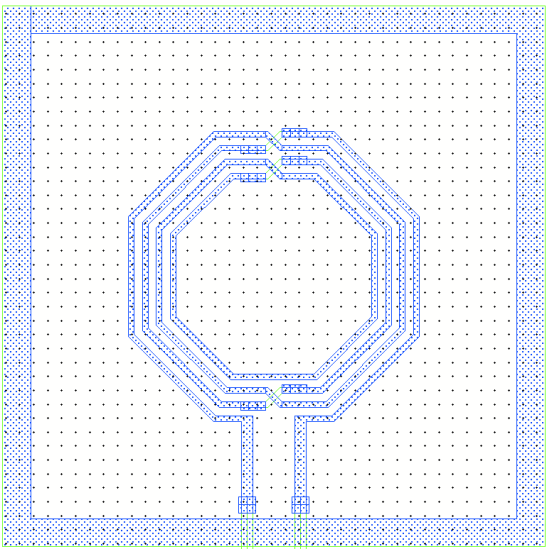

Fig. 3. Layout of the PIP transformer with top metal layer (*i.e.*, OA layer in Samsung 65 nm technology). The area of the transformer is 175 x 175 μm^2.

By utilizing the proposed transformer as a compact inter-stage network, BWER is comparable to PIP method with much smaller occupation area. The top metal (whose thickness is 3 μm) is used for the transformer, which only occupies an area of 175 x 175 μm2, as shown in Figure 3.

C. Noise analysis of the proposed CG-LNA

The trans-conductance of the CG-LNA is given by

$$G_m = \frac{i_{ds}}{V_{in}} = \frac{|Z_{in}(s)|}{Z_{in}(s)+R_s} g_m \tag{5}$$

where $Z_{in}(s)$ is defined by

$$\frac{s/C_{gs}}{s^2+s\frac{g_m}{C_{gs}}+\frac{1}{L_S C_{gs}}} \tag{6}$$

The LNA noise factor is defined by (neglecting r_o)

$$F = 1 + \frac{\gamma}{\alpha g_m R_s} + \frac{\delta\alpha}{5 g_m R_s}\left(\frac{\omega}{\omega_T}\right)^2 + \frac{R_D}{X(s)} \tag{7}$$

where X(s) is defined by

$$(\omega^2 {L_D}^2 + {R_D}^2) R_s {g_m}^2 \left(\frac{Z_{in}(s)}{Z_{in}(s)+R_s}\right)^2 \tag{8}$$

where γ, α, and δ are process-dependent parameters. Because L_s partially cancels the parasitic capacitance at the source node of the transistor in front stage, its noise contribution remains much less than that of the transistor even at relatively high frequencies. The noise is dominated by the thermal noise (second term), which is mainly frequency-independent. The frequency-dependent gate induced noise (third term), and the frequency shaping of the resistor noise (fourth term) results in a small variation of the CG-LNA noise factor over the BW.

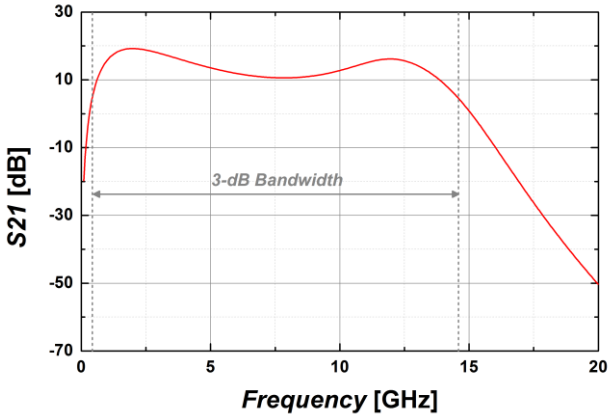

Fig. 4. Post-layout simulation result of S21 for the 5-stage LNA.

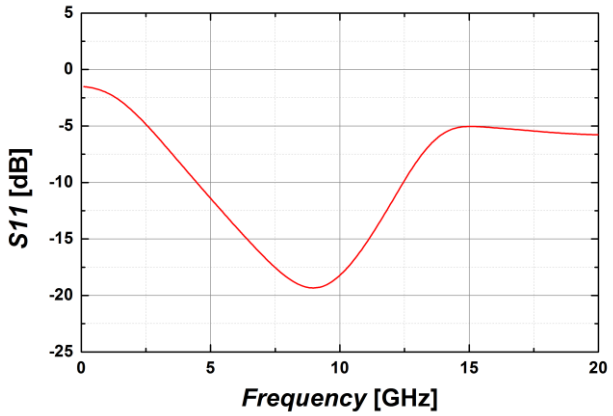

Fig. 5. Post-layout simulation result of S11 for the 5-stage LNA.

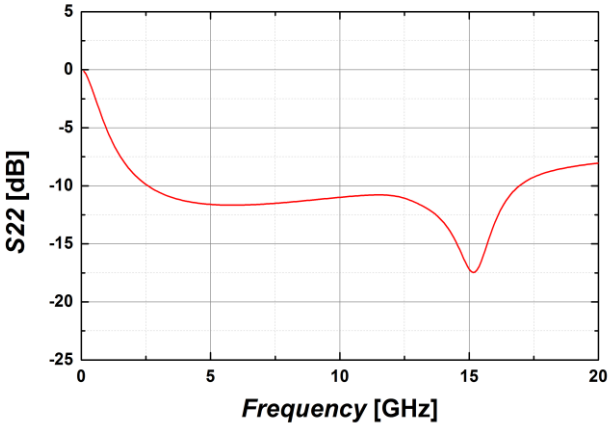

Fig. 6. Post-layout simulation result of S22 for the 5-stage LNA.

III. SIMULATION AND MEASUREMENT RESULTS

Figure 4 presents the simulated S21. The maximum voltage gain is 16.2 dB and the minimum gain is 10.5 dB between 3.8

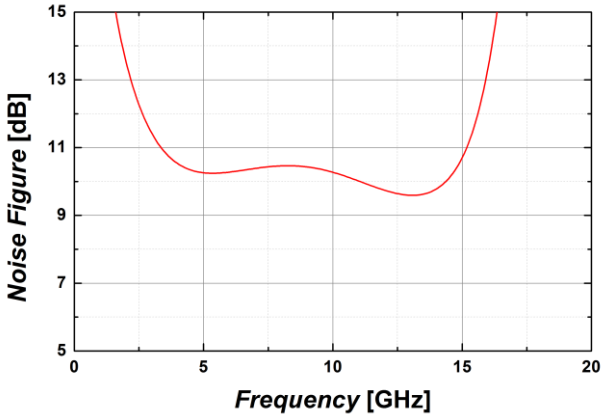

Fig. 7. Post-layout simulation result of noise figure for the 5-stage LNA.

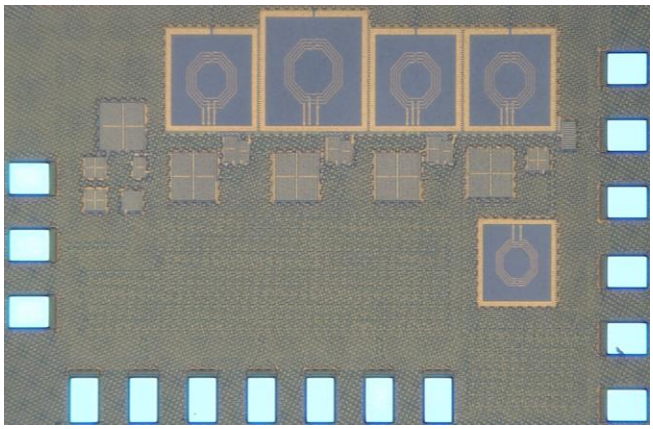

Fig. 8. Chip micrograph (Size : 0.73 x 1.68 mm^2)

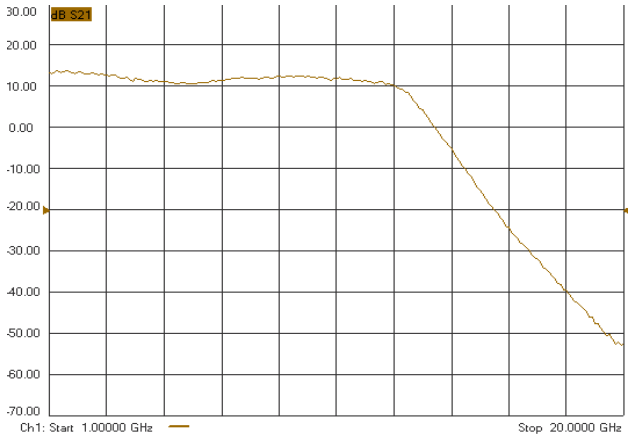

Fig. 9. Measured result of S21 with correct bias current for the 5-stage LNA.

and 12.5 GHz for the LNA. The 3 dB bandwidth of the gain is wider than 14 GHz. The peak is as a function of g_m where the peak can be flattened by choosing correct bias current. Figure 5 and 6 shows the simulated input and output reflection coefficients. S11 is lower than -10 dB between 3.8 and 12.5 GHz for the LNA. The output buffer achieves excellent matching up to 17 GHz. The noise figure (NF) of the LNA is shown in Figure 7. The minimum noise figure is

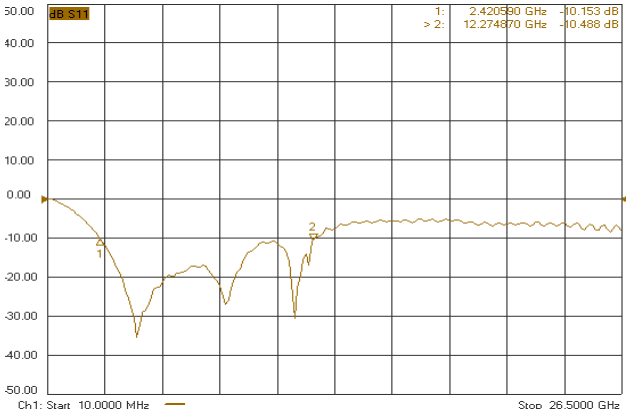

Fig. 10. Measured result of S11 for the 5-stage LNA.

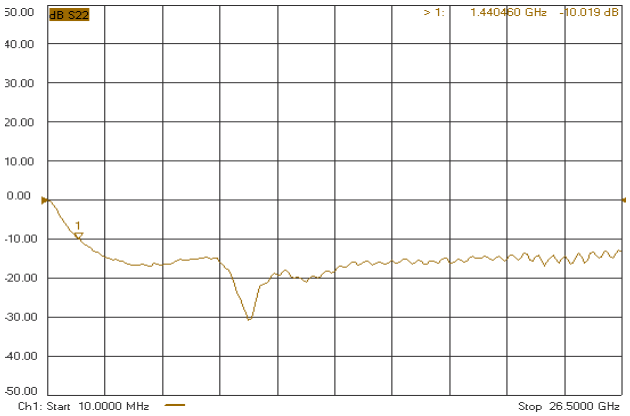

Fig. 11. Measured result of S22 for the 5-stage LNA.

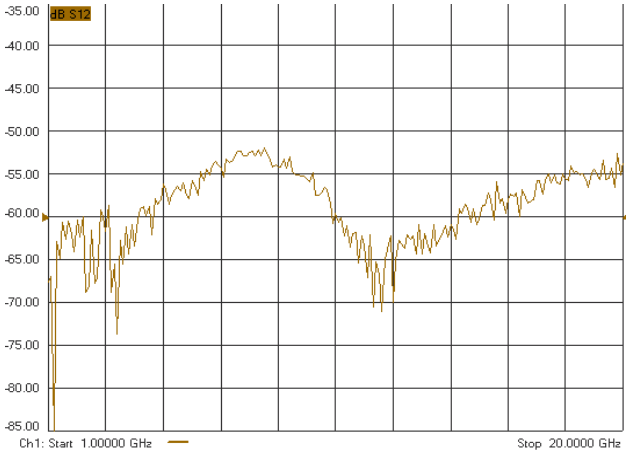

Fig. 12. Measured result of S12 for the 5-stage LNA.

9.4 dB at 12.8 GHz in simulation.

The LNA was fabricated in Samsung 65 nm RFCMOS technology. Figure 8 shows the chip micrograph. The overall chip area is 0.73 x 1.68 mm^2. The LNA consumes 11 mW from a 1.2 V supply. The measured S-parameters are shown in Figure 9 to 12. Within 1 – 13 GHz, the measured small-signal gain (S21) with correct bias current achieves a maximum value of 14.3 dB at 8.2 GHz, and has a minimum value of 10.2 dB at 4.32 GHz. The measured 3-dB bandwidth of the gain is wider than 13GHz. In this frequency range, the

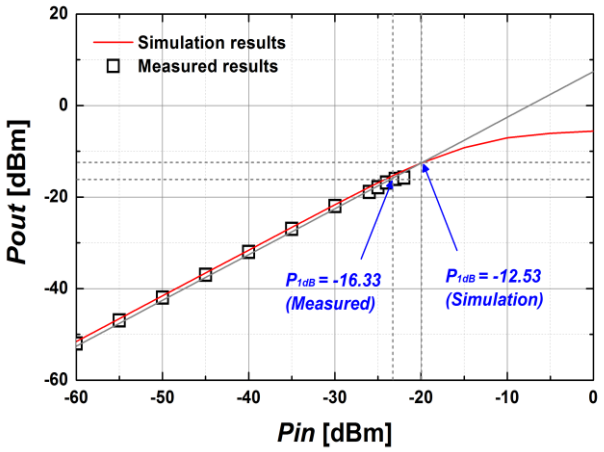

Fig. 13. Simulation *vs.* Measured result of P_{1dB} for the 5-stage LNA.

measured output return loss (S22) is less than -10 dB, the measure input return loss (S11) is less than -10 dB, and the measured isolation (S12) is less than –52.4 dB. The simulation in general agrees well with the measured results. The relatively large discrepancy in S22 can be attributed to the source follower used for output matching. The stability factor K calculated from the measured S-parameters is greater than 1 suggesting unconditional stability of the circuit. At 8.2 GHz with maximum gain, the proposed LNA has P_{1dB} of -16.33 dBm. The measured P_{1dB} is well matched with simulation result.

IV. CONCLUSIONS

In this study, a low power wide-band 5-stage low noise amplifier (LNA) was realized in Samsung 65 nm CMOS. The designed wideband LNA demonstrated 1-13 GHz of bandwidth with > 10 dB of the gain flatness by using the proposed compact inter-stage network.

ACKNOWLEDGMENT

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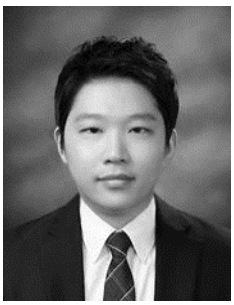

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