A 10.3125 Gb/s Deserializer for IEEE 10G-EPON Standard

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***Abstract* - The throughput requirement of high-speed interface such as wireline I/O and memory I/O has been increased even if the power budget for the interface circuits has been maintained and decreased. This paper, true single-phase clock logic and half-rate architecture to implement the 16-to-1 10.3125 GB/s deserializer is used to minimize the power consumption with remaining high-speed operation. The design method for essential block such as demultiplexer, clock data recovery circuit, continuous time linear equalizer, decision feedback equalizer and lock detector is also described in paper. The designed deserializer is fabricated through 65nm CMOS process and dissipate about 200mW is satisfied with IEEE standard. The developed deserializer has BER 10^{-12} with PRBS 2^9-1.**

***Keywords*—Deserializer, Ethernet, High speed interface**

I. INTRODUCTION

As data traffic for services such as 5G, high-resolution video streaming, and IoT is rapidly developing, the demand for high-speed interface is rising sharply. A high-speed interface circuit must overcome several challenges including high speed operation, equalization techniques, and low power consumption. The developed 1:16 10.3125Gb/s deserializer which converts high-speed serial data to parallel data is for 10G-EPON IEEE standard. As shown in Fig. 1, the deserializer consists of equalizer to compensate for distorted data, 1:16 demultiplexer, clock and data recovery circuit (CDR). In the 10.3125Gb/s deserializer, the key blocks are CDR and equalizer. The CDR aligns the clock to the center of the data and recovers the clock by using the input data. The developed CDR is continuous type of CDR because the data packet in Ethernet system is continuously transmitted. In order to minimize the malfunction of CDR, in this paper, the new architecture of Bang-Bang phase detector (BBPD) is proposed. Also, the lock detector based on a counter for the exact loop selection between frequency detection loop and phase detection loop in CDR is implemented. The developed lock detector is able to change the resolution, which results in making the flexibility of the frequency of data. Because the CDR recovers the clock by the information of the data, the slope information of data is critical. However, due to channel loss, the data is distorted, which causes to disappear the slope information of data. In order to prevent this problem, the equalizer is necessary. In developed deserializer, two types of the equalizer are implemented. One is continuous-time linear equalizer (CTLE) that compensates for the lag between pre-cursor and post-cursor of the distorted data. Because the operation of CTLE is like the amplifier operating at the specific frequency, the CTLE could amplify the noise at the specific frequency. This characteristic of CTLE may distort the data. Because of this reason, the decision-feedback equalizer (DFE) that compensates only for post-cursor of the distorted data is also developed. Because the DFE is optimized for post-cursor of the distorted data, it is usually employed for the channel that is severe in terms of reflection. Therefore, the CTLE and DFE are developed for 10G-EPON deserializer.

In order to design low power deserializer with high-speed operation, half-rate architecture and true single-phase clock (TSPC) logic are employed. Thanks to the above mentioned techniques, a 10.3125 Gb/s 16-to-1 deserializer for IEEE 10G-EPON has been successfully designed in this paper. Each parts are described in following sections and the performance results and specifications are summarized. The conclusion is drawn in section IV.

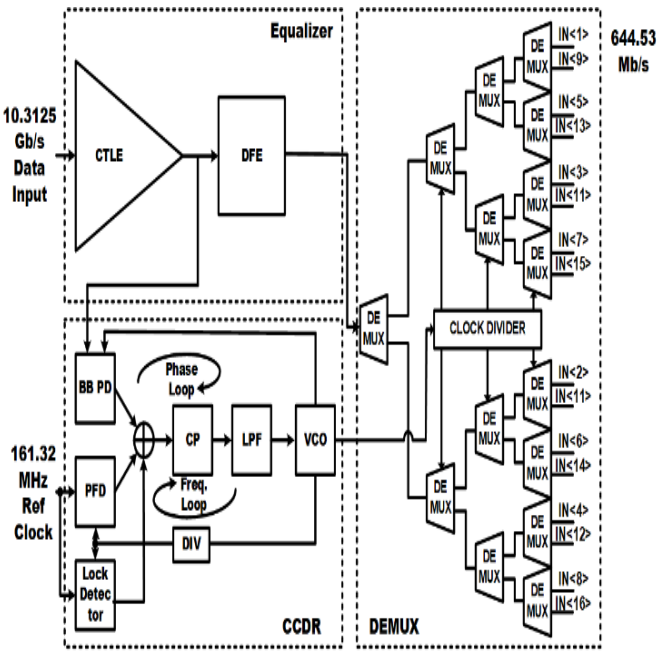

Fig. 1. Block diagram of the developed deserializer

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II. IMPLEMENTATION

A. 1 to 16 Demultiplexer (DEMUX)

The demultiplexer circuit converts the serial data to parallel data. The block diagram of the 2-to1 demultiplexer is presented in Fig. 2. The input data is aligned by rising and falling edge of clock at first. In order to align the order of the data, the additional latch is employed at the line of D1. Through this operation, the data packet is consequently separated. In demultiplexer, because the data is separated by the clock having the same data rate, the rising and falling time of clock has to be identical. Conversely, if the duty of the clock is different, commonly additional jitters are caused. The clock of latch should stay above 0.8UI in order for the latch to have the gain to increase or remain the amplitude of output swing. If not, the time to simultaneously turn input switched on the increase, which leads to reduce the time spent to increase the output amplitude. In other words, the turn-off time of input switches is decreased. Because of these reasons, the clock distribution and slope in demultiplexer are essential factors. The block diagram and layout of the developed demultiplexer are shown in Fig. 3. The input data rate is 10.3125Gb/s serial data and the output data rate is 644.53Mb/s parallel data. The structure of the developed demultiplexer is third-type in order to have an identical clock delay [1]. By locating clock driver at the center of the 1:16 demultiplexer, the clock can have the almost same clock delay.

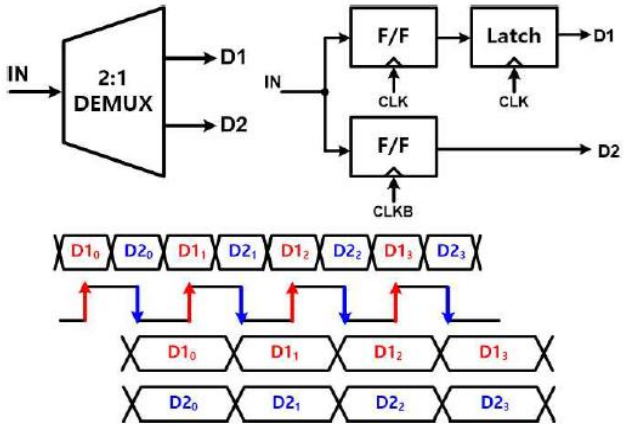

Fig. 2. Block diagram and timing diagram of demultiplexer

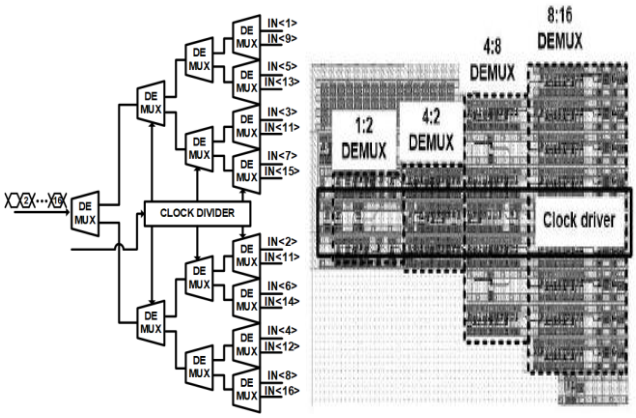

Fig. 3. Block diagram and layout of the developed demultiplexer

B. Clock and Data Recovery Circuit

The deserializer is only able to obtain the data from the serializer due to the problem caused by the skew between data and clock. Because of this reason, a circuit is needed to recover the clock by utilizing the received data. It is referred as to Clock and Data Recovery Circuit (CDR). The CDR's major function is to align the rising edge of the clock to the center of the data. The operation flow of CDR is as follows: Firstly, the frequency of the required clock is set in frequency locked loop by the reference clock. Then, the frequency of the clock is evaluated by the lock detector. If the result is correct, the phase loop operates in order to align the rising edge of the clock to the center of the data with the frequency locked loop off.

As aforementioned, the CDR can detect a transition of data and the difference between the received data and recovered clock by using frequency loop in CDR. Through this operation, the timing circuit in demultiplexer is able to have the set-up time which is about the half of the T_{data} period, making the timing circuit robust when it operates at high frequency domain. In order to find the ideal sample point, the phase detector is indispensable. For this reason, a binary phase detector (BBPD) is employed. The BBPD compares the phase of the input data with the phase of clock by using four flip-flops and two XOR gates. Fig. 5 shows the gain of BBPD is ideally infinite [2]. The BBPD can be

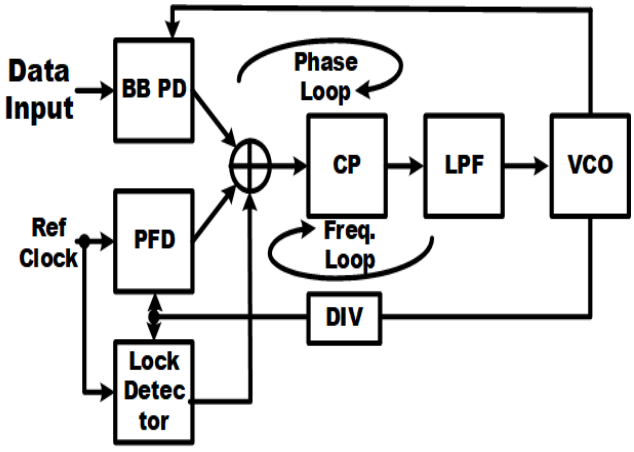

Fig. 4. Block diagram of clock and data recovery circuit

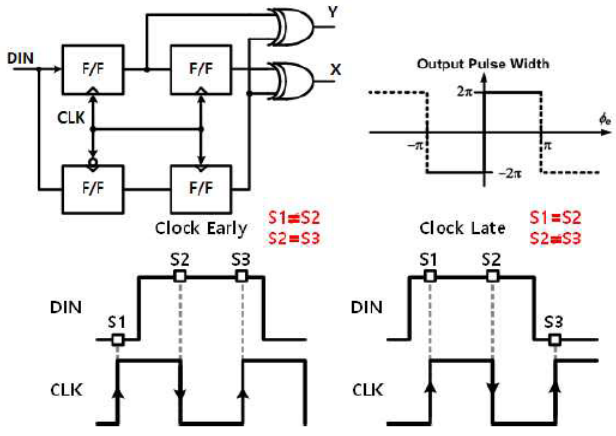

Fig. 5. Block diagram of bang-bang phase detector

implemented with two XOR gates and two timing circuits. If the clock arrives earlier than the data, the BBPD provides the information to delay the clock with the charge-pump. On the contrary, if the clock arrives later than the data, the BBPD provides the information which enables clock to reach faster. In order to distinguish whether the clock arrives early or late, the BBPD uses three sampled data by using the consecutive edge of the clock. As shown in Fig. 5, if the data sampled by the first clock edge is different from the others, the clock is located early. Conversely, if the consecutive sampled data of the first and second clock edge is the same and is different from the last one, the clock is late. However, the BBPD causes several problems in high-speed operation. The rising and falling edge of S1 and S3 are different from that of S2 due to the unequal output load of the timing circuits. Also, the clock skew delays the propagation of S1, S2, and S3, which provokes the malfunction of XOR gates. Therefore, the errors occur as shown in Fig. 6. The simulation verifies this phenomenon. If the load of S1 and S3 are smaller than 3.5 times compared with the load of S2, the average sum of up signal is equal to that of down signal, which causes the clock not to be in the center of the data. In this paper, in order to overcome this problem, the BBPD with re-aligned flip-flops is proposed. Fig. 7 shows the proposed BBPD that connects with four flip-flops at the output node of the

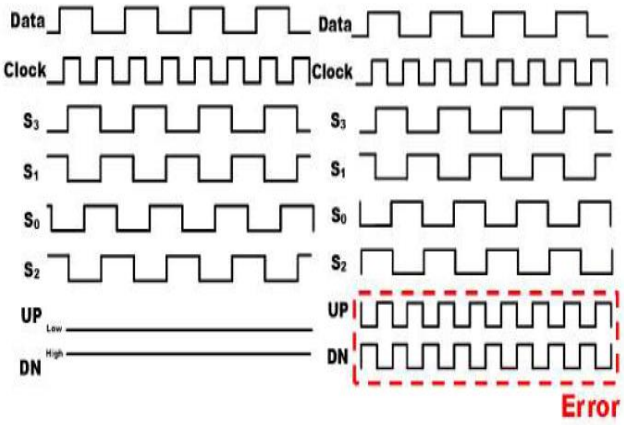

Fig. 6. Error of the conventional bang-bang phase detector

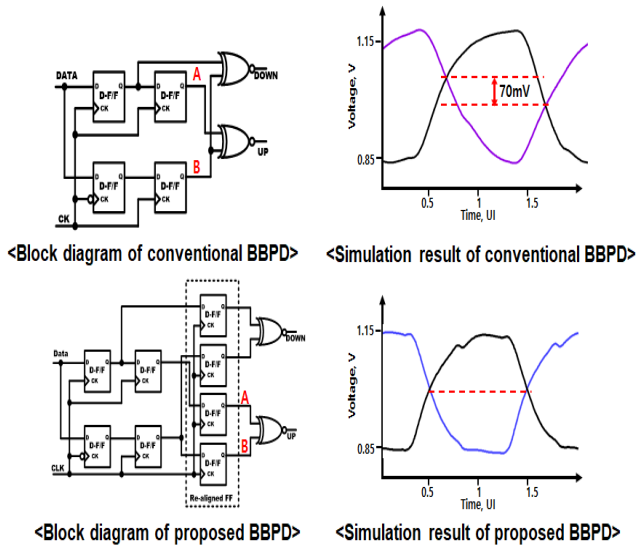

Fig. 7. Comparison between conventional and the proposed BBPD

convention BBPD. Since the loads of the final flip-flops are equal and the rising and falling time are identical, it leads to reduce the burden of the XOR gates. At the last timing circuit stage, the data is realigned with the same clock. As shown in Fig. 7, when the conventional BBPD is utilized for a 10.3125Gb/s system, the amplitude difference of midpoint of data is about 70mV. However, if the proposed BBPD is adopted for the same system, the difference of the midpoint of data is almost zero, which allows to effectively increase the bandwidth of XOR gates.

C. Lock Detector (LD)

The lock detector (LD) whose key role is to switch the frequency loop to the phase loop has an important role in CDR. If a LD malfunctions when it evaluates the frequency, the BBPD cannot align the clock to the center of the data. As shown in Fig. 8, a phase-based LD is able to compare reference clock with a divided clock of VCO in terms of phase. The output of LD is low as soon as the CDR is turned on. Afterwards, the phase-based LD continuously compares the delayed-divided clock. If the rising edge of the delayed-divided clock is located at the gap between reference and delayed reference clock, the frequency is locked. As a result, the output of LD is expected to be high. However, two types of problems may occur in terms of frequency and phase. In practice, the difference between the reference and delayed frequency occurs.

Because of this reason, the phase difference is accumulated by the difference of frequency, which causes that lock state becomes off even if the frequency loop is done. Another one is the difference in terms of phase. Even though the frequency of reference and the divided is the same, the phase offset may occur due to the mismatch of the charge pump and unexpected spur by the power supply. In

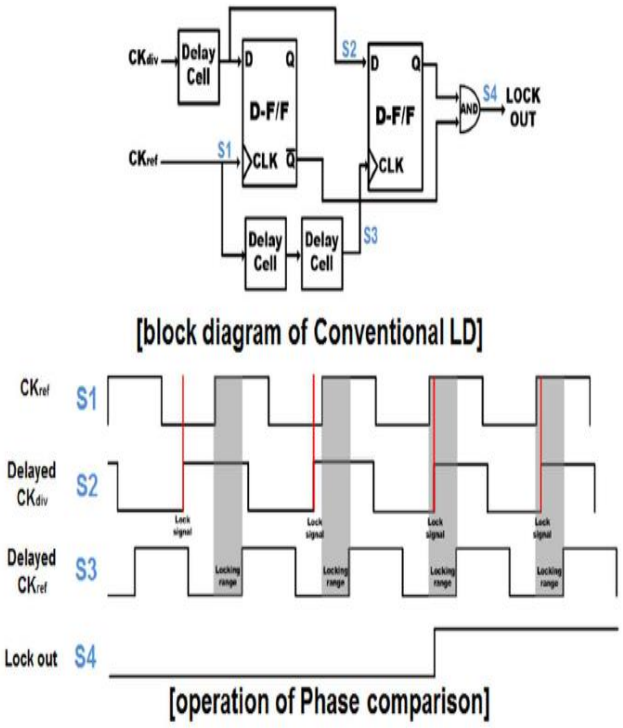

Fig. 8. Block diagram and operation of phase-based lock detector

the case of this phenomenon, the output of the lock detector is always low. Simply, in order to overcome these problems, it is easy for delay cells to be controlled. However, the optimized delay cannot be found due to the variations of PVT. Consequently, the method of phase-based LD is unstable due to using the phase difference. Because of these problems, in this paper, the LD based on the synchronous digital counter by the clock is used. Also, the method of the employed is based on the frequency difference. As shown in Fig. 9, the counter-based LD consists of N-bit counters, the timing circuits for aligning reference and divided clock, the resolution control circuit, and the lock decision circuit. The basic principle of the counter-based LD compares the number of the counter for reference clock with the number of the counter for divided clock. If the number is the same within the specified time, this state is called lock. Fig. 10 shows the timing diagram of the operation for the counter-based LD. As aforementioned, if the number of counters for the divided clock is 2^n-K and it is located within the range from 2^n-(K-1) to 2^n-(K+1) of locking for reference clock counter, this state is lock. And then the reset is operated in order to prevent to accumulate the phase error.

Fig. 11 shows the N-bit asynchronous counters in the LD. Because this is asynchronous counter, the layout of reference and divided clock line should be careful. By using the interested count number, the LD makes one pulse and lock window.

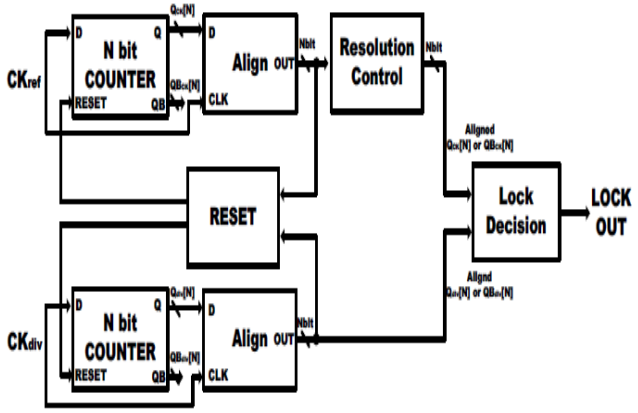

Fig. 9. Block diagram of the proposed lock detector

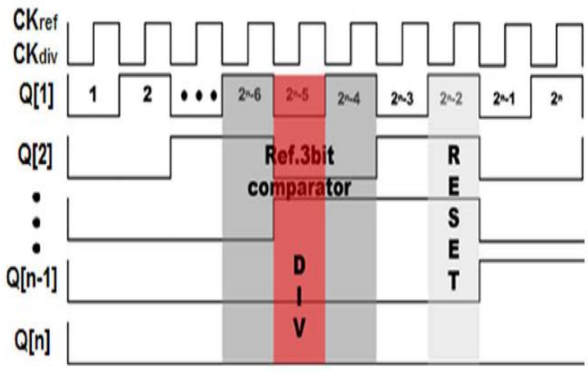

Fig. 10. Operation method of the counter-based lock detector

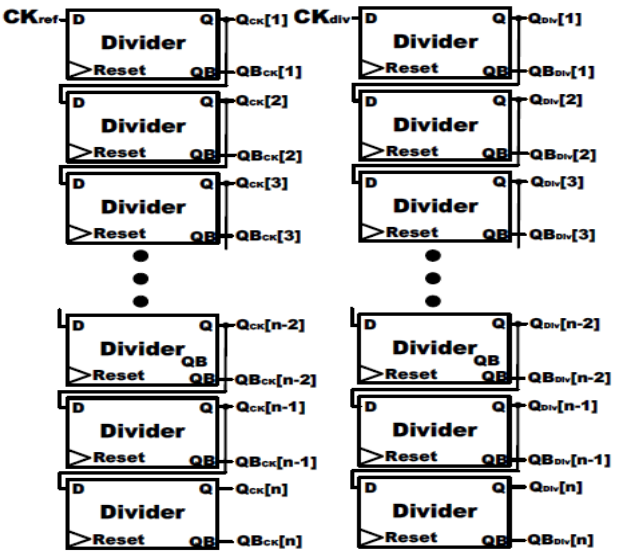

Fig. 11. N-bit counter having reset function in the counter-based LD

D. Continuous Time Linear Equalizer

The CTLE that acts as the high-pass filter and boosts the gain at the interested frequency can compensate for channel loss. The CTLE is able to eliminate pre-cursor and post-cursor ISI. Generally, CTLEs have both active and passive types. The passive CTLE made of resistor and capacitor is presented in Fig 12 [3][4]. On the contrary, the active CTLE includes an amplifier with high-pass characteristics, meaning that the gain is decreased in the active CTLE at low-frequency.

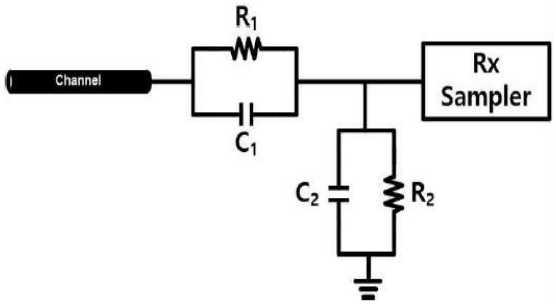

Fig. 12. Block diagram of passive continuous time linear equalizer

Because the passive equalizer has poles and zeros, the peaking gain is commonly generated after the zero in the passive equalizer. Since the passive equalizer consists of passive components, the gain at high-frequency is produced by degrading the gain at low-frequency. The value of gain and frequency for the peaking are determined by modifying the value of resistor and capacitor. The passive equalizer does not require additional power and has great linearity. On the other hands, larger space is needed compared to other equalizers, and the passive equalizer is not able to make the additional gain at Nyquist frequency. Because of this reason, in order to overcome the disadvantages of the passive equalizer, the active equalizer is presented. Fig. 13 shows a schematic of the active CTLE [5]. The active CTLE is composed of the input pair transistors, current sources,

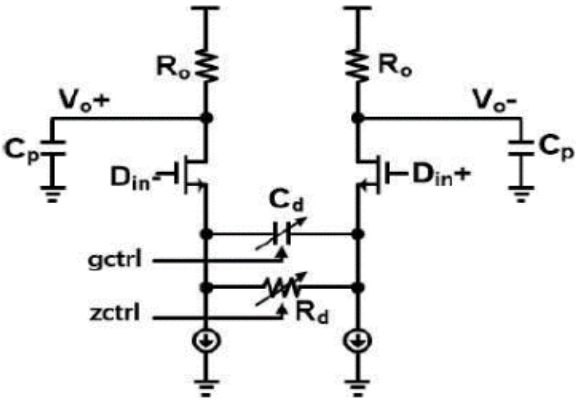

Fig. 13. Schematic and transfer function of active continuous time linear equalizer

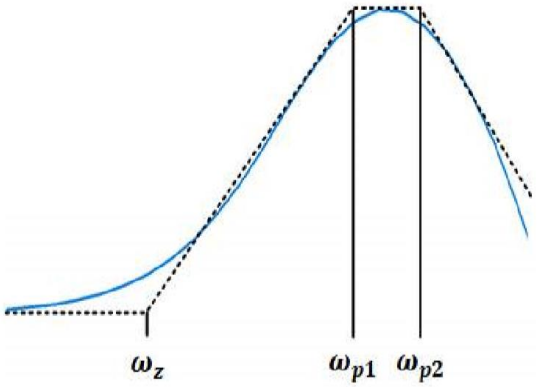

Fig. 14. Frequency response of active continuous time linear equalizer

output resistors, degeneration resistor to improve the bandwidth, and degeneration capacitor. The resistor and capacitor connected with the source of the input transistors determine the location of zeros and poles to make the peaking gain at the interested frequency. The transfer function of the active CTLE can be formulated as follows:

$$H(s) = \frac{g_m}{C_P} \frac{s+\frac{1}{R_d C_d}}{(s+\frac{1+\frac{g_m R_d}{2}}{R_d C_d})(s+\frac{1}{R_O C_P})} \quad (1)$$

$$\omega_z = \frac{1}{R_d C_d}, \omega_{p1} = \frac{1+\frac{g_m R_d}{2}}{R_d C_d}, \omega_{p2} = \frac{1}{R_O C_P} \quad (2)$$

The equation consists of one zero and two poles. The zero and pole at relatively low frequency are generated by degeneration resistor and capacitor. The last pole is dependent upon load capacitance. By using the Equation (1) and (2), the peaking gain at the interested frequency can be obtained.

$$Gain_{DC} = \frac{g_m R_O}{1+\frac{g_m R_d}{2}} \quad (3)$$

$$Gain_{Peaking} = g_m R_O \quad (4)$$

$$Peaking = \frac{Gain_{DC}}{Gain_{Peaking}} = \frac{\omega_{p1}}{\omega_z} = 1 + \frac{g_m R_d}{2} \quad (5)$$

As shown in Equation (3), (4), and (5), the frequency response of active CTLE for peaking gain is determined by zero and first pole. By the second pole, the interested frequency is finally decided. In order to design active CTLE, there are two factors to consider: First one is the amplitude of the received data should be within the input range of the active CTLE because the active CTLE is also an amplifier. Second one is that the current of the active CTLE is determined by the output load.

In the developed 10.3125Gb/s deserializer, the active CTLE is employed instead of the passive CTLE due to the area and the peaking gain. The block diagram of the developed active CTLE that consists of 3-stage active CTLE and bias circuits for 10.3125Gb/s deserializer is shown in Fig. 15. The received data is distorted by channel loss. The designed active CTLE recovers the data that can be recognized. Then, the output of the designed active CTLE would be connected with DEMUX, DFE, and CDR. The gctrl means the peaking gain control and zctrl means the location of zero control. In order to compensate for the channel loss by FR4 PCB line, coaxial cable, and the inductance of the package, in the filter cell, the resistor and the capacitor made by transistors are added. Therefore, the peaking gain and frequency is simply adjusted by the gate voltage of Rd and Cd. In order to prevent the variation of the common-mode voltage at the output, this feedback was necessary. Because this is replica circuit for the active CTLE, components should be matched with the transistors of the active CTLE. VTT was required for common-mode voltage. By using the feedback, the current of the filter cell was changed by the variation of Bias CS voltage in order to maintain the VTT voltage. In the developed active CTLE, the amplitude of the data is 400mV and VTT is 1V. The amount of current in the filter cell is about 350mA. Fig. 16 represents the simulation result indicating the peaking gain and frequency according to the variation of the gate voltage of gctrl and zctrl. As above mentioned, the simulation results verify that the peaking gain is changed according to the variation of the degeneration resistor and the peaking frequency is determined by the value of degeneration

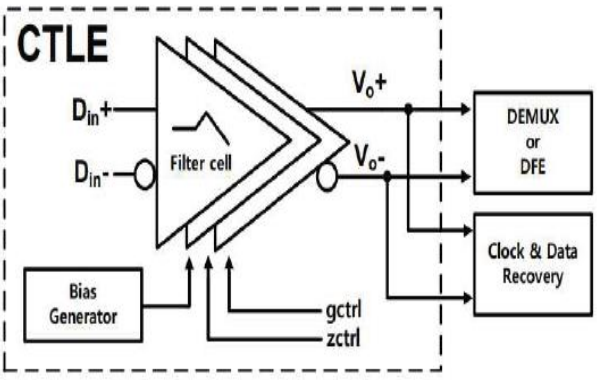

Fig. 15. Block diagram of active Continuous Time Linear Equalizer

capacitor. Fig. 17 shows the compensated frequency response at 10.3125Gb/s. The used insertion channel loss is -16dB at 10.3125Gb/s. At the frequency, the peaking gain of the active CTLE is 9.28 dB. As a result, the channel response becomes uniformed to the interested frequency. The eye-diagram having 260.1mV amplitude and about 0.86UI width is shown in Fig. 18.

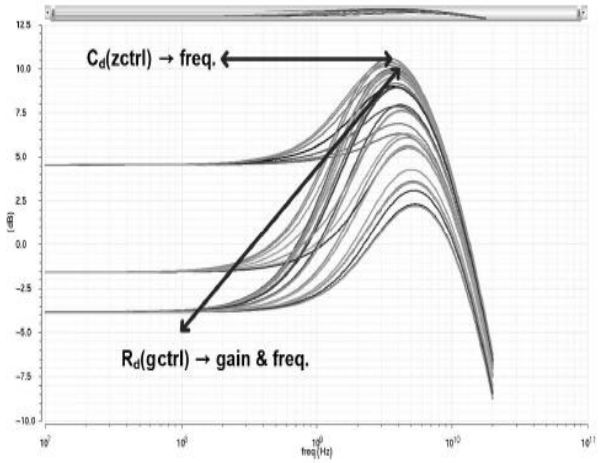

Fig. 16. Simulation results of peaking gain and frequency by control

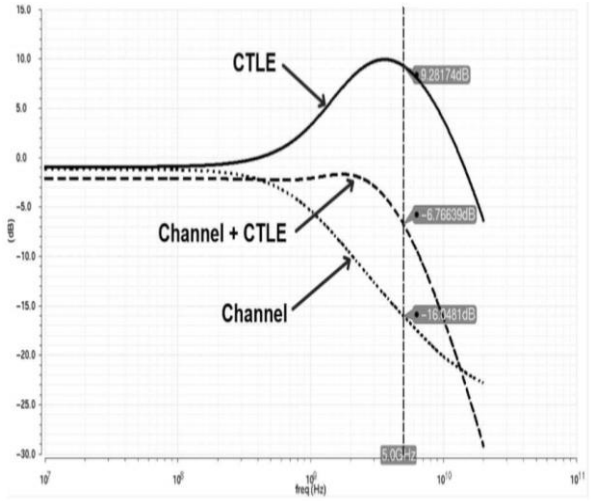

Fig. 17. Simulation results of the active CTLE with channel

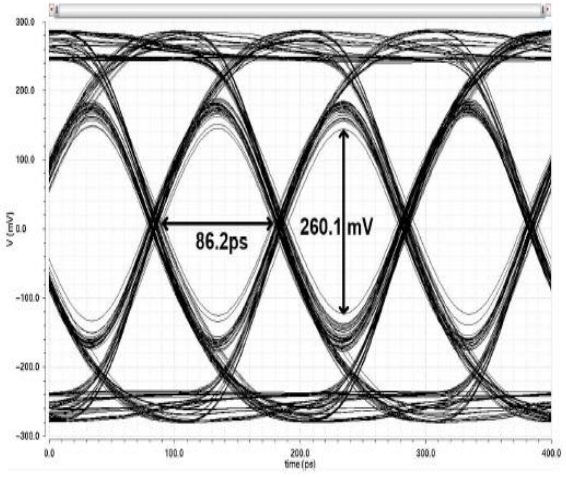

Fig. 18. Simulation results of the active CTLE with channel

E. Decision Feedback Equalizer

As aforementioned, the active CTLE can compensate for pre-cursor and post-cursor ISI with the characteristic of high-pass filter. Because of this reason, the noise could be generated, which results in making the ringing effect. The DFE can eliminate this type of ringing effect by removing the post-cursor ISI [6]-[10]. Therefore, DFE is located after CTLE. Fig. 19 shows the block diagram of the conventional DFE that is composed of decision slicer (flip-flop), 1-UI delay cells and the summer. The operation flow of the conventional DFE as follows: First of all, the initial data z_k is determined by the decision slicer. And then, d_k called the determined data is delayed with 1-UI. The more the number of the delay cell increases, the more the taps to weight W_k to the delayed cell also increases. The taps for weight have to be considered by the characteristics of the channel. Finally, the weighed data that is reflected by the channel response is summed or subtracted with the received data.

As shown in Fig. 20, the DFE is able to remove post-cursor ISI with the weighted delayed data. The advantage of the DFE is that the noise and crosstalk related to high frequency post-cursor ISI can be eliminated without amplifying the noise. On the other hands, the conventional DFE is not able to eliminate pre-cursor ISI, which could result in recovering the clock by using the received data due to the slow transition of the data. Also, because the conventional DFE has the feedback structure, there is a critical timing path.

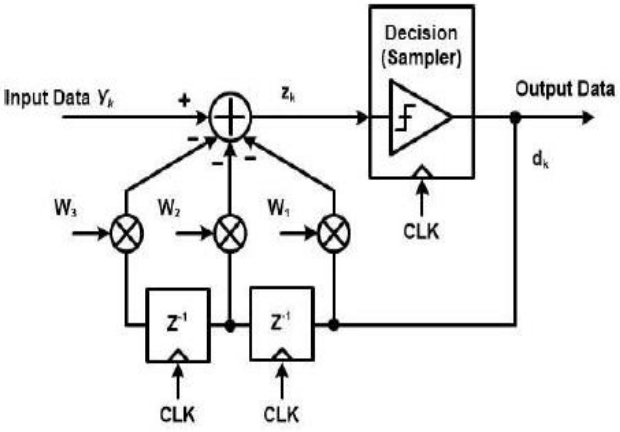

Fig. 19. Block diagram of the conventional decision feedback equalizer

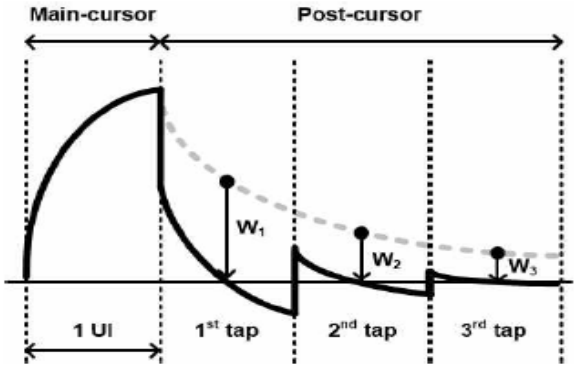

Fig. 20. The basic operation of the conventional decision feedback equalizer

F. Half-Rate Architecture and True Single-Phase Clock Logic

At the frequency beyond 10 Gb/s, the full-rate architecture dissipates significant power, because the power consumption of digital logic is proportional to the square of the frequency. On the other hand, a half-rate architecture can reduce a lot of power by using twice the slower clock. The current mode logic is generally used in high-speed circuit design due to its high operating frequency. But, unlike CMOS logic, static currents are constantly flowing, which consumes significant power. At 10 Gb/s, TSPC dissipates only 1/10 of power than CML in 65 nm process [11].

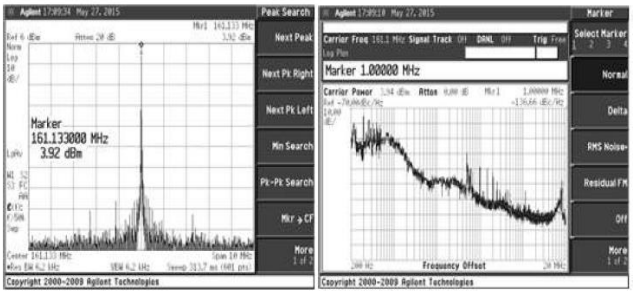

Fig. 21. Spectrum and phase noise of CDR

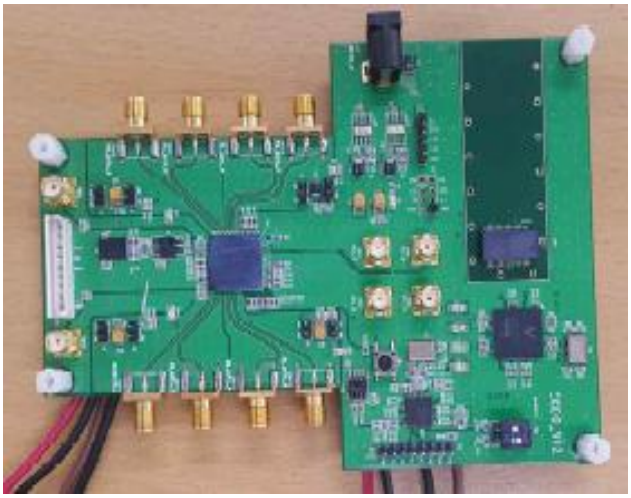

Fig. 22. Test board of the developed deserializer

III. MEASUREMENTS AND DISCUSSION

The developed 10.3125Gb/s deserializer for 10G-EPON is fabricated through 65nm CMOS process. The results of the designed deserializer are as follows: The deserializer occupies area of 1.96mm^2. The power consumption of the developed deserializer with CTLE is 380mW including I/O buffers. The input pattern provided by the PARBERT equipment and reference clock is applied to the developed deserializer. The extracted data patterns are compared with the input data patterns by using MATLAB codes. In order to evaluate the data patterns, the recovered clock that is able to be the standard to operate is first evaluated as shown in Fig. 21. As a result, the phase noise of the deserializer is -107dB/c at 1MHz offset. The developed deserializer is evaluated with 2^{31}-1 data pattern. The result of the evaluation is passed without the error. In the test boar as shown in Fig. 22, the developed deserializer is evaluated by using the optical module and IXIA. The output of the deserializer transmits to the external serializer. And then, the IXIA evaluates the transmitted data of the serializer. As a result, among the transmitted data 3,840,000 bytes, the 3,792,000 bytes is accepted. The accepted data rate is about 98.75%.

TABLE I
PERFORMANCE SUMMARY

Specification	16:1 Desrializer
Technology	65nm CMOS
Input data rate	10Gb/s
Reference clock	156.25MHz
Equalizer	CTLE / DFE
Supply voltage	1.2 V
Power consumption	200mW
Area	1.4mm X 1.4mm

IV. CONCLUSION

The deserializer for 10G-EPON standard is rendered through 65nm CMOS. The deserializer for 10G-EPON with CTLE and DFE is implemented. In order to evaluate deserializer, the PRBS 2^{31}-1 patterns were put in the designed deserializer by using the PARBERT. The deserializer is evaluated by MATLAB without error. Also, it is evaluated with optical modules and IXIA integrated the Ethernet data packet. As a result, it achieves the 98% of data reliability rate.

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