Self-Cascode Structures Using Optional devices in Standard CMOS Technology

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***Abstract* - This paper describes two possible configurations of an asymmetric-VTH self-cascode (SC) structure using optional devices in a 0.18-μm standard CMOS process. Standard CMOS technologies offer optional devices for a range of circuit design solutions, such as zero threshold voltage (ZVT) MOSFETs and thick gate oxide input/output (I/O) MOSFETs. In this paper, ZVT and I/O MOSFETs were implemented in the asymmetric-threshold voltage (VTH) self-cascode (SC) structures. These asymmetric-VTH SC structures with optional devices and a two-stage operational amplifier (OPAMP) using these SC structures were fabricated and evaluated. As a result of single device level evaluation, the SC with ZVT MNOSFET device showed improved output resistance as well as transconductance than the conventional single MOSFETs. From measurements of the fabricated two-stage OPAMP, the OPAMP with ZVT-SC device showed higher DC gain, faster slew rate, and higher unity-gain frequency.**

I. INTRODUCTION

CMOS integrated circuits (ICs) are normally composed of digital logics and embedded analog circuits for mixed-signal system-on-a-chip applications [1]. In modern standard digital-CMOS technologies, generally, core MOSFETs have been optimized for high-performance digital logic functions, such as high speed, low power consumption, and small dimensions. On the other hand, the core MOSFETs are unsuitable for analog circuits because of channel length modulation (CLM) [2]-[4]. To overcome CLM effects, analog circuit designers prefer to use longer channel transistors or conventional cascode structures. The self-cascode (SC) is used widely for low-voltage analog circuits because of its high output resistance (r_{out}) and wide output voltage swing [5]-[6]. However, the large channel width and length (W/L) ratio of the two MOSFETs in the SC structure is one of its disadvantages. To save silicon die area, asymmetric threshold voltage (V_{TH}) SC structure using low-V_{TH} MOSFET has been proposed [7]. On the other hand, this approach requires additional V_{TH} adjustment process steps. Another SC technique using forward body-biasing was proposed [8]-[9]. This technique is suitable for a p-channel SC in the standard CMOS process with a p-substrate, but cannot be used for a body grounded n-channel MOSFET (nMOSFET) in standard CMOS technology. In this case, triple-well or silicon-on-insulator (SOI) CMOS technology is required.

In this paper, we propose new SC configurations with two optional devices in a 0.18-μm standard digital-CMOS technology. Usually, modern standard CMOS technologies offer optional devices, such as zero-V_{TH} device for low-voltage circuits and thick gate oxide input/output (I/O) devices to connect with the off-chip components [10]-[11]. Simply, therefore, n-channel SC configurations can be implemented owing to the difference in V_{TH} between the core MOSFET and optional devices in standard CMOS technologies. In this experiment, two SC configurations are designed and fabricated using 0.18-μm standard digital-CMOS technology. One is composed of core and zero-V_{TH} MOSFETs, and the other is composed of core and I/O MOSFETs. Basic current-voltage characteristics of the fabricated SC devices are evaluated. The advantages and disadvantages of each SC structure are discussed in detail from the experimental results. Moreover, an operational amplifier (OPAMP) example is also discussed and used to confirm the circuit performance.

II. SELF-CASCODE STRUCTURE

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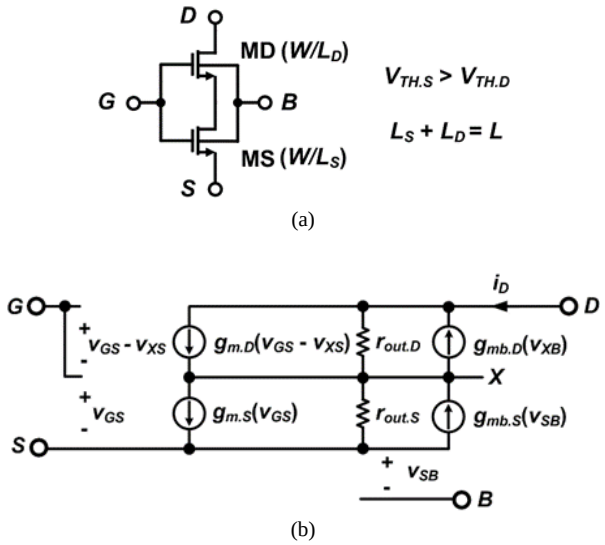


Fig. 1. (a) n-channel self-cascode structure (b) equivalent small-signal model

A. Asymmetric threshold voltage self-cascode structure

Fig. 1(a) presents the n-channel self-cascode structure. The nMOSFETs MD and MS are connected in series, and their gates and bodies are commonly connected. Therefore, the SC works as a single MOSFET. An asymmetric-V_{TH} SC is implemented if the V_{TH} of the source-side MOSFET MS is higher than that of the drain-side MOSFET MD ($V_{TH.S} > V_{TH.D}$). The channel width (W) of the two MOSFETs is identical. The SC structure is a well-known circuit configuration for low-voltage analog circuit design because of its high output resistance (r_{out}) and wide output voltage swing [5]-[7]. The MOSFET MS normally operates in the triode regime and MD operates in the saturation regime. If the V_{TH} of MD is lower than that of MS, the channel resistance and drain-source voltage V_{DS} of MD decrease and V_{DS} of MS increases at a constant current. Therefore, both transistors MD and MS can be operated in the saturation regime and the effective output resistance of the SC ($r_{out.SC}$) can be enhanced. The condition Eq. (1) must be satisfied to guarantee the SC structure in the saturation regime [7].

$$V_{DS(sat).D} \geq V_{TH.S} - V_{TH.D} \tag{1}$$

where $V_{TH.S} > V_{TH.D}$, $V_{DS(sat).D}$ is the drain-source voltage of MD, and $V_{TH.S}$ and $V_{TH.D}$ are threshold voltage of MS and MD, respectively. The minimum voltage headroom is $2V_{DS(sat)}$ in the saturation regime and the voltage headroom of the SC increases with decreasing $V_{TH.D}$.

The output resistance of SC, $r_{out.SC}$ in the saturation regime is obtained using the equivalent small-signal model, as shown in Fig. 1(b). V_S and V_B are set to 0 V in the analysis. The small-signal drain current (i_D) through two MOSFETs can be expressed as

$$i_D = g_{m.D}(-v_{XS}) + \frac{v_{DS} - v_{XS}}{r_{out.D}} - g_{mb.D}(v_{XS}) \tag{2}$$

$$i_D = \frac{v_{XS}}{r_{out.S}} \tag{3}$$

where $g_{m.D}$ and $g_{mb.D}$ are transconductance and body-effect transconductance of MD, respectively. $r_{out.D}$ and $r_{out.S}$ are output resistance of MD and MS, respectively. From (2) and (3), $r_{out.SC}$ is

$$r_{out.SC} = \frac{v_{DS}}{i_D} = (1 + (g_{m.D} + g_{mb.D})r_{out.D})r_{out.S} + r_{out.D} \tag{4}$$

Because output resistance is much larger than transconductance in the saturation regime, Eq. (4) is simplified as

$$r_{out.SC} \approx g_{m.D}\, r_{out.D}\, r_{out.S} \tag{5}$$

The effective transconductance of the SC ($g_{m.SC}$) in the saturation regime, and the small-signal drain current can also be obtained as follows:

$$i_D = g_{m.D}(v_{GS} - v_{XS}) + \frac{-v_{XS}}{r_{out.D}} - g_{mb.D}(v_{XS}) \tag{6}$$

$$i_D = g_{m.S}(v_{GS}) + \frac{v_{XS}}{r_{out.S}} \tag{7}$$

where $g_{m.S}$ is transconductance of MS, From (6) and (7), $g_{m.SC}$ is

$$g_{m.SC} = \frac{i_D}{v_{GS}} = \frac{(g_{m.D} + g_{mb.D})g_{m.S} + \frac{g_{m.D}}{r_{out.S}} + \frac{g_{m.S}}{r_{out.D}}}{g_{m.D} + g_{mb.D} + \frac{1}{r_{out.S}} + \frac{1}{r_{out.D}}} \tag{8}$$

Eq. (8) can be simplified as follows:

$$g_{m.SC} \approx g_{m.S} \tag{9}$$

$g_{m.SC}$ is dominated by the g_m of the source-side transistor MS. Therefore, an asymmetric-V_{TH} SC can have a higher g_m and r_{out} with similar $V_{DS(sat)}$ of a single MOSFET.

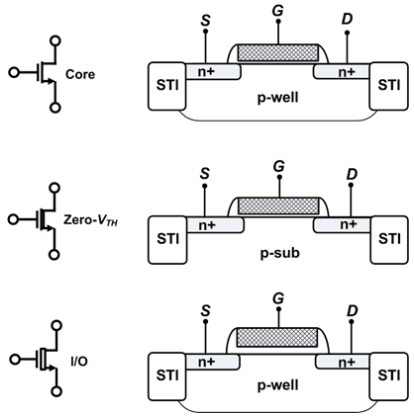


Fig. 2. Cross-section of n-channel optional devices in the standard CMOS process.

B. Self-cascode structures using optional devices

Fig. 2 shows n-channel core and two optional devices, which are commonly available in modern foundry CMOS technology. The zero-V_{TH} device (also called a native device) is identical to a core MOSFET but has a near zero V_{TH} [10]. The zero-V_{TH} device is used for low-voltage analog amplifiers such as the source follower and transmission gates in digital logics. On the other hand, p-channel zero-V_{TH} MOSFET is unavailable in CMOS processes with a p-substrate. Standard CMOS technologies also offer n- and p-channel I/O devices.

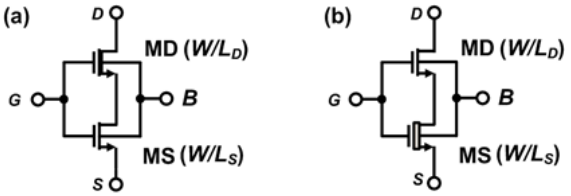


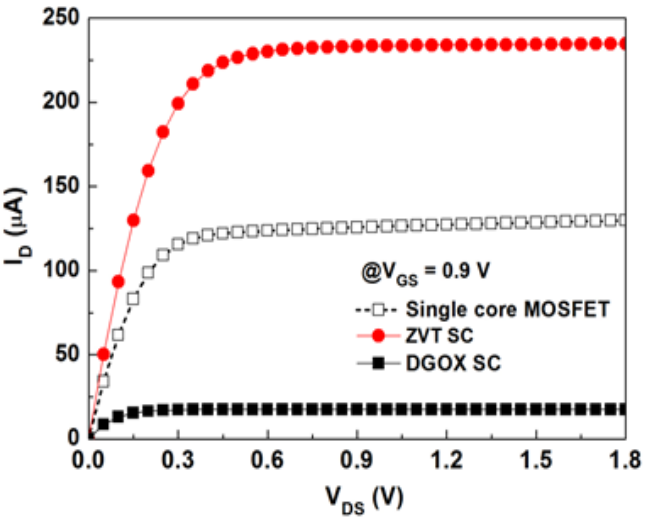
Fig. 3. n-channel self-cascode structure using optional devices. (a) ZVT (b) DGOX SC

Fig. 3 shows two possible SC structures using optional devices in 0.18-μm standard CMOS technology. One SC configuration was composed of the core and zero-V_{TH} MOSFET, as shown in Fig 3(a), which is called a zero-V_{TH} (ZVT) SC. The difference in V_{TH} between the core and I/O device was 0.50 V because the V_{TH} value of the core MOSFET was 0.50 V. The other SC configuration using I/O and core MOSFET, as shown in Fig 3(b), is called the dual gate oxide (DGOX) SC. The V_{TH} of an I/O MOSFET was 0.78 V and the V_{TH} difference between of I/O and core device was 0.28 V, respectively. For this experiments, the W/L of the transistor MS and MD in the fabricated ZVT and DGOX SC structure was 10.0/0.5 μm/μm. Therefore, the total channel length ($L = L_S + L_D$) was 1.0 μm. A single core MOSFET with equivalent dimensions (W/L = 10.0/1.0 μm/μm) was also fabricated for a comparative study.

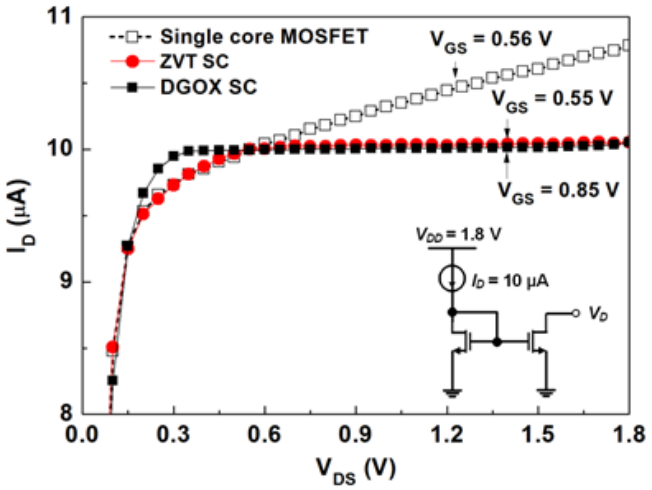
III. EXPERIMETAL RESULTS

A. Performance of the self-cascode structures using optional devices

Fig. 4 shows the measured I_D-V_{DS} characteristics of the ZVT and DGOX SC structures. As shown in Fig. 4(a), the drain current of the ZVT SC structure under identical bias conditions (V_{GS} = 0.9 V & V_{DS} =1.8 V) was improved by 89 % compared to that of the single core MOSFET. The zero-V_{TH} device in the ZVT SC can improve the drain current. On the other hand, the DGOX SC showed a much lower I_D due to the higher V_{TH} of the I/O device. The poor drain current of the DGOX SC requires a large channel width. At an identical drain current I_D = 10 μA, the I_D of the single core MOSFET increased largely with increasing drain voltage, as shown in Fig. 4(b). The ZVT and DGOX SC structures, however, showed no significant CLM. This is evidence of the r_{out} improvement in the two SC structures. The r_{out} values of the ZVT and DGOX SC structures were 7.7 and 21.6 MΩ, respectively, at V_{DS} = 0.9 V. Although the ZVT SC showed a lower output resistance than the DGOX SC due to the lower r_{out} of the zero-V_{TH} MOSFET, the r_{out} of the ZVT SC was five times larger than the 1.5 MΩ obtained for the single core MOSFET. Generally, an improved r_{out} is useful for active loads. From Eq. (1), the saturation conditions of both transistors of SC are dependent on the difference in V_{TH} between the two MOSFET (ΔV_{TH} = $V_{TH.S}$ - $V_{TH.D}$). The $V_{DS(sat)}$ of the DGOX SC was slightly lower than that of the ZVT SC because the ΔV_{TH} values of ZVT and DGOX SC were 0.50 and 0.28 V, respectively.



(a)



(b)

Fig. 4. Measured ID–VDS characteristics of the self-cascode structures (a) ID–VDS characteristics at identical VGS (b) ID–VDS characteristics at an identical drain current.

Fig. 5 shows the transconductance and drain current as a function of the gate voltage. Generally, the larger I_D of the transistor results in higher g_m. The ZVT SC showed higher g_m than the single core MOSFET and approximately 88 % improvement at $V_{DS} = V_{GS} = 0.9$ V. On the other hand, the g_m of the DGOX SC was much lower than that of the single core MOSFET because the DGOX SC showed a higher V_{TH} and lower drain current characteristics because of the source-side I/O device. Small g_m characteristics of the DGOX SC from Eq. (9) can also be expected.

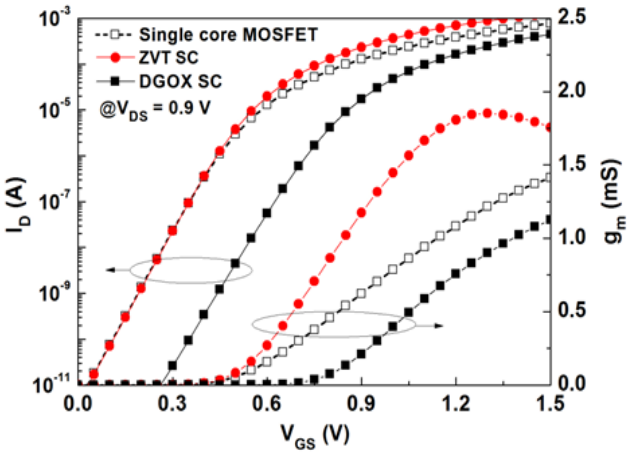


Fig. 5. Measured ID–VGS and gm–VGS characteristics of the self-cascode structures.

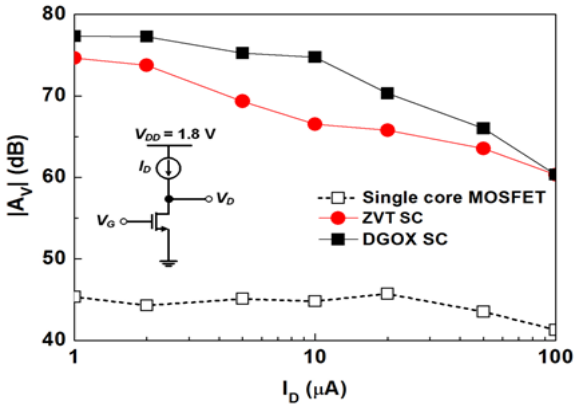


Fig.6. Measured intrinsic voltage gain (AV) of the self-cascode structures as a function of the drain current.

TABLE I. PERFORMANCE OF THE SELF-CASCODE STRUCTURE

Items	Single Core MOSFET	ZVT SC	DGOX SC
Channel width (W)	10.0 μm	10.0 μm	10.0 μm
Channel Length (L) (L_S+L_D)	1.0 μm	1.0 μm (0.5 μm + 0.5 μm)	1.0 μm (0.5 μm + 0.5 μm)
ΔV_{TH} ($V_{TH.S}$-$V_{TH.D}$)	-	0.50 V (0.50 V – 0.00 V)	0.28 V (0.78 V – 0.50 V)
$I_{D(sat)}$ (V_{DS}=1.8V, V_{GS}=0.9V)	125.6 μA	233.5 μA	17.4 μA
g_m (V_{DS}=0.9V, V_{GS}=0.9V)	0.62 mS	1.17 mS	0.21 mS
r_{out} (V_{DS}=0.9V, I_D=10 μA)	1.5 MΩ	7.7 MΩ	21.6 MΩ
A_V (V_{DS}=0.9V, I_D=10 μA)	44.8 dB	66.5 dB	74.7 dB

The improved r_{out} and g_m characteristics of a transistor can achieve a larger intrinsic voltage gain (A_V). Fig. 6 shows the intrinsic voltage gain ($A_V = \partial V_{OUT}/\partial V_{IN}$) as a function of the drain current. An external current source was applied to the drain node and the voltage transfer characteristics (VTC) were measured. The A_V was extracted from slope of the VTC at V_{DS} = 0.9 V. The A_V of the ZVC and DGOX SC at I_D = 10 μA was 66.5 and 74.0 dB, respectively, whereas the A_V of the single core MOSFET was 44.8 dB.

Consequently, the ZVT SC showed an improved drain current, transconductance and output resistance without an increase in V_{TH}, compared to the single core MOSFET. The DGOX SC also showed the largest output resistance and intrinsic gain except for the higher V_{TH}. Table 2 lists the measured performance data of the SC structures, which was discussed so far.

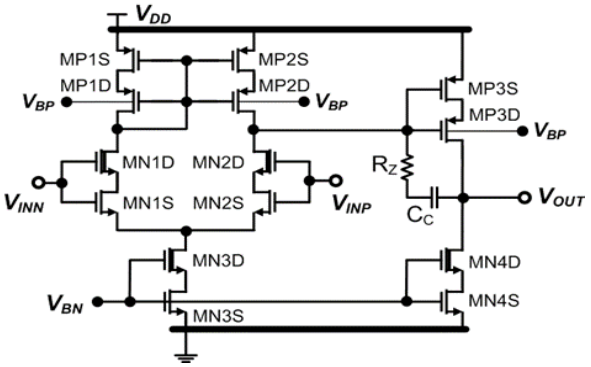


Fig. 7. Circuit diagram of the two-stage OPAMP using the self-cascode structures. Unless shown otherwise, the body terminal of each pMOSFET was connected to VDD and the body terminal of each nMOSFET was connected to the ground.

B. Performance of operational amplifier using the self-cascode structures

It is hard to fully evaluate performance of the SC configuration with single device level. An operational amplifier (OPAMP) is one of most popular analog building blocks of mixed-signal systems. Therefore, a two-stage OPAMP with the asymmetric-V_{TH} SC structures was designed to confirm the performance improvement. The SC structures were used in the design of the two-stage OPAMP, as shown in Fig. 7. As discussed earlier, the DGOX SC structure is unsuitable for low-voltage analog circuits because of the high V_{TH} and low drain current characteristics. Thus, OPAMP with the ZVT SC is only considered in this work.

To enhance the performance of the OPAMP, ZVT SC structures were used for the differential input pairs, MN1-MN2, and for the current mirror, MN3-MN4. In addition, the forward body-biased p-channel SC (pSC) structures were used for the active load MP1-MP2 and 2nd stage common-source amplifier MP3 [9]. The tail current of MOSFET MN3 was 20 μA. The conventional OPAMP composed of the single core n- and p-channel MOSFETs was also designed to compare the performance comparison.

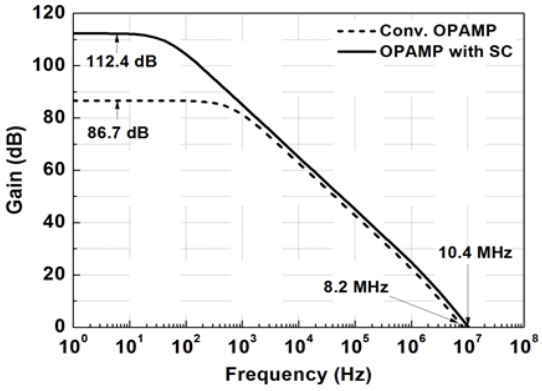


Fig. 8. Simulated open-loop frequency response of two-stage OPAMPs. Load capacitor CL = 15pF. Compensation capacitor (CC) and resistor (RZ) are 1.3 pF and 35 kΩ, respectively.

Fig. 8 shows the simulated frequency response of both the conventional OPAMP and the OPAMP with the SC structures. The DC gain of OPAMP with the SC structures was 112.4 dB, which was 25 dB higher than that of the conventional OPAMP. The improved r_{out} of the ZVT SC and body-biased pSC resulted in the higher DC gain of OPAMP. A simple measurement technique using a servo loop and auxiliary OPAMP (μA741) was used to measure the DC gain [12]. The measurement results also showed approximately 9 dB higher DC gain of the OPAMP compared to that of the conventional OPAMP.

In addition, the unity-gain frequency (f_T) of the OPAMP with the SC was 10.4 MHz, which was 2 MHz higher than that of the conventional OPAMP. The improvement in g_m of the ZVT SC in the differential input pairs resulted in higher f_T. The common-mode rejection ratio (CMRR) and the power-supply rejection ratio (PSRR) were proportional to the output resistance of the tail current source. Therefore, the r_{out}-enhanced SC, MN3, in Fig. 7 achieved approximately 10 dB improvement in the CMRR and PSRR.

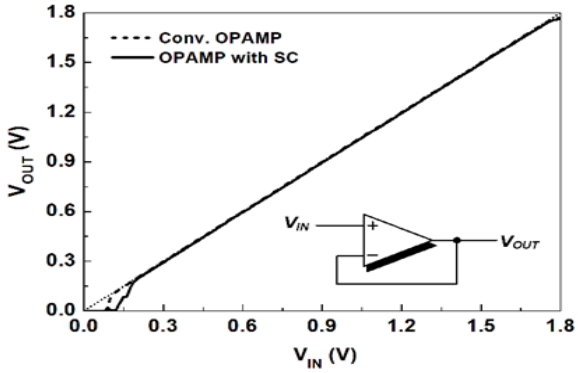


Fig. 9. Measured DC transfer characteristics of the unity-gain buffer using the fabricated OPAMPs. Non-inverting input VIN was applied from 0 V to 1.8 V.

Fig. 9 shows the measured DC transfer characteristics of the unity-gain buffers. The applied input voltage V_{IN} was varied from 0 V to 1.8 V. The output voltage of the OPAMP with the SC structures ranged from 190 mV to 1.76 V. 70mV difference in minimum allowable input voltage was observed due to the $V_{DS(sat)}$ of tail current source SC, MN3.

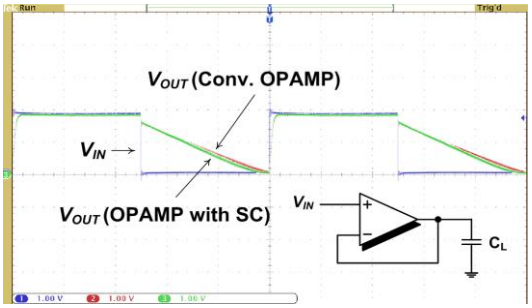


Fig. 10. Measured large signal step response of the unity-gain buffer using the fabricated OPAMPs. Off-chip load capacitor CL=15pF. Applied step input voltage VSTEP and frequency were 1.8 V and 100 kHz, respectively.

Fig. 10 shows the measured large-signal step response of the unity-gain buffers. The load capacitor, C_L was 15 pF. The applied step input voltage and frequency were 1.8 V and 100 kHz, respectively. The maximum falling slew rate of the OPAMP was equivalent to the ratio of the discharging current of MN4 and load capacitor C_L ($\approx I_{MN4}/C_L$). The falling slew rate of the OPAMP with the SC structures was -0.5 V/μs, showing 20% improvement compared to the conventional OPAMP with a single MOSFET. The improved drain current of the ZVT SC can result in more rapid discharge of the load capacitance [13]. Table II presents a summary of the OPAMP with the SC and the conventional OPAMP.

Fig. 11 shows a photomicrograph of the OPAMP with the SC structures, which was fabricated using a standard 0.18-μm CMOS process. The chip area was 6,642 μm^2.

TABLE II.
PERFORMANCE SUMMARY OF THE TWO-STAGE OPAMPS

Items	Conventional OPAMP	OPAMP with SC
Supply voltage	1.8 V	
Tail current	20 μA	
*Power consumption	71.7 μW	70.8 μW
*DC gain	71.1 dB	80.0 dB
Phase margin	48.6 degree	45.9 degree
Unity-gain frequency	8.2 MHz	10.4 MHz
*Output swing	0.12 – 1.77 V	0.19 – 1.76 V
*Slew rate (falling)	-0.4 V/μS	-0.5 V/μS
CMRR	85.3 dB	93.6 dB
PSRR+/-	224.2 / 86.7 dB	233.5 / 112.4 dB
*Offset	1.8 mV	5.3 mV

Off-chip load capacitor C_L=15pF. Compensation capacitor (C_C) and resistor (R_Z) were 1.3 pF and 35 kΩ, respectively. *measurement results.

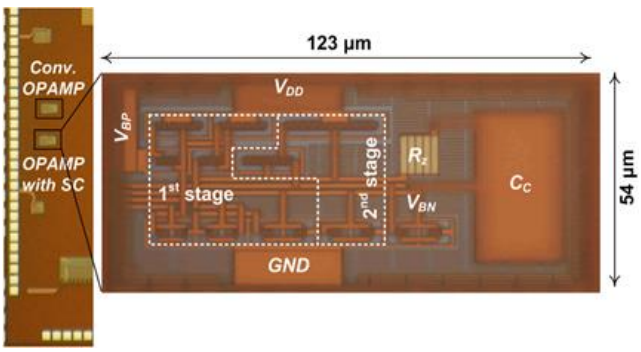


Fig. 11. Photomicorgraph of the fabricated OPAMP with the SC structures. The chip area was 123 μm x 54 μm.

IV. CONCLUSIONS

This paper reports the performance of asymmetric-V_{TH} self-cascode structures using optional devices in standard 0.18-μm CMOS technology. The performance of the two possible self-cascode configurations, zero-V_{TH} and DGOX self-cascode structures were investigated. The zero-V_{TH} self-cascode showed better transconductance and the DGOX self-cascode structures showed better output resistance and intrinsic voltage gain. Although both self-cascode structures showed some weaknesses, their analog performance was much better than that of the single core MOSFET. The enhanced electrical characteristics of the self-cascode structures using the optional devices are expected to be useful for the design of analog circuits in standard digital-CMOS technology.

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