Design and verification of internal core circuit of FlexRay transceiver in the ADAS

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Abstract **- Recently, many people engaged in domestic semiconductor design are growing interest in the automotive and semiconductor research and development, but to a variety of semiconductors, lack the research and development of FlexRay transceivers in the spotlight as the next generation communication vehicles. Because FlexRay communication uses two bus lines and two channels, which are differential signals, it is very strong against noise and high reliability. Currently, three domestic auto company buying FlexRay transceiver semiconductor need a lot of research to localize because it uses to import 100%. This paper's core blocks were designed, fabricated, and tested to localize the FlexRay transceivers, and develop a FlexRay transceiver therewith.**

I. INTRODUCTION

Recently, self-driving system has become very important issues in vehicles. The self-driving system is that allows a car to drive without any special operation by the driver [1]. In order for a car to replace a driver, sensors that act as drivers are very important, and communication that processes the data of sensor is also very important. Vehicles network communication methods include CAN (controller area network), FlexRay and MOST communication. Among them, FlexRay communication is relatively fast and is actually used [2]. ECU (electronic control units) are connected structure in parallel in FlexRay communication. It has a speed of 10Mbps, which is about 10 times faster than CAN communication.

Figure 1 shows the block diagram of the FlexRay communication platform [3]. The block consists of communication controller, bus guardian, and bus driver. The block was controlled by microcontroller as host controller. Because it uses two bus lines and two channels, which are differential signals, it is very strong against noise and high reliability. In addition, FlexRay communication requires a FlexRay transceiver that transfers data between ECUs. Now, the FlexRay transceiver in the Korea is 100% imported from overseas.

Figure 2 shows the internal block of the actual FlexRay transceiver. Each block plays a role of data signal processing and error signal detection [4]-[5].

In this paper, we design and verify the internal core blocks (transmitter driver, receiver, clock generator, time-out, comparator with hysteresis, bus fail detector, and LDO) of FlexRay transceiver, targeting commercial chip for localization to FlexRay transceiver.

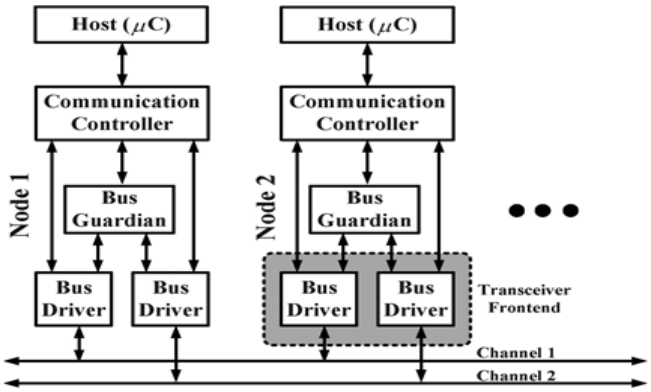

Fig. 1. Block diagram of FlexRay communication platform

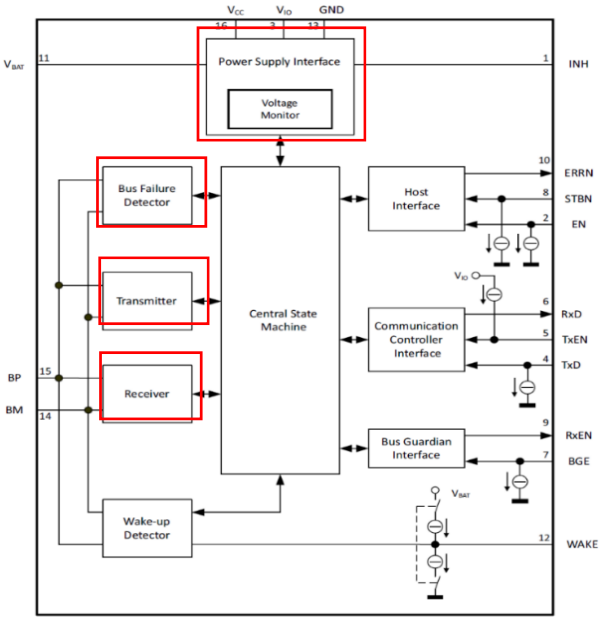

Fig. 2. Block diagram of FlexRay transceiver

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II. CIRCUIT DIAGRAM AND SIMULATION

Figure 3 shows the transmitter circuit to driver output signal that converts the ECU signal to the BP and BM differential signals in the FlexRay transceiver. The internal block consists of NOR, NAND, inverter, switch, and resistor. The operation principle is that the EN signal and the ENB signal are output according to the NOR operation of the Idle and Idle_LP signals. Depending on the state of Idle_LP, the switch is shorted to Vref_P and the BP and BM outputs are offset by 1.65V of Vref_P. The transistors are turned on/off according to the states of Data0 and Data1, and then output as differential signals having offset of Vref_P, that is, BP and BM.

Figure 4 shows the waveforms of simulation result for the transmitter circuit. Data0 and Data1 signals are output to BP and BM only when both Idle and Idle_LP signals are low.

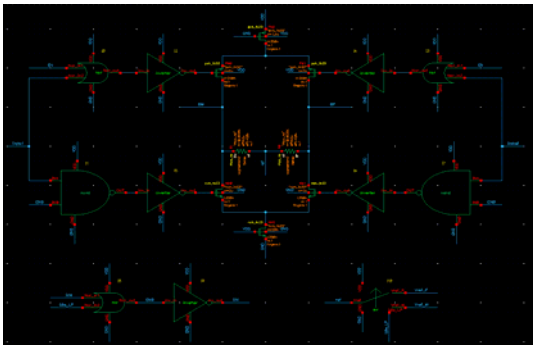

Fig. 3. Circuit diagram of transmitter block in FlexRay transceiver

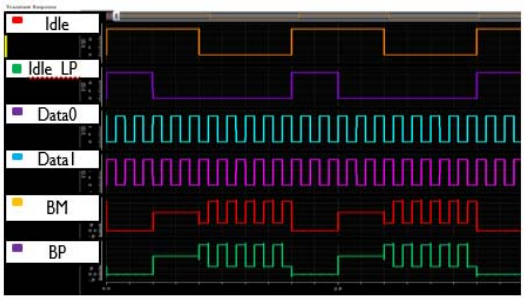

Fig. 4. Simulation waveforms of transmitter block

Figure 5 shows the receiver circuit that receives the BP and BM signals of the transmitter. The internal block consists of comparator, NOR, XOR, inverter, resistor, and capacitor. The attenuated voltage was obtained by connecting two resistors (equal in resistance value) to both ends of the BP and BM signals. BP and BM, the attenuated voltage is input to comparator, and the outputs of the two comparators below are output to the Ridle signal via XOR and inverter. This Ridle signal performs the nor operation with the output terminal of the top comparator and finally outputs the BP and BM signals to the Rdata signal, which is the ECU signal.

Figure 6 shows the simulation result of the receiver circuit. The Ridle signal is determined according to the Idle and Idle_LP signal. When Idle, Idle_LP and Ridle signals are both low, the BP and BM signals are output as Rdata, the ECU signal.

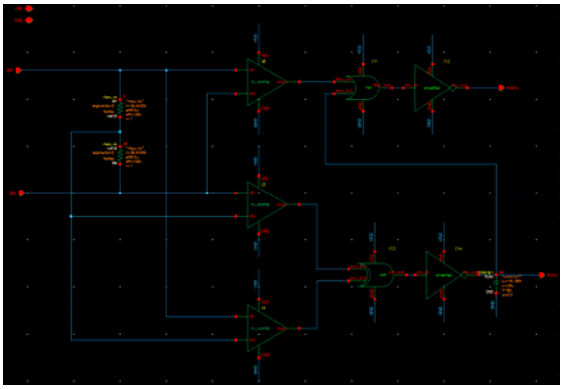

Fig. 5. Circuit diagram of receiver block in FlexRay transceiver

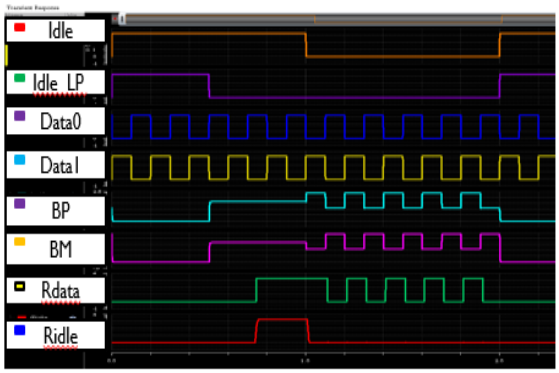

Fig. 6. Simulation waveforms of receiver block

Figure 7 is a circuit diagram of the clock generator. The clock generator is composed of two comparators, inverters, capacitors, RS-latch, and bias circuit. The operation principle is that Vref_H charge to capacitor when comparator is High, otherwise, Vref_L discharge from capacitor when comparator by Iref is low. The output the oscillation frequency was setting as a 4MHz. The following figure shows the simulation results depending on the value of Vref_H and Vref_L, capacitor.

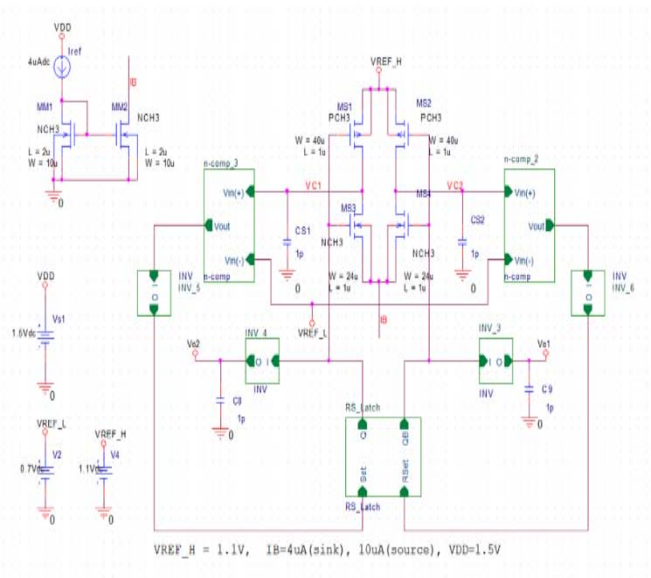

Fig. 7. Circuit diagram of clock generator

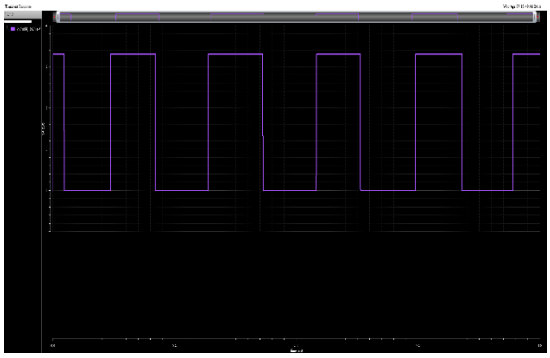

Fig. 8. Simulation waveform of clock generator
(Vref_H : 2.5V, Vref_L : 2V, CAP : 1pF)

Figure 9 is a circuit diagram of 3-bit time out circuit. This circuit is mainly composed of three D flip-flops (F/F) in series connection and a control logic circuits. To test 3-bit time-out, we use two signals of clock and TxD and applied in the circuit. The three D flip-flops (F/F) operate like a 3-bit counter in this circuit.

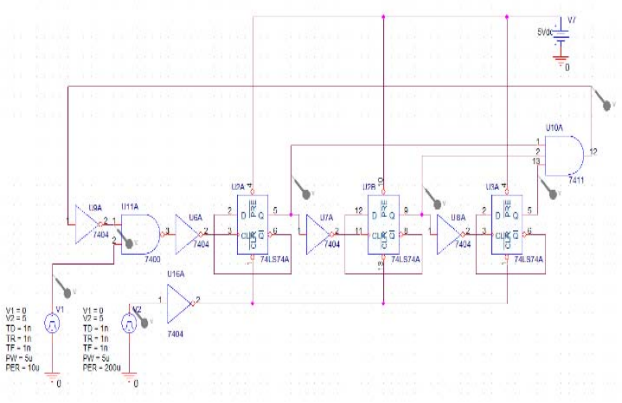

Fig. 9. Circuit diagram of time delay out

Figure 10 shows simulation results of 3-bit time-out circuit are shown in the Fig. 9. If TxD signal did not trigger the time-out block, the time-out signal will go to 'HIGH" mode after a 3-bit consecutive counting. This 'HIGH" signal will continue until a normal TxD signal input occurred to the circuit. If a "HIGH" signal in FlexRay transceiver in Fig. 3 is occurred, it turn-off the two power transistors in driver stage. Therefore, it protects the two power transistors and transceiver chip is also in safety operating mode when there is no signal being take place in TxD.

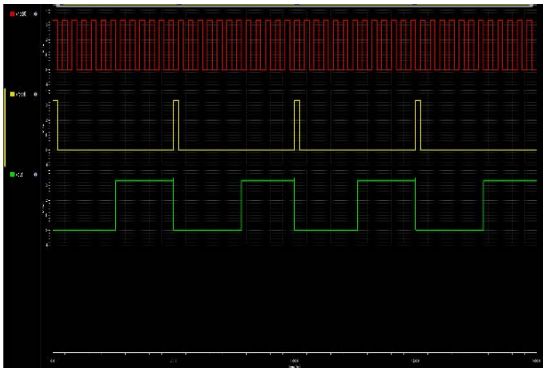

Fig. 10. Simulation waveform of time-out circuit

Figure 11 is a diagram showing the comparator with hysteresis circuit [6]. In this circuit, hysteresis is added to the two-stage amplifier plus output inverter comparator using a fixed-value resistor and a current steering circuit, as shown in the Figure 11. The circuit uses a current source, a differential amplifier and a fixed-value resistor to obtain hysteresis. It has an inverting hysteresis characteristic with equal positive and negative thresholds, V_{TH} and V_T. The effect is to move the negative input terminal by an amount equal to the hysteresis bias current multiplied by the fixed-value resistor, which can be expressed as $V_{TH} = - V_{TL} = R \times I_{hyst}$.

And, even if the noise generated between the input voltages is the reference voltage, the output voltage maintains a previous output value. Hysteresis current cannot be modified because it is fixed to the internal circuit. Therefore, it should be adjusted to the outside of the resistance value in order to adjust the hysteresis characteristic.

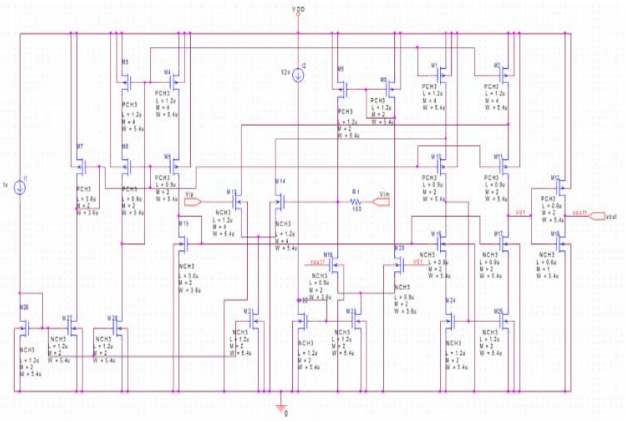

Fig. 11. Circuit diagram of comparator with hysteresis

Figure 12 shows the simulation waveform of comparator with hysteresis when hysteresis control resistor was 1kΩ.

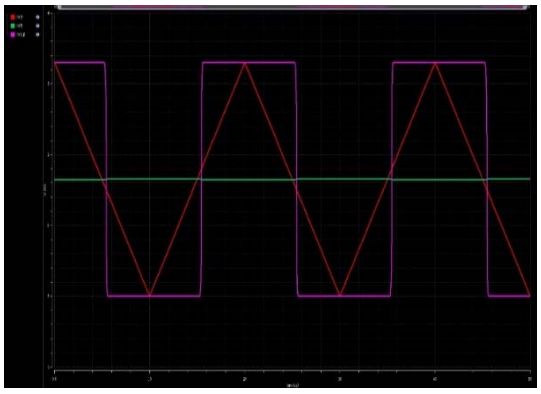

Fig. 12. Simulation waveform of comparator with hysteresis (1kΩ)

Figure 13 shows the bus-failure-detector circuit. The bus driver circuit outputs an error signal when the signal of the BP and BM was short to VDD and GND, respectively. The Vo1 becomes high when BP was a short in the VDD. The output Vo2 becomes high when the high was short to GND. As when BM was a short in the VDD Vo3 becomes high, the output Vo2 when the high was short to GND. The following figure 14 shows an output waveform corresponding to the signal of the BP and BM.

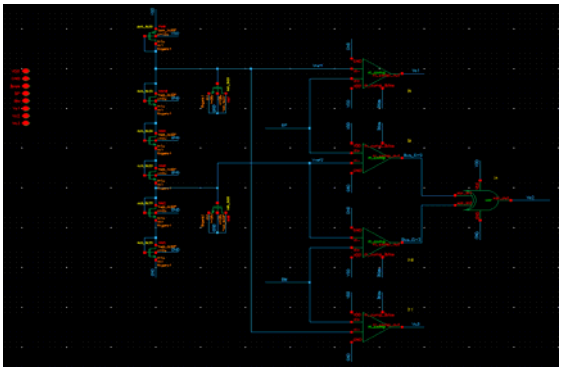

Fig. 13. Circuit diagram of bus failure detector

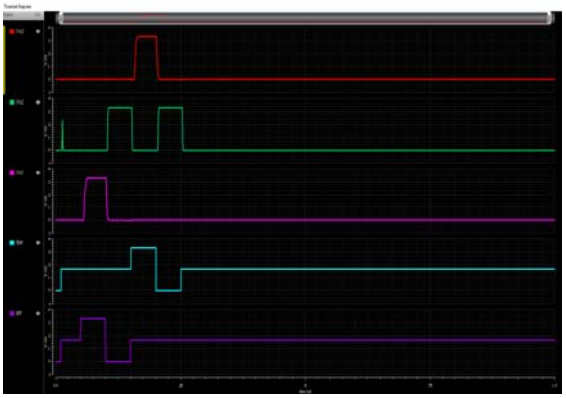

Fig. 14. Simulation waveform of bus failure detector

Figure 15 shows the LDO (low drop output regulator) circuit diagram [7]. The circuit outputs a constant voltage when the supply voltage is above a predetermined voltage. The circuit serves as a reference voltage or bias voltage to another circuit. The purpose of the LDO is to design a circuit supplying the reference voltage to the driver and clock generator circuit. Figure 16 shows the simulation result when supply voltage changes from 0V to 3.3V.

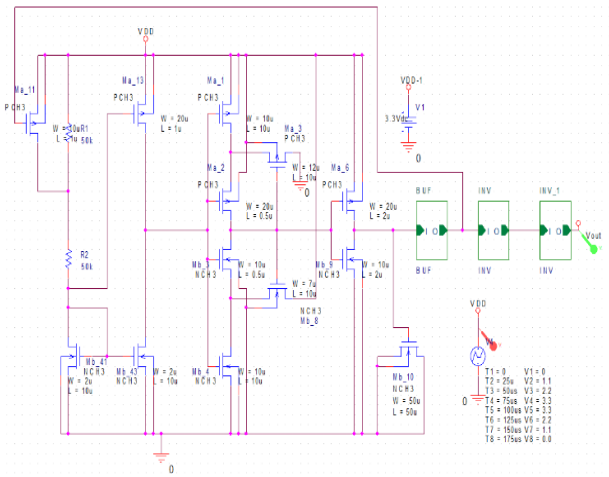

Fig. 15. Circuit diagram of LDO

III. EXPERIMENTS RESULT AND DISCUSSION

Figure 19 and 20 show the experimental results of the driver. Figure 19 shows the BP and BM output waveforms when the Idle and Idle_LP signals are low in the driver transmitter circuit. It can be confirmed that the differential signal output has an offset of 1.65V which is a reference voltage. Figure 20 shows the waveforms of the Rdata and Ridle, each is signals of the ECU and signal of enable. These signals are BP and BM signals received from the driver receiver circuit.

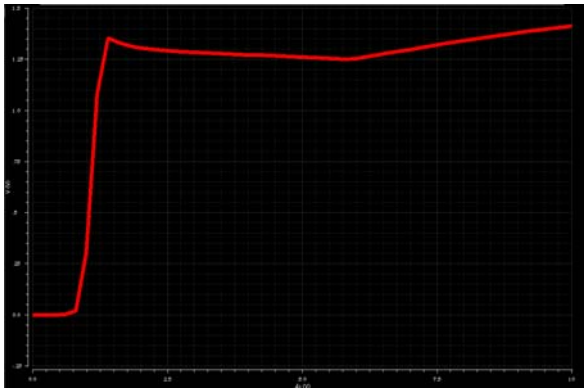

Fig. 16. Simulation waveform of LDO

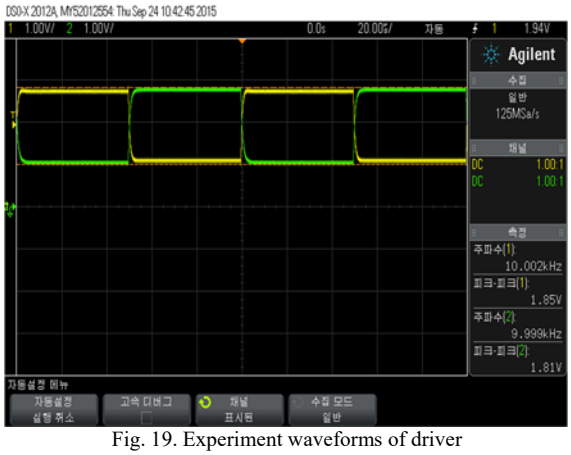

Fig. 19. Experiment waveforms of driver (BP, BM) for FlexRay transceiver

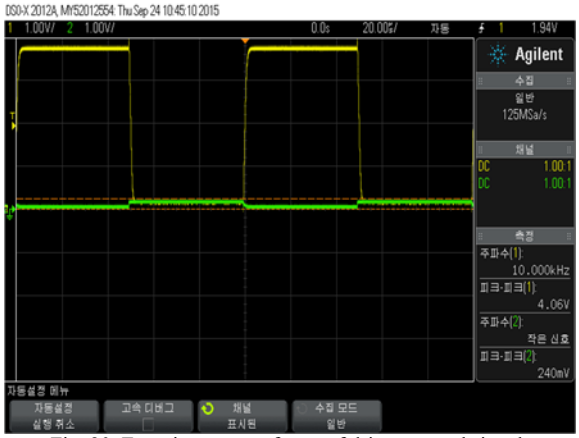

Fig. 20. Experiment waveforms of driver control signals (Rdata, Ridle) for FlexRay transceiver

The following figure 21 shows the experimental result of clock generator circuit. The following figure shows the experimental results depending on the value of Vref H, Vref, and capacitor. The output of oscillation frequency is 403.1kHz. The oscillation frequency changes depending on the value of Vref_H, Vref, or capacitor.

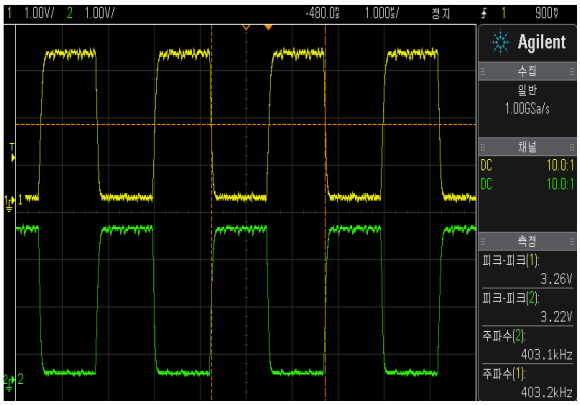

Fig. 21. Experiment waveforms of clock generator circuit (Vref_H : 2.5V, Vref_L : 2V, CAP : 1pF)

The following figure 22 and 23 show the experimental result of time-out circuit. Experiment with the clock signal was applied to the clock generator instead of a function generator. Similarly, the frequency is 50kHz signal TxD to export the error signal, a signal was applied to a 10% duty. According to two input signal (Clock and TxD) sends out a high output signal after counting a predetermined 3-bit in accordance with a D-flip flop of the 3-bit design.

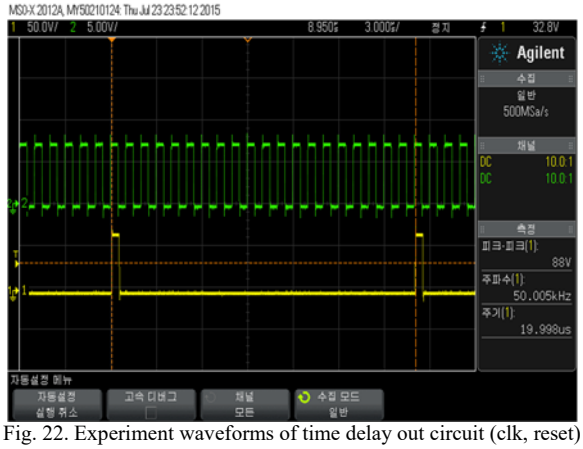

Fig. 22. Experiment waveforms of time delay out circuit (clk, reset)

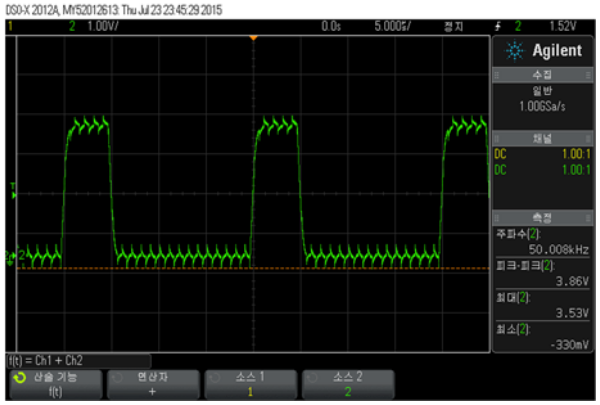

Fig. 23. Experiment waveforms of time delay out circuit (time out)

The following figure 24 and 25 show the experimental results of comparator with hysteresis circuit. Figure 24 and 25 show wave forms of the input and output when the hysteresis resistors was 20kΩ and 10kΩ, respectively.

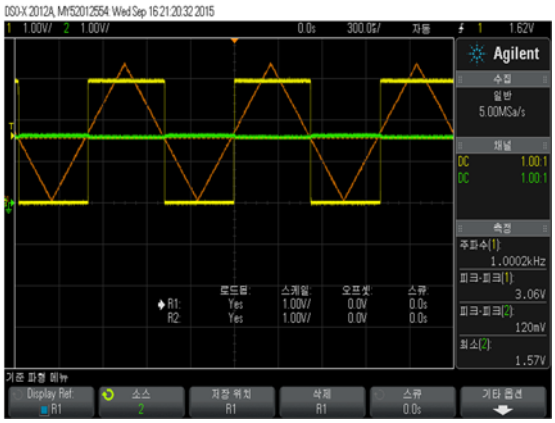

Fig. 24. Experiment waveforms of comparator with hysteresis (20kΩ)

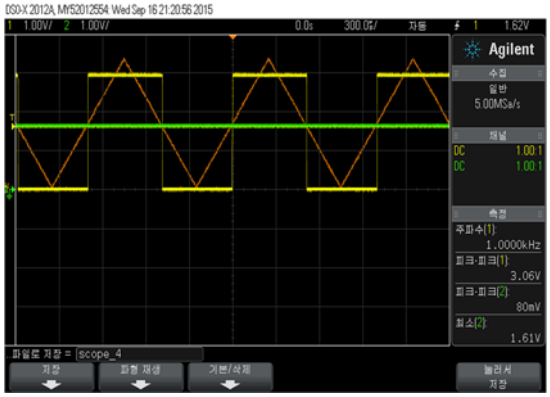

Fig. 25. Experiment waveforms of comparator with hysteresis (10kΩ)

Figure 26 and 27 show the experimental results of bus failure detector circuit. Figure 27 shows when the BM signal is normal. When BP is shorted to VDD, Vo1 outputs a high signal, and when BP is shorted to GND, Vo2 outputs a high signal. Figure 28 shows when the BP signal is normal. When BM is shorted to VDD, Vo3 outputs a high signal, and when BM is shorted to GND, Vo2 outputs a high signal. It was confirmed that the error signal was normally detected.

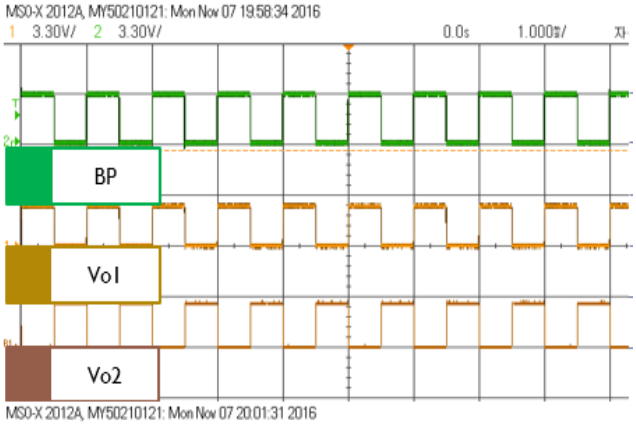

Fig. 26. Experiment waveforms of bus failure detector (BP, Vo1, Vo2)

Figure 28 shows the experimental result of the LDO. VDD was varied from 0 to 3.3V and the experiment was conducted. It was confirmed that the output voltage was constantly output from 1.5V to 1.5V.

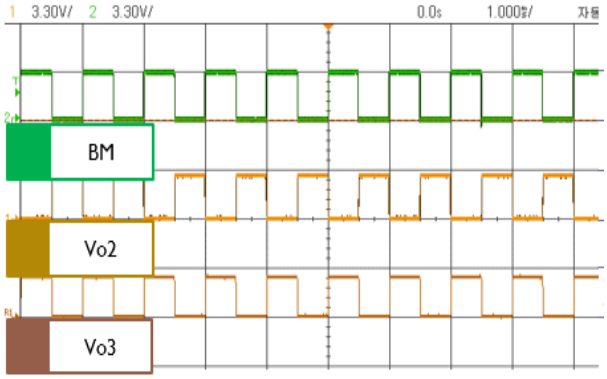

Fig. 27. Experiment waveforms of bus failure detector (BM, Vo2, Vo3)

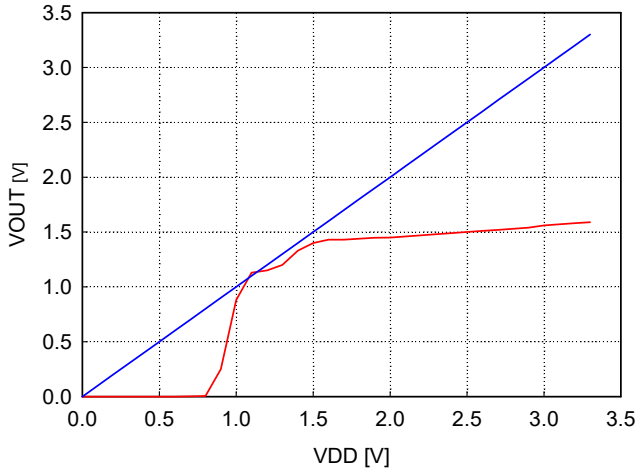

Fig. 28. Experiment waveforms of LDO

IV. CONCLUSIONS

In order to localize the FlexRay transceiver, we designed the internal core circuits driver (Tx, Rx), clock generator, time -out, comparator with hysteresis, bus failure detector, and LDO based on commercial FlexRay transceiver. It is confirmed that the experimental results of each block are similar to the simulation results. In the future, each block is combined into one block, and the performance is compared with commercial FlexRay transceiver, and it will be tested after connecting with FlexRay controller.

ACKNOWLEDGMENT

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