Implementation of power regulation unit for biomedical implantable devices

Sadeque Reza Khan and Goang Seog Choi
SoC Design Lab., Department Information and Communication Engineering, Chosun University
E-mail: gschoigs@chosun.ac.kr

Abstract **- Power supply of the biomedical devices such as pacemakers, artificial hearts, function electrical stimulators, monitoring devices, and retinal stimulator for long term operation is a challenging task. A major issue involved in the wireless power supply is the power flow regulation with proper efficiency. Therefore, a stable power regulating unit is required including band-gap reference (BGR) circuit and regulator to power up the implant with a stable dc voltage. In this paper, a temperature compensated BGR is proposed along with a stable capacitor-less low dropout (LDO) regulator. The proposed analog domain-based circuits are manufactured in SK Hynix 0.18um CMOS technology. The circuits presented in this paper have been implemented and the results have shown that the first bandgap reference (BGR) circuit has achieved power supply rejection ratio of 66 dB at room temperature. The gain of the proposed LDO regulator is 60dB. Furthermore, the drop out voltages of the LDO regulator is less than 200 mV. The stability of the regulator is measured with different capacitive load and currents and the gains in accordance with frequency response.**

Keywords **—Power flow regulation in biomedical implantable devices, Stable capacitor-less low dropout (LDO) regulator, Temperature compensated bandgap reference BGR**

I. INTRODUCTION

Biomedical implant devices are used in medical science for the accurate diagnosis of different diseases. Thus, acquiring the correct signal and powering up the devices inside the body are essential research topics in present days. Voltage references of process variations, voltage and temperature (PVT) independent are widely used in analog, mixed signal, RF, and digital circuits [1]. The circuit architecture of a voltage reference can be divided in to three primary sections: the generation of two voltages (or currents), one proportional and the other complementary to absolute temperature (PTAT and CTAT, respectively) and biasing. Furthermore, low-dropout (LDO) voltage regulator with low output ripple is the best option, especially for high performance and sensitive analog/mixed-signal blocks and radio frequency identification (RFID) application.

Bandgap reference (BGR) with traditional circuit architecture generates CTAT voltage with a p-n junction, which presents a slightly non-linear behavior over temperature [2]. Previous attempts mostly exploited two nodes to produce CTAT and PTAT currents by using equal valued resistors [3]. Additionally, the startup circuit design methodology for BGR followed in the past required either an external power on reset signal (POR) [4], or to be composed of several MOS transistors for generating bias current [5]. Further, the power supply rejection ratio (PSRR) against power spurious is the most important factor for BGR circuits when they are used with low dropout (LDO) regulators.

Several capacitorless (CL)-LDOs have been published in the recent years [6]. In [7], high power consumption-based LDO with capacitor multiplier stage to improve the dynamic performance is presented. The simple flipped voltage follower (FVF) structure LDO which reported in [8] has suffers from weak load and line regulations. Due to the simple folded structure, the LDO regulator in [9] can be made stable easily in exchange of loop gain which affects the load regulation of such structures. In [10], the design demonstrates a faster settling time but it suffers from larger undershoot and overshoot which makes this architecture improper in some applications. The proposed architecture in [11] can switch between two and three stages with respective power transistor, depending on load requirement. However, the quiescent current of the LDO is high at full-load condition and the circuit suffers from poor load and line regulations. A local common-mode feedback high slew-rate current-mode error amplifier-based LDO is proposed in [12] which managed to maintain low quiescent current and improved load transient performance. Nevertheless, the proposed LDO suffers from high output voltage variation when the load current changes in a full swing manner. Numerous researches demonstrated gain improvement techniques, such as cascading and gain boosting [13], [14]. These approaches rely on increasing the output resistance of an amplifier, and are widely accepted in sub-micron technology circuits. However, these approaches failed to maintain the trade-off between LDO speed and stability [15]. Another approach is to improve the loop gain by utilizing multiple high-gain stages. This method increases the gain by the cost of multiple low frequency poles. Consequently, internal compensation scheme would be required [16] using capacitors in the range of pico-farad (pF). This issue imposes area constraints to the system.

Manuscript Received Sep. 25, 2017, Revised Oct. 13, 2017, Accepted Dec. 02, 2017

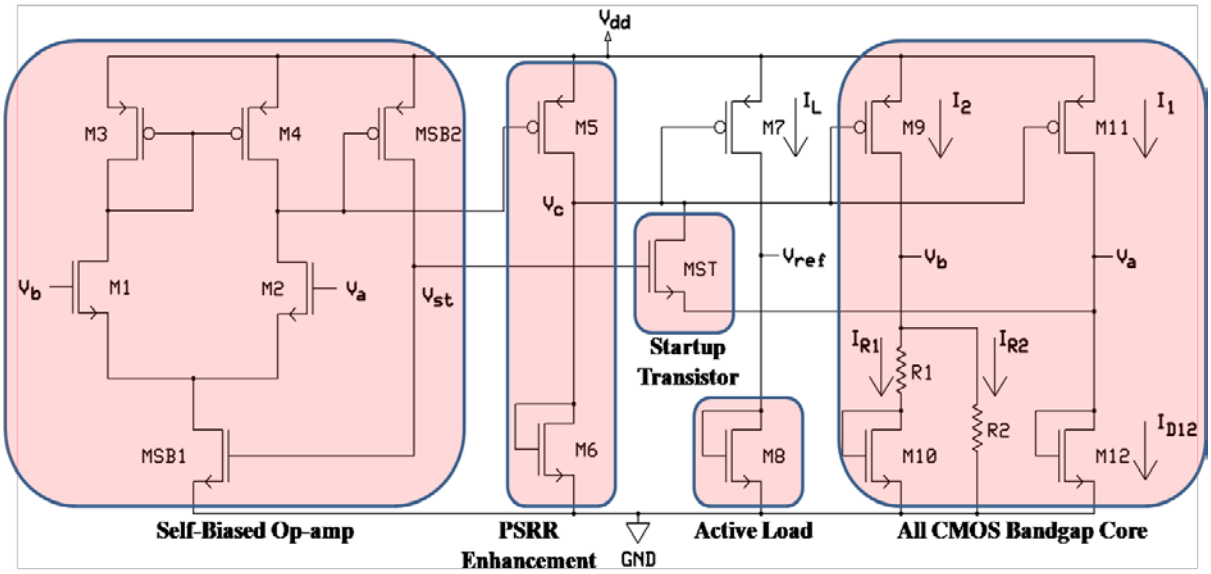

Fig. 1. Proposed BGR circuit.

This paper presents novel BGR and LDO architecture to mitigate previous disadvantages and provide high performance to the biomedical implantable devices. Proposed BGR circuit includes a PSRR enhancement stage. Further, this paper utilizes the gain improvement method using small-gain stage (SGS). On the other hand, the large sized pass transistor (PT) is segmented in to smaller sizes and an adaptive controller unit (ACU) is introduced to distribute the output current according to the load demands.

II. DESIGN ARCHITECTURE

A. BGR circuit

In Fig. 1, by considering the fact that, the active load transistor, M8 works in the saturation region, the BGR output voltage V_{ref} would be given by:

$$V_{ref} = V_{th,M8} + \sqrt{\frac{2I_L}{k_{M8}}} \tag{1}$$

where I_L is the bias current of M8 and $k_{M8} = \mu C_{ox}(W_{M8}/L_{M8})$. μ, C_{ox}, W, and L represent electron mobility in the channel, oxide capacitance per unit area, channel width, and length, respectively. From (1), both the first (threshold voltage, V_{th}) and second (mobility) component of V_{ref} are susceptible to the temperature coefficient, which can be completely suppressed by a bias current proportional to mobility.

The self-biased op-amp input voltage, V_a and V_b must be equalized by controlling the current I_1 and I_2. The common mode voltage V_c is responsible to maintain I_1, I_2, and I_L equal. V_b is the one-node of the Bandgap core circuit to generate temperature independent I_2, thus, I_L. I_2 is controlled by R1 and R2 resistor currents I_{R1} and I_{R2}, respectively, and M10. The diode connected NMOS, M10 and M12 are defined to operate in weak inversion regime. Fig. 1 shows that, V_{th} is inversely proportional to T. Thus, V_{gs1} (as well as I_{R2}) of (4) is proportional to CTAT. Consequently, I_{R1} and I_{R2}, which are connected in a common node, are used to produce the voltages which have the positive and negative temperature coefficients, respectively. Therefore, we can derive temperature independent I_L from (1) as:

$$V_{ref} = V_{th,M8} + \sqrt{2\left(\frac{V_{gs1}}{k_{M8}R2} + \frac{nV_T \ln(M)}{k_{M8}R1}\right)} \tag{2}$$

The gain of proposed BGR can be represented with A_1, A_2, and A_3, the open loop gains of the three stages. The overall open loop gain of the equivalent network is, $A = A_1A_2A_3$.The power supply gain of the network can be represented as, $A_p = A_{p3} + A_3 [1 - (A_{p2} + A_2 (1 - A_{p1}))]$. Thus, the PSRR of the equivalent network is:

$$PSRR = \frac{A}{A_p} = \frac{A_1A_2A_3}{A_{p3} + A_3[1-(A_{p2} + A_2(1-A_{p1}))]} \tag{3}$$

or

$$\frac{1}{PSRR} = -\frac{1}{A_1A_2PSRR_3} + \frac{1}{A_1A_2} + \frac{1}{A_1PSRR_2} - \frac{1}{A_1} + \frac{1}{PSRR_1} \tag{4}$$

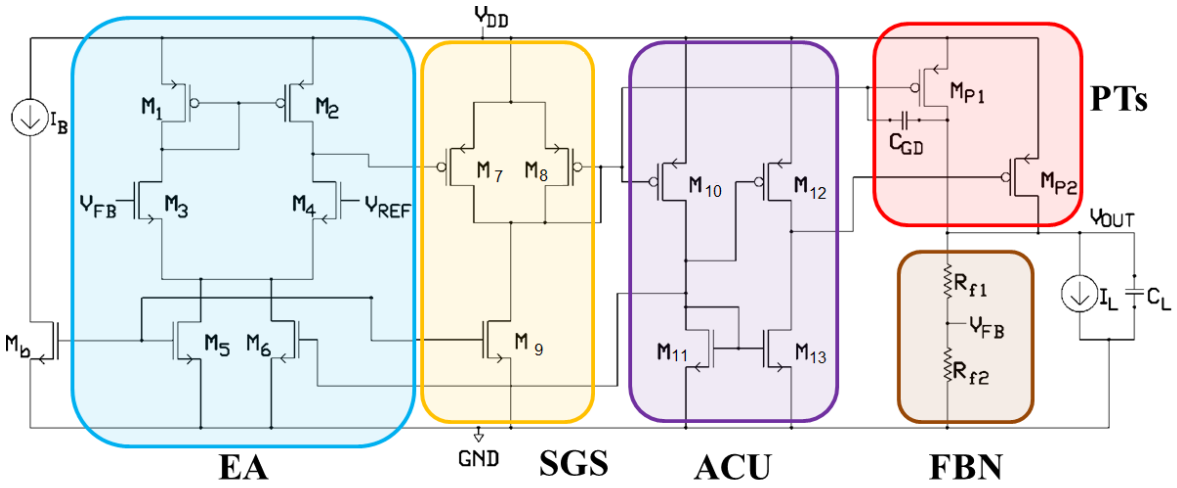

Fig. 2. Proposed LDO architecture.

where $PSRR_1 = A_1/A_{p1} = -g_{m,M1}/(g_{o,M1}+ g_{o,M4})$, $PSRR_2 = -A_2/A_{p2} = -g_{m,M5}/g_{o,M5}$, $PSRR_3 = -A_3/A_{p3} = -g_{m,M7}/g_{o,M7}$. $g_{m,Mi}$ and $g_{o,Mi}$ represent the transconductance and conductance of the transistors, where i = 1 to 8. By replacing the transconductace and conductance in (4), the modified equation (4) can be presented as:

$$PSRR = \frac{g_{m,M1}g_{m,M7}}{4g_{o,M2}g_{o,M5}g_{o,M7}} + \frac{g_{m,M1}g_{m,M5}}{6g_{o,M2}g_{o,M5}}, \quad g_{o,M1} = g_{o,M2} = g_{o,M3} = g_{o,M4}, \quad and\ g_{o,M5} = g_{o,M6}. \tag{5}$$

From (5), the PSRR can be improved significantly by adjusting $g_{o,M5}$.

B. LDO circuit

Fig. 2 shows the circuit structure of the proposed CL-LDO which consists of error amplifier (EA), SGS, and an ACU. The main PT is segmented into M_{P1} and M_{P2}. The feedback network (FBN) is formed by resistors R_{f1} and R_{f2}. In Fig. 2, the size of M_7 of SGS is k times of that of M_8 such that $(W/L)_8 = k \times (W/L)_7$. The total bias current is $(k + 1) \times I_B$. Therefore, M_7 has kI_B of drain current. Consequently, the gain of the SGS is roughly close to the multiplication factor k. Although the gain improvement is possible using a single SGS, it would be more power efficient if it is achieved using multiple SGSs of cascaded structure. In no load condition the stability performance of the LDO degrades due to the large capacitance at the gate terminal of a large PT which requires long time to charge and discharge. Therefore, the LDO suffers from unsatisfactory load and line regulation. In this paper, segmentation of PT is a subject to achieve better load transient response. The proposed LDO is designed with a small bias current IB and extra bias current for higher loads are provided using M_6 to achieve high current efficiency. Further, ACU is responsible to control the bias current through M_6 depending up on the load requirement.

In Fig. 2, there are three left-half-plane (LHP) poles and one right-half-plane (RHP) zero, given by $P_D = 1 / (R_{oPT}C_{oL})$, $P_1 = 1 / (R_{oSGS}C_{oSGS})$, $P_2 = 1 / (R_{oEA}C_{oEA})$, and $Z_1 = -g_{mPT} / C_{GDPT}$. The pole generated by the small stage, P_1 is located in high enough frequency that these poles would not create any stability issue. The ACU is designed in a way that its output pole is shifted at much higher frequencies. Therefore, this stage can be ignored for small signal analysis, and hence, for higher load currents, the total transconductance of PTs are sum (g_{mPT}) of the g_{mPT1} and g_{mPT2} that approximately equals g_{mPT2}. Because of reduced channel resistance and smaller size of the PTs, the dominant pole is approximately placed in the order of tens of kilohertz. Finally, the pole contributed by the input stage is exiled to several hundred megahertz.

Fig. 3 shows the open loop frequency response of the proposed LDO regulator with C_L = 100 pF, confirming that the LDO is stable over the entire load-current range.

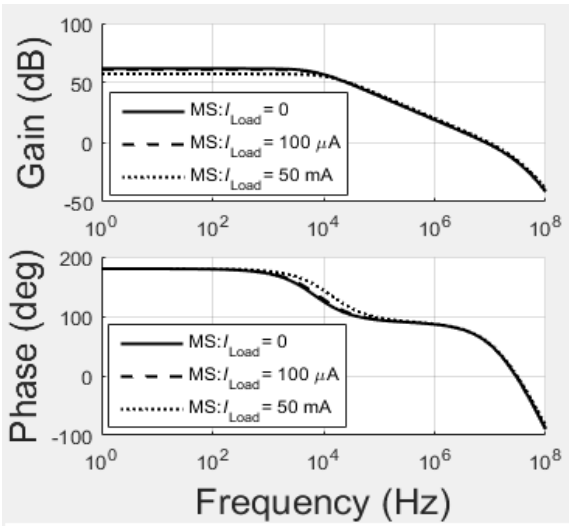

Fig. 3. Frequency response of the proposed LDO.

III. RESULTS AND DISCUSSION

The proposed BGR and LDO regulator is fabricated using Magnachip/SK Hynix 0.18 µm CMOS process. The fabricated chip and the layout of the device are shown in Fig. 4. The designed LDO regulator has been fabricated as a part (lower half) of 3.8 mm × 3.8 mm chip in a low profile quad flat package (LQFP).

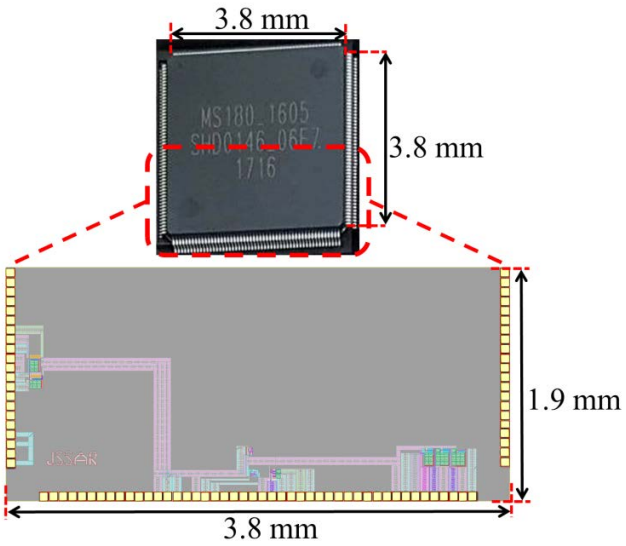

Fig. 4. Chip layout and fabricated IC.

Fig. 5 shows the variation of V_{ref} with the supply voltage. For a supply voltage from 0.9 to 4 V DC the proposed BGR generates average V_{ref} of 507 mV with a line sensitivity of 0.36% at 27˚C. In the range of 0 to 125˚C, the lowest temperature coefficient (TC) is 5.5 ppm/˚C for V_{dd} = 2 V, as show in Fig. 6. Comparing with the conventional BGR, the proposed architecture achieves 25dB of PSRR improvement, as show in Fig. 7.

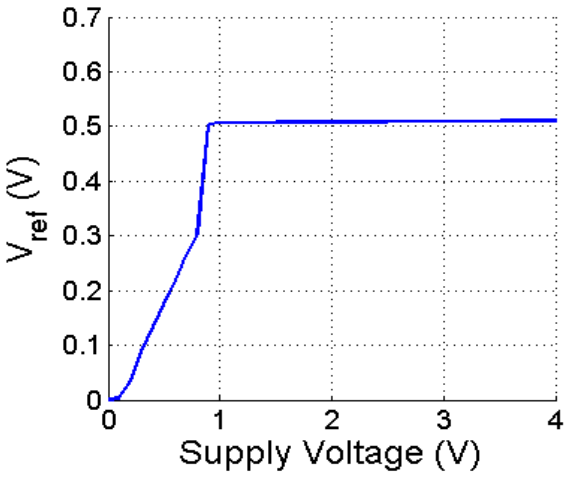

Fig. 5. V_{ref} vs. supply voltage.

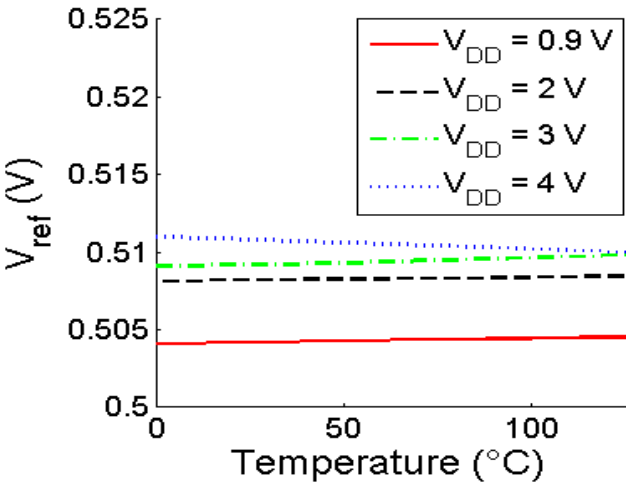

Fig. 6. V_{ref} vs. temperature.

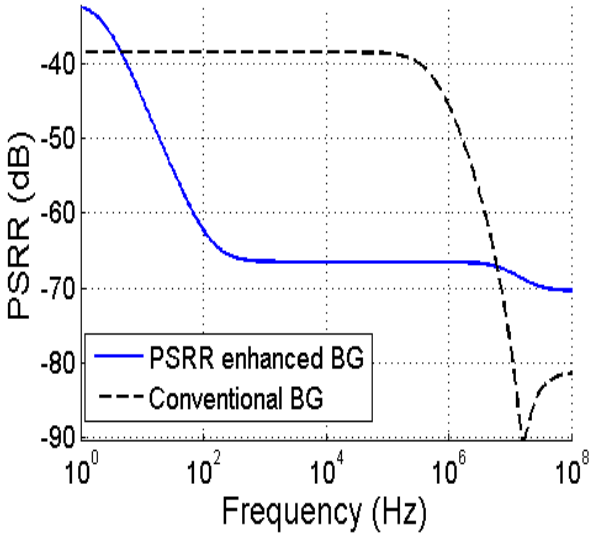

Fig. 7. PSRR vs. frequency.

The proposed LDO maintains a dropout voltage less than 200 mV at maximum load current. An external voltage reference of 0.5 V is used and an on-chip load capacitor, C_L = 100 pF is used for measurement. The load current is switched between 0 and 50 mA for the LDO with segmented PT and without segmented PT, respectively. The maximum output voltage deviation is approximately 51% lower in case of using segmented PT, and the settling time is faster, approximately 46% with segmented PT. A comparison between quiescent current of the LDO with and without the proposed segmentation technique is shown in Fig. 8. It can be seen that using the proposed two PT technique can reduce the quiescent current (I_Q) significantly and it maintains lower I_Q (less than 5 μA) over the whole load range. Fig. 9 shows the measured power supply rejection ratio (PSRR) performance of the proposed LDO. A PSRR of -52 at 1 KHz is maintained.

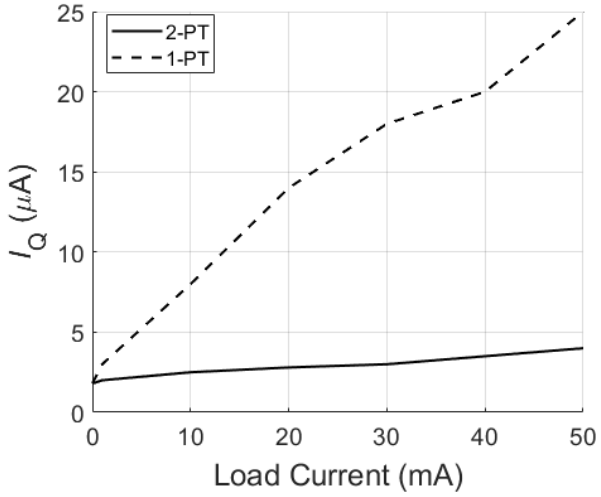

Fig. 8. Quiescent current comparison between with segmented PT and without segmented PT.

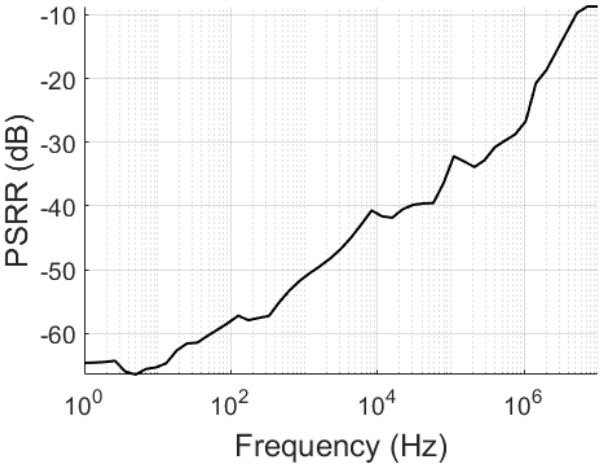

Fig. 9. Measured PSRR.

IV. CONCLUSIONS

A low power one startup transistor-based BGR is presented with a PSRR improvement stage. All CMOS bandgap core is implemented with only two resistors, which compensates the effect of temperature depends on one node and reduces the overall circuit area. Furthermore, in this paper, a low power LDO with one small-gain stage and segmented PT improves both loop gain and bandwidth. Moreover, the proposed LDO architecture does not require any compensation on-chip capacitor. Therefore, a lower active chip area is achieved.

ACKNOWLEDGMENT

This research was supported by the Basic Science Research Program through the National Research Foundation Korea funded by the Ministry of Education (NRF-2017R1D1A3B03033852).

The chip fabrication was provided by MPW of IDEC.

REFERENCES

[1] M. Mohammed, K. Abugharbieh, M. Abdelfattah, and S. Kawar, “Design methodology for MOSFET-based voltage reference circuits implemented in 28 nm CMOS technology,” *Int. J. Electron. Commun. Int. J. Electron. Commun.*, vol. 70, no. 5, pp. 568–577, 2016.

[2] Y. P. Tsividis, “Accurate analysis of temperature effects in I/SUB c/V/SUB BE/ characteristics with application to bandgap reference sources,” *IEEE J. Solid-State Circuits*, vol. 15, no. 6, pp. 1076–1084, Dec. 1980.

[3] H. Banba et al., “A CMOS bandgap reference circuit with sub-1-V operation,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

[4] G. De Vita and G. Iannaccone, “A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator,” *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536–1542, 2007.

[5] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, “A 2.6 nW, 0.45 v temperature-compensated subthreshold CMOS voltage reference,” *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, 2011.

[6] A. Saberkari, R. Fathipour, H. Martinez, A. Poveda, and E. Alarcon, “Output-capacitorless CMOS LDO regulator based on high slew-rate current-mode transconductance amplifier,” Proc. - *IEEE Int. Symp. Circuits Syst.*, pp. 1484–1487, 2013.

[7] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, “Full On-Chip CMOS Low-Dropout Voltage Regulator,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.

[8] P. Y. Or and K. N. Leung, “An output-capacitorless low-dropout regulator with direct voltage-spike detection,” *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458–466, 2010.

[9] P. Y. Or and K. N. Leung, “An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection,” *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458–466, Feb. 2010.

[10] M. Ho and K. N. Leung, “Dynamic Bias-Current Boosting Technique for Ultralow-Power Low-Dropout Regulator in Biomedical Applications,” *IEEE Trans. Circuits Syst.* II Express Briefs, vol. 58, no. 3, pp. 174–178, Mar. 2011.

[11] S. Chong and P. K. Chan, “A 0.9-µ A Quiescent Current Output-Capacitorless LDO Regulator With Adaptive Power Transistors in 65-nm CMOS,” *IEEE Trans. Circuits Syst.* I Regul. Pap., vol. 60, no. 4, pp. 1072–1081, Apr. 2013.

[12] R. Fathipour, A. Saberkari, H. Martinez, and E. Alarcón, “High slew rate current mode transconductance error amplifier for low quiescent current output-capacitorless CMOS LDO regulator,” Integr. *VLSI J.*, vol. 47, no. 2, pp. 204–212, Mar. 2014.

[13] B. J. Hosticka, “Improvement of the gain of MOS amplifiers,” *IEEE J. Solid-State Circuits*, vol. 14, no. 6, pp. 1111–1114, Dec. 1979.

[14] E. Sackinger and W. Guggenbuhl, “A high-swing, high-impedance MOS cascode circuit,” *IEEE J. Solid-*

State Circuits, vol. 25, no. 1, pp. 289–298, 1990.
[15] M. Ho, K. N. Leung, and K. L. Mak, “A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages,” *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2466–2475, 2010.
[16] Ka Nang Leung and P. K. T. Mok, “A capacitor-free cmos low-dropout regulator with damping-factor-control frequency compensation,” *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

Sadeque Reza Khan received the B.Sc. degree in electronics and telecommunication engineering from the University of Liberal Arts Bangladesh, and the M.Tech degree in VLSI design from National Institute of Technology Karnataka (NITK), India.

He is currently working toward PhD degree at SoC Design Lab, Chosun Univrsity, Korea. His research interests include low power VLSI, microelectronics, control system design, and embedded system design.

Goang Seog Choi received the B.S. and M.S. degrees in electronic engineering from Pusan National University, Korea, in 1987 and 1989, respectively, and the Ph.D. degree from Korea University, Korea, in 2002.

From 1989 to 2006, he was with Samsung Electronics Company, Ltd., Korea designing ASIC/SoC in digital media applications. Since 2006, he has been with the Dept. of Information and Communication Engineering, Chosun University, Korea. His recent research interests include ASIC/SoC design for digital media and communications, and microprocessor application.