Equivalent circuit model of MIM capacitor on silicon interposer for power distribution network impedance analysis

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***Abstract* - MIM capacitor test sample has been designed for modeling of the MIM capacitor on silicon interposer or chip. Equivalent circuit model of MIM capacitor is proposed, and the circuit model is verified using vector network analyzer (VNA) measurement. With the extracted parasitic components such as MIM capacitor capacitance, coupling parasitic capacitance and coupling parasitic parallel resistance, the self-impedance of the equivalent circuit model can be obtained. This circuit model is able to be applied for in chip or silicon interposer PDN. Also, the proposed model can be used to evaluate impedance of the chip accurately.**

***Keywords*—MIM Capacitor, Silicon Interposer, Power Distribution Network**

I. INTRODUCTION

Silicon interposer technology is applied in various systems to overcome the physical limitations of the conventional two-dimensional systems in package (2D-SiP) through vertical interconnection and by shortening the interconnection length between different chips. As shown in Fig. 1, using the silicon interposer technology can increase the number of input/output pads to achieve high data bandwidth. Also, the power integrity is secured using the silicon interposer technology by increasing the number of power/ground balls.

The electrical advantages of the silicon interposer technology is the relatively low RC delay and low input/output power consumption due to relatively low interconnection capacitance. However, the low interconnection capacitance may cause undesired effects such as cross talk, reflection due to low impedance and high frequency loss leading to intersymbol interference (ISI) and eye-diagram distortion. Furthermore, the high frequency components from the harmonic generation are coupled to neighboring interconnections and active circuits and may result in unwanted effects which may lead to a system failure. Hence, the paracitic characteristics of the power distribution network (PDN) and passive components on the silicon interposer must be carefully modeled before deigning a silicon interposer [1]-[3].

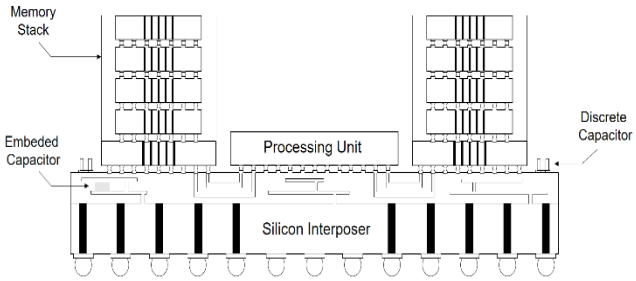

Fig. 1. An illustration of possible silicon interposer for HBM. Silicon interposer is composed of passive components such as embedded capacitor and discrete capacitors.

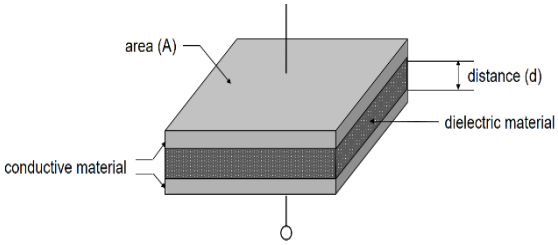

Fig. 2. A simplified illustration of an ideal capacitor.

By fabricating the metal-insulator-metal (MIM) capacitors, which can be used to lower the PDN impedance in a silicon interposer, we demonstrated the parasitic high frequency characteristics. We proposed and verified an equivalent circuit model for the MIM capacitor, which can be used up to 20 GHz.

II. EXPERIMENTS

Conventionally, the embedded capacitors are modeled assuming the structure shown in Fig. 2. Ideally, the voltage across the two plates, V, is given as:

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$$V = \int_0^d E\ dz = \int_0^d \frac{\rho}{\varepsilon}\ dz = \frac{\rho d}{\varepsilon} = \frac{Qd}{\varepsilon A}$$

where E is the electric field between the two plates, A is the Area of the conductive metal plate, ρ is the charge density and, ε is the dielectric constant of the dielectric material and Q is the total charge between the two plates. Since the capacitance, C, is defined as:

$$C = \frac{Q}{V}$$

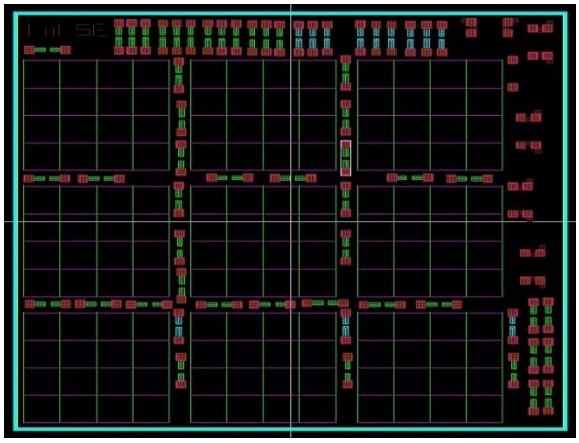

Fig. 3. Fabricated chip design

Therefore, capacitance can be rearranged as:

$$C = \frac{\varepsilon A}{d}$$

Therefore, metal-insulator-metal capacitance can be extracted. Ideally, the MIM capacitor can be modeled with the single capacitance value at all frequency. However, due to parasitic components, the self-impedance shows change in slope at different frequency. To model the parasitic components as an equivalent circuit model, one of the MIM capacitors from the fabricated sample shown in Fig. 3 is selected. 1 pF capacitor is selected for modeling.

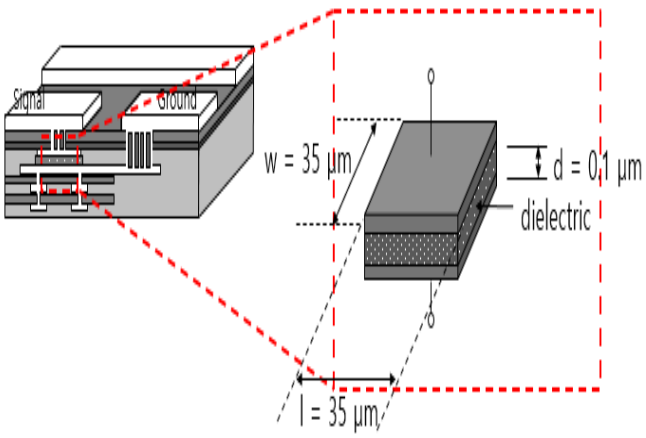

Fig. 4. Simplified schematic of the fabricated MIM capacitor.

The dimension of the 1pF MIM capacitor is shown in Fig. 4. The width and the length of the metal above the dielectric material, silicon nitride. Using the capacitance formula, 1 pF capacitance can be calculated.

III. RESULTS AND DISCUSSIONS

Using a vector network analyzer (VNA), the s-parameter of the test sample was measured. The obtained s-parameter is converted to self-impedance of the MIM capacitor. The measured self-impedance of the MIM capacitor is shown in Fig. 5. Constant capacitance should result in linear decrease in log scale graph of frequency vs. self-impedance. Due to parasitic components of the MIM capacitor, self-impedance slope at frequency regions below 100 MHz and above 1 GHz changes. Therefore, to accurately evaluate the impact of MIM capacitor on the chip-level or interposer power distribution network, an equivalent circuit must be proposed.

Therefore, we proposed an equivalent circuit model for the MIM capacitor which can be used for wide frequency range from 30 kHz to 20 GHz. The proposed equivalent circuit model is given in table I. C_{MIMCAP} refers to the MIM capacitor capacitance, which is 1 pF. $C_{coupling}$ refers to the coupling parasitic capacitance, and $G_{coupling}$ refers to the coupling parasitic parallel resistance. $C_{coupling}$ and $G_{coupling}$ result from metal trace and other interconnecting parasitic components for the MIM capacitor sample. G_{MIMCAP} refers to the parallel resistance between two contact pad metals through silicon substrate. Using the measurement results the three parasitic component values are extracted by fitting the equivalent circuit to the measurement result. $C_{coupling}$ value is 700 fF, $G_{couplin}$ value is 8.33 mS and G_{MIMCAP} value is 30.3 μS. G_{MIMCAP} results from the bulk silicon resistance between the two contact pad metals which goes through the bulk silicon substrate. Higher doping concentration of silicon or increase in size of the contact pad will decrease the resistance between the two pads. The equivalent circuit component values are given in Table I.

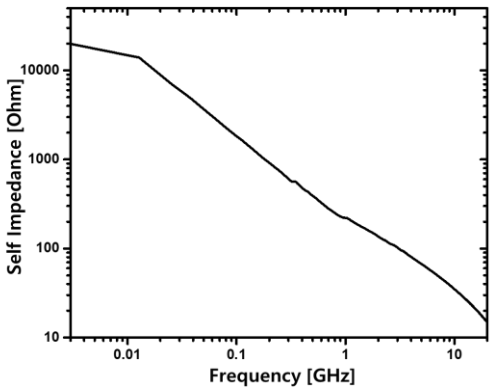

Fig. 5. Measured self-Impedance of the 1 pF MIM capacitor sample.

Below 100 MHz, the self impedance changes abruptly in Fig. 5. Such abrupt change results from the VNA measurement with low number of linear frequency steps. If the measurement were to be done with log scale with more

TABLE I. MIM Capacitor Equivalent Circuit Model Components

Equivalent Circuit Model Component	Parameter
C_{MIMCAP}	1.0 pF
$C_{coupling}^{*}$	700 fF
$G_{coupling}^{*}$	8.33 mS
G_{MIMCAP}	30.3 μS

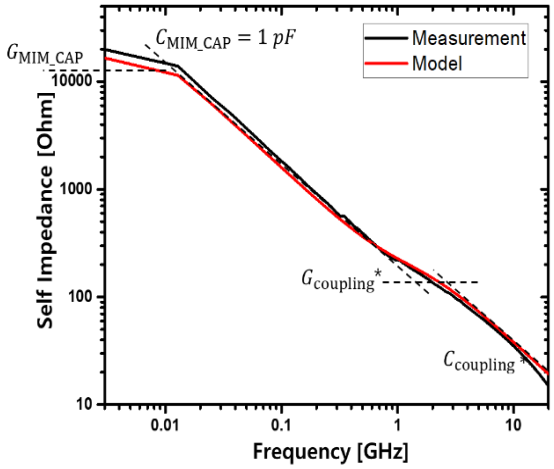

Fig. 6. Equivalent circuit verification using the measurement results.

frequency measurement points, such abrupt change in slope will not be observed.

With the extracted parasitic components and calculated MIM capacitor capacitance value, the self-impedance of the equivalent circuit model can be obtained. The equivalent circuit model is verified with the measurement results as shown in Fig. 6.

IV. CONCLUSION

In this paper, we have proposed an equivalent circuit model of the MIM capacitor which can be used in chip or silicon interposer PDN. Our model can be used to evaluate accurate impedance of the chip or silicon interposer PDN impedance analysis.

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REFERENCES

[1] Sunohara, Masahiro, et al. "Silicon interposer with TSVs (Through Silicon Vias) and fine multilayer wiring." Electronic Components and Technology Conference, 2008. ECTC 2008. 58th. IEEE, 2008.

[2] Zhang, Xiaowu, et al. "Development of through silicon via (TSV) interposer technology for large die (21× 21mm) fine-pitch Cu/low-k FCBGA package." Electronic Components and Technology Conference, 2009. ECTC 2009. 59th. IEEE, 2009.

[3] Yoon, Kihyun, et al. "Modeling and analysis of coupling between TSVs, metal, and RDL interconnects in TSV-based 3D IC with silicon interposer." Electronics Packaging Technology Conference, 2009. EPTC'09. 11th. IEEE, 2009.

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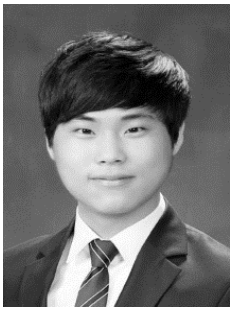

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Joung Ho Kim received B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1984 and 1986, respectively, and Ph.D degree in electrical engineering from the University of Michigan, Ann Arbor, in 1993. In 1994, he joined Memory Division of Samsung Electronics, where he was engaged in Gbit-scale DRAM design. In 1996, he moved to KAIST (Korea Advanced Institute of Science and Technology). He is currently professor at electrical engineering department of KAIST. Also, he is director of 3DIC-RC (3DIC Research Center) supported by SK Hynix Inc, and SAE-RC (Smart Automotive Electronics Research Center) supported by KET Inc.

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He has authored and co-authored over 440 technical papers published at refereed journals and conference proceedings. Also, he has given more than 242 invited talks and tutorials at the academia and the related industries. Recently, he published a book, “Electrical Design of Through Silicon Via,” by Springer in 2014. Dr. Joungho Kim will be Conference chair of IEEE EDAPS 2015 in Seoul, and Joint conference chair of Japan-Korea Microwave society in 2015. He also was the conference chair of IEEE WPTC (Wireless Power Transfer Conference) 2014, held in Jeju Island, Korea. And he was the symposium chair of IEEE EDAPS Symposium 2008, and was the TPC chair of APEMC 2011. He is also an associated editor of the IEEE Transactions of Electromagnetic Compatibility. He served as a guest editor of the special issue in the IEEE Transactions of Electromagnetic Compatibility for PCB level signal integrity, power integrity, and EMI/EMC in 2010, and also as a guest editor of the special issue in the IEEE Transactions of Advanced Packaging for TSV (Through-Silicon-Via) in 2011. He serves as a guest editor of the mini-special issue in the IEEE Transactions of Microwave Theory and Techniques, for IEEE WPTC in 2014. He received Outstanding Academic Achievement Faculty Award of KAIST in 2006, KAIST Grand Research Award in 2008, National 100 Best Project Award in 2009, KAIST International Collaboration Award in 2010, and KAIST Grand Research Award in 2014, respectively. He was appointed as an IEEE EMC society distinguished lecturer in a period from 2009-2011. He received Technology Achievement Award from IEEE Electromagnetic Society in 2010. Recently, he published a book, “Electrical Design of Through Silicon Via,” at Springer.