Highly Efficient Envelope-Tracking Modulator Over Wide Output Power Range for Dual-Mode Power Amplifier

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Abstract – This paper presents a highly efficient envelope-tracking (ET) modulator over wide output power range. The ET modulator is designed to operate with a dual-mode power amplifier (PA). The supply voltage of the linear regulator is adjusted according to the average power level for further enhanced efficiency at a low power region. An adaptive bias circuit is designed to avoid the crossover distortion generated by the adjusted supply voltage. For a 10-MHz long term evolution signal with a peak-to-average power ratio of 7.44 dB, the ET modulator delivers measured efficiencies of 76.9% and 62.5% at the maximum output power and 10-dB back-off power, respectively. The measured efficiency at the 10-dB back-off power is enhanced by 10% point, while maintaining the peak efficiency.

I. INTRODUCTION

The advanced mobile systems adopt spectrally efficient complex modulation schemes owing to the demand for high data rate services. The RF signals employed in these systems have high peak-to-average power ratios (PAPR) and wide channel bandwidths (BW). Unfortunately, a radio frequency power amplifier (RF PA), which consumes a large power in RF transmitters, has a low efficiency under these conditions to satisfy a good linearity. Therefore, the efficiency improvement techniques of the RF PA become an important research item [1]-[14].

Fig. 1. Block diagram of ET system.

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Envelope-tracking (ET) technique has been extensively studied to achieve the high efficiency and good linearity, simultaneously [1]-[10]. The ET system delivers high efficiency by replacing the fixed DC supply to the dynamic supply voltage, which closely tracks the envelope of the transmitted RF signal, as shown in Fig. 1. The ET modulator in the ET system dynamically supplies the supply voltage to the RF PA, which is optimal voltage for the envelope power generation. The modulator has a hybrid structure, in which a highly efficient switching converter is combined with a wide BW linear regulator via a feedback loop. The switching converter supplies most of the current to the RF PA with a high efficiency. The linear regulator covers the remaining high frequency signal components with a high speed. Therefore, the ET modulator achieves high efficiency and high speed, simultaneously. The linear regulator and switching converter are optimized separately for their own functions. Synchronism of the two amplifiers is also important for high efficiency with a stable operation.

Dual-mode PAs, which have different paths with optimized device sizes, have been also investigated to save current for low power operation [12]-[14]. These PAs improves the efficiency at the low power region. However, one of the main drawbacks of the conventional dual-mode PAs is rapid decrease of the efficiencies at back-off power regions from the maximum powers in both high and low power modes. Therefore, we have designed an ET modulator for ET operation of the dual power-mode PA. In addition, The supply voltage of the linear regulator in the ET modulator is adjusted according to the average power level for further enhanced efficiency at the low power region. For this purpose, an adaptive bias circuit is designed to avoid the crossover distortion generated by the adjusted supply voltage. Although the ET modulator for ET operation of the dual power-mode PA and DC supply adjustment technique are demonstrated in [7] and [8], respectively, this paper presents more detailed analyses.

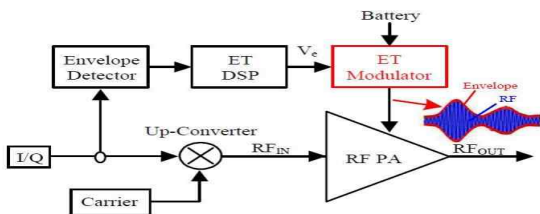This paper is organized as follows. Section II describes the ET modulator for ET operation of the

dual-mode PA. Section III proposes the adaptively biased linear regulator to implement the DC supply adjustment technique. Section IV presents the proposed ET modulator architecture. Section V presents the measurement results, and conclusions are discussed in Section VI.

II. ET MODULATOR FOR DUAL-MODE PA

A. Concept

The load impedances of the dual-mode PAs are optimized for each mode operation. Generally, the optimum output impedance of the low-power mode (LPM) with a small device is higher than that of the high-power mode (HPM). Depending on the output power requirement, the PA is switched between the HPM and LPM, achieving higher efficiency in the LPM. Although the PA provides high efficiency at the maximum output powers in the two power-modes, the efficiencies at the back-off power region decrease rapidly when the PA is operated at a large back-off from their maximum output powers. To address this limitation, we have developed an ET modulator for the ET operation at the HPM and LPM, as depicted in Fig. 2(a). The dual-mode PA with the ET operation can have a enhanced efficiency over the wide output power region, as shown in Fig. 2(b).
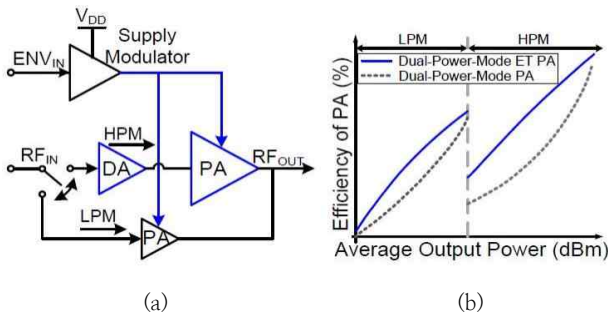

Fig. 2. (a) ET PA structure with dual-mode PA. (b) Efficiency curve of the dual-mode PA and ET PA.

B. Stability

To design and implement the ET modulator with a stable operation, we have analyzed the RF PAs in the HPM and LPM. The load of the ET modulator is modeled as introduced in [2]. In this paper, the modeled loads are 7.5 Ω and 75 Ω in HPM and LPM, respectively. The different load conditions in the two power-modes can deteriorate stability of the ET modulator. A typical structure of the linear regulator consists of an operational transconductance amplifier (OTA), class-AB biasing circuit, and buffer, as shown Fig. 3. The dominant pole in this structure can be expressed as where $G_{m.buffer}$ is transconductance

$$p_1 \approx \frac{-1}{r_{o.OTA} \cdot G_{m.buffer} \cdot R_L \cdot C_C} \qquad (1)$$
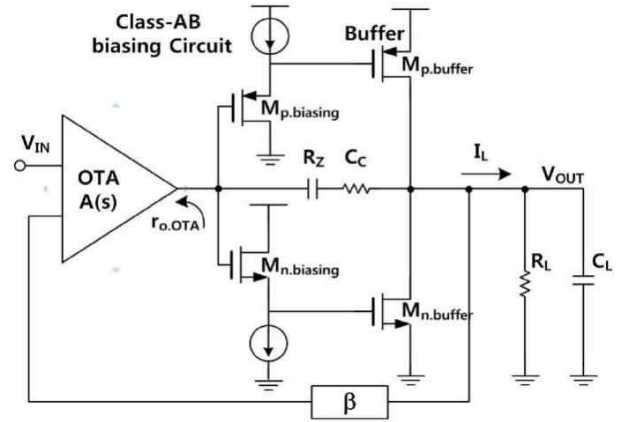

Fig. 3. Typical structure of a linear amplifier.

of the buffer, $r_{o.OTA}$ is output resistance of the OTA, C_C is frequency compensation capacitance, and R_L is load resistance. A DC gain of the linear regulator can be also written as

$$A_{tot}(s) = A(s) \cdot G_{m.buffer} \cdot R_L \qquad (2)$$

where A(s) is dc gain of the OTA. Because of the ten times larger load resistance (R_L) in LPM, the dominant pole of the LPM is located at a lot lower frequency than that of HPM, and the dc gain in LPM is also larger than that of HPM, as shown in Fig 4. The dominant pole located at the lower frequency with the larger dc gain can cause unstable operation with decreased phase margin (PM). To compensate the increased load resistance in LPM, the buffer size is reduced for the lower $G_{m.buffer}$ in (1) and (2), implemented by switch in the buffer (see Fig. 5). In HPM, all buffers (M1−M4) in the linear regulator operate, while only M2 and M4 of
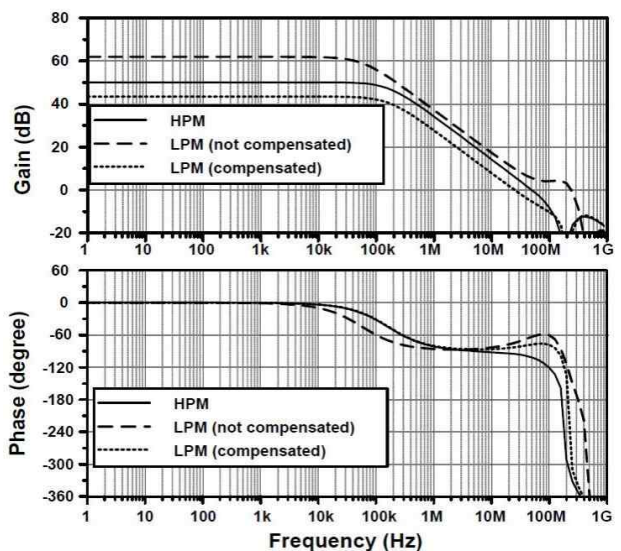

Fig. 4. Simulated frequency responses of linear regulator with HPM and LPM PA loads.(HPM : 7.5Ω, LPM : 75Ω)
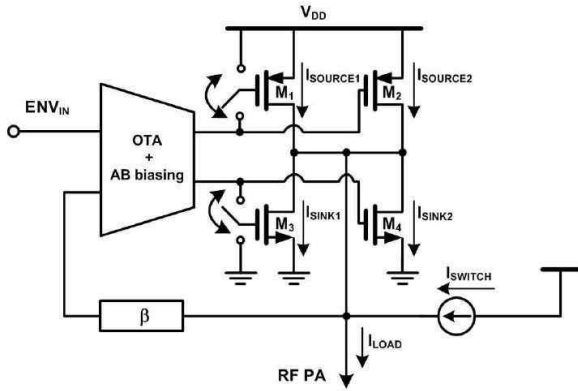
Fig. 5. Linear regulator with buffer size adjustment for a stable operation.

the buffer operate in LPM. The dominant pole in LPM is almost the same with that of HPM by the buffer size adaptation as shown in Fig. 4, and PM is improved, ensuring the stable operation in two different load resistances.

C. Efficiency Improvement

The output current and switch current can be expressed as

$$I_{OUT} = \frac{V_{OUT}}{R_L} \qquad (3)$$

$$\Delta I_{SW} = \frac{1}{L} \cdot V_L \cdot \Delta t \qquad (4)$$

where I_{OUT} and V_{OUT} are output current and voltage, respectively. L is inductance of the switching converter, V_L is voltage across the inductor, and ΔI_{SW} and Δt are variations of the switch current and time, respectively. The I_{OUT} is reduced due to the larger R_L in LPM, while ΔI_{SW} is not changed as shown in Fig. 6, because L and V_L of LPM are the same as those of HPM. At LPM, the I_{OUT} is switched with the same $\Delta I_{SW,}$ and the
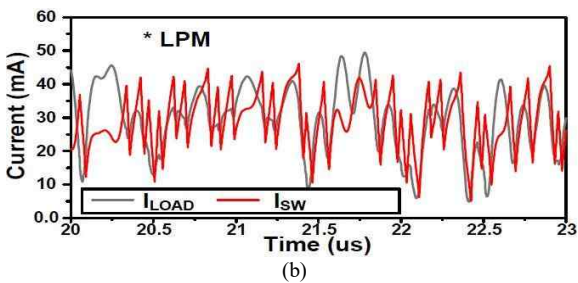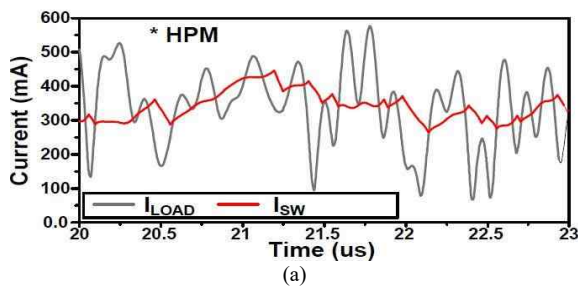
switching frequency is increased, generating high frequency distortions at the output. The efficiency of the ET modulator is degraded because of the increased switching loss. We estimate the inductance in the switching converter for a high efficiency operation of the ET modulator in HPM and LPM load conditions, as shown in Fig. 7. For HPM operation, the inductance of 1.5 uH – 2.2 uH is optimum value, while the optimum inductance in LPM is 10 uH – 25 uH. The optimum inductances in LPM and HPM are quite different. To achieve high efficiency in the two power-modes, a compromised inductance of 4.7 uH, which is larger than the previously used inductance (2.2 uH), is employed. Although the inductance in the switching converter is increased to reduce the switching frequency, the switching loss is still dominant power loss at LPM. To decrease the switching loss, the power transistor size in the switching converter is reduced for lower capacitance of the switcher. To test the optimum power transistor size of the switching converter, we simulate the efficiency of the switching converter with
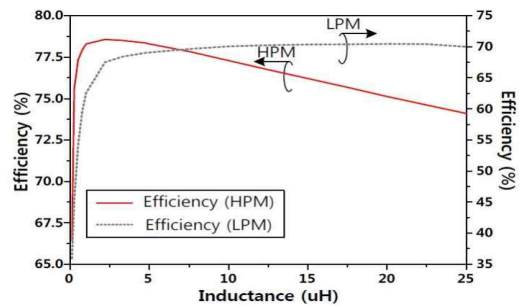

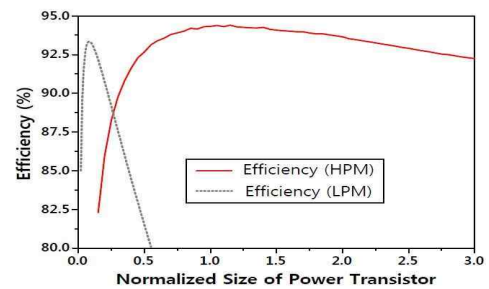Fig. 7. Efficiency according to the inductance in switching converter for HPM and LPM operation.

Fig. 8. Efficiency of switching converter over normalized size of power transistor for two different modeled loads.

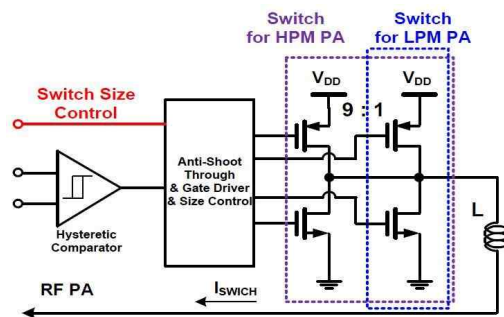Fig. 6. Simulation results of load and switch current. (a) HPM operation. (b) LPM operation.

Fig. 9. Switching converter with size control for dual power-mode PA.

various power transistor sizes at the two power-modes, and the results are depicted in Fig 8. The power transistor size is normalized based on the optimum size at the HPM. The optimum power transistor size at the LPM is ten times smaller than that of HPM. In LPM, the switching converter operates with only M6 and M8, while it operates with all power transistors (M5–M8) in the HPM as shown in Fig. 9. It is easily implemented by the digital logic gates with a mode control. By controlling the size of power transistor, the switching converter delivers the high efficiency in the two power-modes.

III. ADAPTIVELY BIASED LINEAR REGULATOR

A. Concept

For further enhanced efficiency of the ET PA at the back-off power region, we have adjusted the supply voltage of the linear regulator according to the average power level, which is similar to the average power tracking (APT) [11] as shown in Fig. 10. Although the current portion of the linear regulator is small, it increases the overall efficiency of the ET modulator because the efficiency of the regulator is drastically decreased at a low power level. However, when the supply voltage of the linear regulator is reduced, the bias state of the push-pull output stage is changed from a class-AB to a class-B. In the class-B bias state, the linear regulator generates the crossover distortion noise at the output. Therefore, it is important to maintain the bias state even if the supply voltage is adjusted. We have designed an adaptively biased linear regulator to avoid the crossover distortion noise.
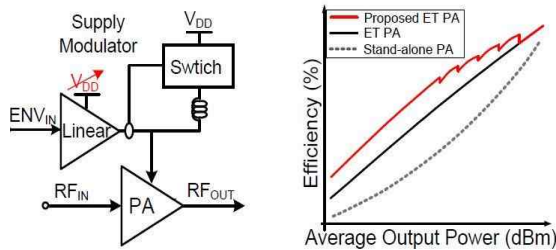
Fig. 10. (a) ET PA with linear-supply-adjusted ET modulator. (b) Expected efficiency curve.

B. Circuit Implementation

Fig. 11 shows a rail-to-rail push-pull configuration with the adaptive bias. The load and the switching converter are simplified as a resistor and a DC current source, respectively. In the conventional structure (see Fig. 3), it is possible to maintain a class-AB biased operation using only the constant voltage source (V_2, V_3) with a fixed supply voltage. However, the supply voltage of the proposed linear regulator is adjusted according to the average power level, and a variable voltage source (V_1) is needed to maintain the class-AB bias state. The proper values of V_1, V_2, and V_3 for the proposed case are estimated according to the supply

voltage and compared with V_2' and V_3' of the conventional case in Fig. 12. At the peak supply voltage (5 V), the voltage source summation ($V_1+V_2+V_3$) of the proposed structure is almost the same as that (V_2'+V_3') of the conventional structure. However, when the supply voltage is reduced, the adaptively biased linear regulator maintains the class-AB biased operation by adjusting the V_1, while the conventional linear regulator generates the crossover distortion because the bias state is changed from class-AB to class-B.

Fig. 13 shows the circuit topology of the adaptively biased linear regulator. To maintain the class-AB bias state regardless of the supply
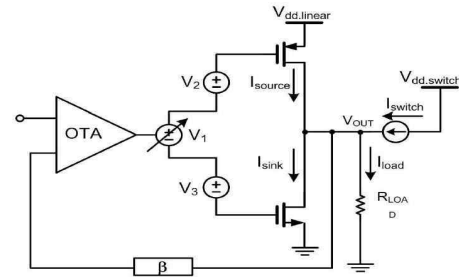
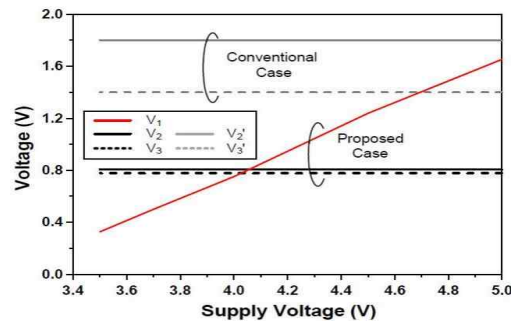Fig. 11. Simplified block diagram of the adaptively biased linear regulator.

Fig. 12. Magnitudes of voltage sources according to the supply voltage for adaptive bias.

voltage, the floating class-AB control (M9, M10) and the floating voltage sources (M17, M18) are designed to operate as the variable voltage source (V_1) and constant voltage sources (V_2, V_3), respectively. The floating class-AB control is designed based on [15]. The floating voltage sources are designed the same way as the conventional structure [1]. The proposed linear regulator maintains the class-AB bias state even if the supply voltage is adjusted, resulting in high efficiency over the entire output power range.
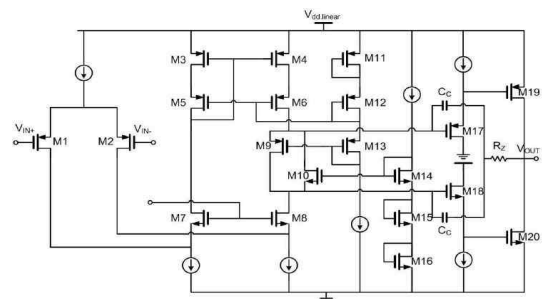
Fig. 13. Schematic of adaptively biased linear regulator.

IV. PROPOSED ET MODULATOR

Fig. 14(a) shows the proposed ET system in this paper. The ET modulator is designed considering the stability and efficiency for applying to the dual-mode PA. In addition, the supply voltage of the linear regulator is adjusted
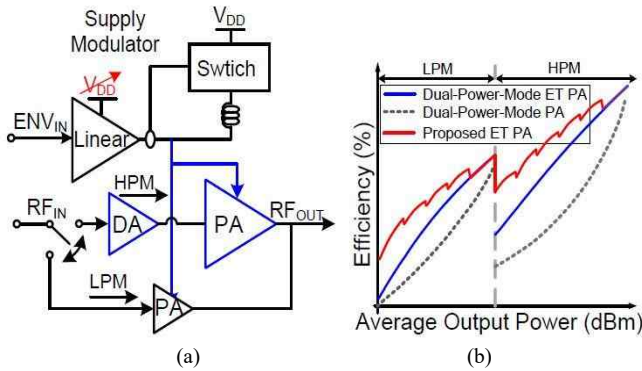

Fig. 14. (a) Proposed ET PA. (b) Expected efficiency curve.
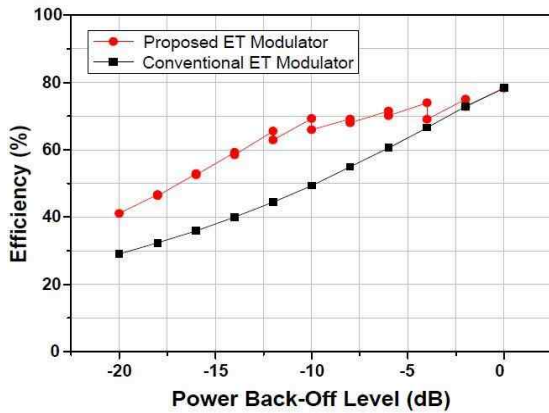

Fig. 15. Simulated efficiencies of the proposed and conventional ET modulators

according to the average power level of the input signal for further enhanced efficiency at the back-off power region, and the operation is similar to the APT operation of the conventional PA. Fig. 14(b) illustrates the expected efficiency curve of the ET PA when the proposed ET modulator is applied to the dual-mode PA. The efficiency will be significantly improved over a broad power range by combining the proposed ET modulator with the dual-mode PA.

Fig. 15 illustrates the simulated efficiencies of the proposed and conventional ET modulators. As expected, the proposed ET modulator has a higher efficiency compared to the conventional ET modulator. In the proposed modulator, the efficiency decrement at LPM is more rapid than that of HPM, because the quiescent current strongly affects to the efficiency in LPM, whose output current is much smaller than that of HPM.

Fig. 16 shows the proposed ET modulator architecture. The adaptively biased linear regulator is employed to maintain the class-AB bias state regardless of the supply voltage of the linear regulator. The size of the buffer is adjusted for stable operation in HPM and LPM, and the switch size is also controlled by the digital logic for the maximized efficiency at each power-mode.

The proposed ET modulator delivers a swing range of 0.5 V – 4.5 V to the 7.5 Ω and 75 Ω loads at the maximum output powers of the HPMand LPM, respectively. The swing range is considered the linear operation of the PA without having the knee effect and the voltage drop through the pass transistor of the linear regulator.

The maximum output powers in HPM and LPM are 905.7 mW and 88.2 mW with the simulated efficiencies of 78.4% and 69.1%, respectively. Especially, the simulated efficiency in LPM is improved by 19.8% point using the proposed techniques. The simulated performance of the designed ET modulator is summarized in Table I.
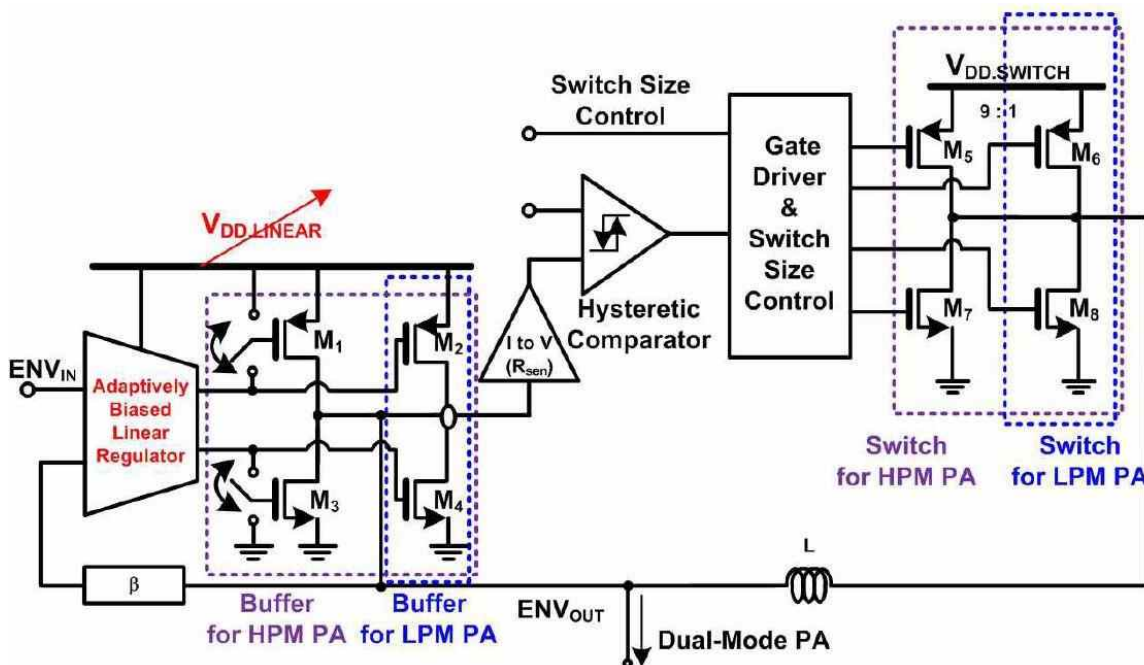

Fig. 16. Block diagram of the proposed ET modulator.

TABLE I.
Performance Summary of Designed ET Modulator
for 10-MHz LTE Signal

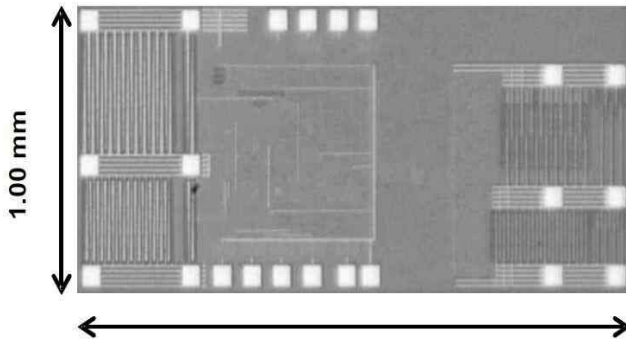| Parameters	HPM	LPM
Signal	10-MHz LTE	
Swing Range	0.5 V - 4.5 V	
Pout	905.7 mW	88.2 mW
Load Resistance	7.5 Ω	75 Ω
Switching Frequency	3.6-MHz	5.3-MHz
Efficiency	78.4%	69.1%
Technology	Dongbu 0.35um BCDMOS	

Fig. 17. Chip microphotographs of the ET modulator.
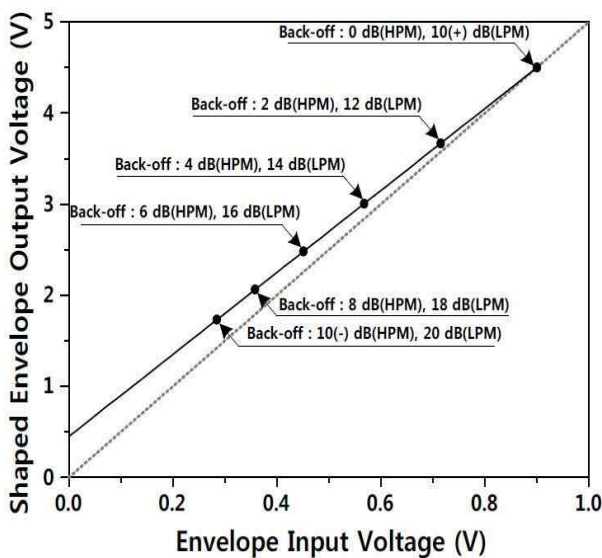
V. MEASUREMENT RESULTS

Fig. 18. Envelope shaping function for ET operation of dual power-mode. (Output/input gain is 5.)

The proposed ET modulator is fabricated using Dongbu 0.35-um BCDMOS process, and the Chip microphotograph of the fabricated ET modulator is shown in Fig. 17. This modulator is 2.31 mm x 1.0 mm, including all the pads.
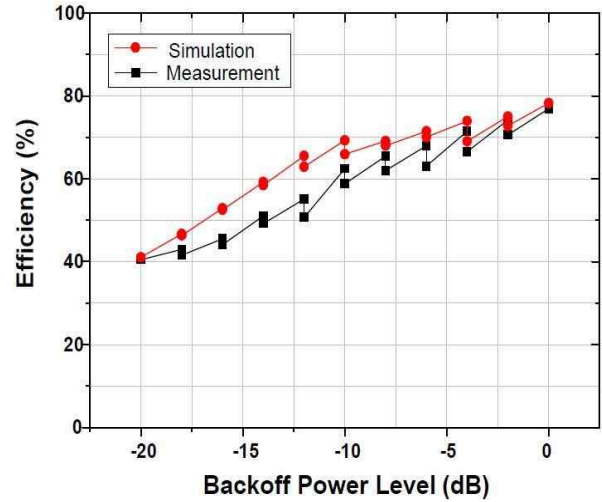

Fig. 19. Measured efficiencies of the proposed and conventional ET modulators

An envelope shape for the ET operation of the dual-mode PA is shown in Fig. 18, which follows the sweet spot tracking until 10-dB back-off as introduced in [2]. At the 10-dB back-off power, the envelope is reshaped with the mode change, and the peak voltage of the envelope is 4.5 V, which is the same as the peak voltage in HPM.

To test performance of the proposed ET modulator, the PA is simply modeled as 7.5 Ω and 75 Ω resistive loads for HPM and LPM, respectively. The test signal is the 16-quadrature amplitude modulation (QAM) LTE envelope signal with 7.44-dB PAPR and 10-MHz BW. By employing the proposed techniques, the designed ET modulator has a higher efficiency over a broad power range. The measured efficiency is compared with the simulated efficiency, as shown in Fig. 19. The measured efficiencies in the low power region is lower than simulated efficiencies, because the quiescent current is larger in measurement compared to the simulation. The quiescent current degrades severely the efficiency at LPM, because the output current is much smaller than that of HPM. The ET modulator delivers 4.5 V peak voltage with the measured efficiencies of 76.9% and 62.5% at the maximum power and 10 dB back-off power for the HPM and LPM, respectively. At the 10-dB back-off power, the measured efficiency is improved from the 52.5% to 62.5%.

VI. CONCLUSIONS

A highly efficient ET modulator is implemented using a Dongbu 0.35-um BCDMOS process. By a proper size adaptation of the buffer in the linear regulator and the power transistor in the switching converter, the efficiency of the ET modulator is improved in the whole back-off power region with a stable operation. For further enhanced efficiency, the supply voltage of the linear regulator is adjusted following the APT technique and the adaptively biased linear regulator is properly designed to avoid the crossover distortion with the several supply voltages. An envelope shaping method is also employed to implement the proposed ET modulator. For a 10-MHz LTE signal with PAPR of 7.44 dB, the ET modulator delivers 4.5 V peak voltage with the measured efficiencies of 76.9% and 62.5% at the maximum power and 10 dB back-off power for the HPM and LPM, respectively. The ET modulator improves the measured efficiency of 10% point at the 10 dB back-off power. This ET modulator can be a promising structure with the dual-mode PA to maintain a high efficiency over a broad output power range in the future transmitter systems.

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Prof. Kim is a member of the Korean Academy of Science and Technology and the National Academy of Engineering of Korea. He was an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) and an AdCom member.